AMICSA & DSP 2016

Sunday 12 June 2016 - Thursday 16 June 2016

Gothenburg, Sweden

Proceedings

Table of Contents

AMICSA: Space applications for analogue and mixed-signal ICs

Rad-Hard Microcontroller For Space Applications

Fredrik Johansson, Jan Andersson, Fredrik Sturesson,
Nils-Johan Wessman, Magnus Hjorth
Cobham Gaisler, Kungsgatan 12, SE-411 91, Göteborg, Sweden
Tel: +46 31 775 86 50
info@gaisler.com

Steven Redant, Wim Sijbers, Geert Thys
IMEC
Kapeldreef 75, 3001 Leuven, Belgium
Tel: +32 16 28 11 41
info@imec.be

Claudio Monteleone
European Space Agency,
Keplerlaan 1, PO box 299, NL-2220AG Noordwjik, The Netherlands
Tel: +31 71 56 56791
claudio.monteleone@esa.int

ABSTRACT

This paper describes a mixed-signal LEON3FT microcontroller ASIC (Application Specific Integrated Circuit) targeting embedded control applications with hard real-time requirements. The prototype device is currently in development at Cobham Gaisler, Sweden, and IMEC, Belgium, in the activity *Microcontroller for embedded space applications*, initiated and funded by the European Space Agency (ESA).

The presentation and paper will describe the architecture and functionality of the device. This abstract describes an on-going development where the devices are in the architectural design stage before detailed implementation phase. The presentation and final paper will contain further details on the device and will describe the latest progress made within the activity.

BACKGROUND

Software based data acquisition, dataprocessing and simple control applications are widely used in spacecraft subsystems. They allow implementation of software based control architectures that provide a higher flexibility and autonomous capabilities versus hardware implementations. For this type of applications, where limited processor performance are is required, general purpose microprocessors are usually considered incompatible due to high power consumption, high pin count packages, need of external memories and missing peripherals. Low-end microcontrollers are considered more attractive in many applications such as:

- Propulsion system control
- Sensor bus control
- Robotics applications control
- Simple motor control
- Power control
- Particle detector instrumentation
- Radiation environment monitoring
- Thermal control
- Antenna pointing control
- AOCS/GNC (Gyro, IMU, MTM)
- RTU control
- Simple instrument control
- Wireless networking

In these kind of applications the microcontroller device should have a relatively low price, a low power consumption, a limited number of pins and must integrate small amount of RAM and most of the I/O peripherals for control and data acquisition (serial I/Fs, GPIO's, PWM, ADC etc.). The requirements for memory and program length are usually minimal, with no or very simple operating system and low software complexity.

MICROCONTROLLER APPLICATIONS

Spacecraft subsystem control and monitoring of parameters such as power supply voltages, currents, pressures and temperatures are ideal applications for the LEON3FT microcontroller. Bridges between different communication standards or interface of an equipment towards a higher level controller or the central On Board Computer (OBC) are also ideal applications for the LEON3FT microcontroller.

The LEON3FT microcontroller can perform advanced data handling to offload any higher level controller or the central On Board Computer (OBC). By hiding the data handling details the transmitting data volume can be reduced and simplified functionalities and timing requirements are requested to the higher level controller.

The LEON3FT microcontroller integrates several on-chip data bus standards, such as SpaceWire, CAN, MIL-STD-1553, I2C, SPI, UART and can easily provide data packetization for serial communication using standard protocols. The microcontroller can also efficiently replace FPGAs in accomplishing the above functionalities. Generally the FPGA implementation is faster but much more complexity and flexibility can be captured in the software of a microcontroller even with limited processing capability. The correct use of FPGAs in space applications can be complex to achieve and also cost, package size and availability of integrated analog functions can favour the use of a microcontroller with respect to FPGA.

Below are listed a number of possible microcontroller use cases and specific applications.

- Nanosatellite controller
- Instrument Control Unit
- Remote Terminal control
- Mass Memory control
- Propulsion Unit control
- Electric Motor Control

MICROCONTROLLER ARCHITECTURE

Figure 1 shows an overview of the architecture. The system consists of three AMBA AHB buses, one main system bus, one debug bus and one bus for DMA traffic.

The main bus will include the LEON3FT core connected to a shared on-chip RAM and ROM. The main bus also connects all other peripheral cores in the design as well as the external memory controllers. Several peripherals are connected through two AMBA AHB/APB bridges where the bridges are integrated with the design's DMA controller.

The debug AMBA AHB bus connects a serial UART debug communications link and one JTAG debug communication link to the debug support unit and also to the rest of the system through an AMBA AHB bridge.

The third bus, a dedicated 32-bit Debug bus, connects a debug support unit (DSU), AHB trace buffers and several debug communication links. The Debug bus allows for non-intrusive debugging through the DSU and direct access to the complete system, as the Debug bus is not placed behind an AHB bridge with access restriction functionality.

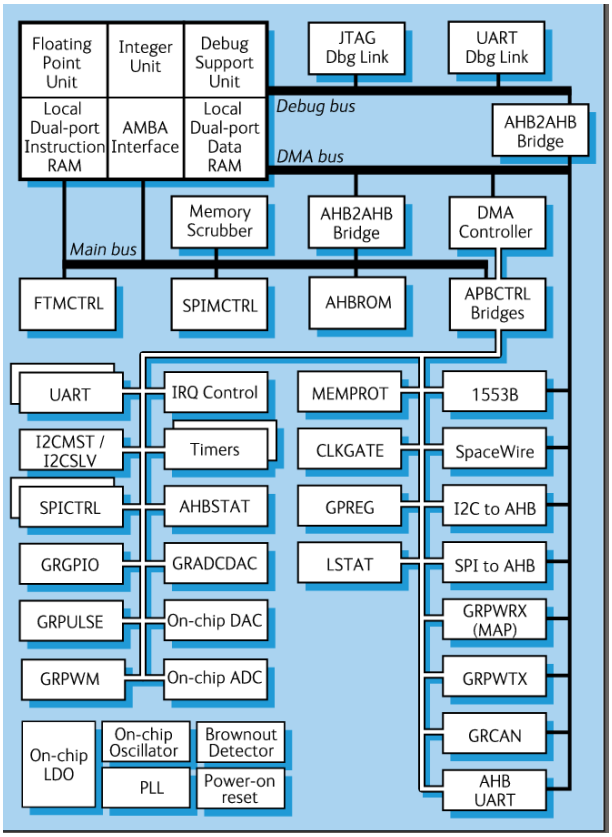


Fig. 1. Architecture overview

The list below summarizes the specification for the system:

- System Architecture
  - LEON3FT 32-bit SPARC V8 processor with LEON reduced instruction set
  - System AHB bus connecting processor, AHB/APB bridges
  - Separate debug AHB bus connecting debug communication links to DSU in order to allow non-intrusive debugging
  - On-chip ROM, SRAM.
  - Off-chip PROM, SRAM and memory mapped IO.
  - Pin sharing via switch matrix
  - Atomic operations
- Processor core
  - LEON3FT with tightly coupled data RAM and tightly coupled instruction RAM, 32-bit MUL
  - GRFPU floating-point unit with 4-word instruction FIFO
  - Reduced instruction set, without removing support for full instruction set.
  - SPARC V8e extensions (SVT, partial WRPSR, alternative window pointer)
  - Debug support unit with performance monitoring and AHB/instruction trace buffers

- Peripherals
  - Integrated on-chip 13-bit ADC/DAC, 100ksps
  - Power On Reset and Brown Out Detector
  - JTAG debug communication link
  - 8-bit UARTs
  - CCSDS CRC accelerator with DMA engine
  - MIL-STD-1553B interface
  - CAN controller
  - SpaceWire
  - General purpose I/O port
  - PWM and Pulse generator
  - PacketWire receiver and transmitter
  - I2C master and slave interface
  - SPI master/slave controller
  - Clock gate unit for power control
  - DMA controller
  - Hardware memory scrubber
  - Memory protection unit
  - Oscillator, PLL and pad control units
  - Temperature sensors
- External memory interfaces
  - Fault-tolerant 8 bit PROM/SRAM/IO controller with BCH ECC
  - SPI memory controller with support for Dual Memory Redundancy and BCH ECC
  - I2C memory controller with support for Dual memory Redundancy

Processor performance and determinism

In order to improve determinism, the LEON3FT microcontroller contains only a local instruction and data static RAM with fixed response times. All EDAC units in the system have the same latency and behaviour in the corrected as in the uncorrected case. This also applies to the CPU, so dynamic SEU handling schemes such as the LEON3FT pipeline restart on error options is not used.

Local instruction RAM tightly coupled to the LEON3FT CPU will be the main memory to execute the software. Due to its direct connection to the CPU, the execution of the software will be deterministic. For applications where full cycle-level determinism is not needed, it will also be possible to execute software from an external SRAM.

The local instruction memory will be implemented using dual-port RAM. The memory's second port will be connected to the main system AHB. This will allow modifying of the local instruction RAM without the intervention of the CPU. The contents of this memory will be protected against SEU errors with EDAC and scrubbing.

If the DMA peripherals and the processor are connected to a shared single-port memory, or to a memory via the same bus, and try to simultaneously access the shared resource then the DMA activity will have an effect on the execution time. On the other hand DMA activity will have no impact on SW execution time by using a dual-port on-chip data RAM and a separate bus for the DMA peripherals. This means that there is a separate access path for the CPU core to local instruction and data RAMs that is unaffected by concurrent DMA activity.

For applications demanding determinism on nested interrupts, a special interrupt handling scheme will be implemented in software where nested interrupts are allowed to occupy one additional register window. The number of levels of nested interrupts that can be handled without additional timing penalty depends on the complexity of the software implementation.

In the architecture, deterministic interrupt latency will be achieved by:

- Running software (including interrupt handlers) from local RAM and accessing any data needed during the interrupt handling through port separate from AMBA ports.
- Adapting the register window usage (using a flat model) structure to avoid unexpected window over/underflow traps. This is done in the compiler and application code, and most OS code does not need modification.
- The alternate window pointer feature from the SPARC V8E extension to allow window over/underflow handlers to run with traps enabled.
- Register file partitioning to allow partitioning of the register file (the windows) to different “contexts”. Contexts can for example be threads to speed up context switching and/or interrupt contexts to dedicate windows to ISRs.

SPARC Reduced instruction set

LEON-REX is an extension to the SPARCv8 instruction set. Similar extensions exist for other architectures such as THUMB/THUMB2 for ARM and MIPS16 for MIPS. The reduced SPARC V8 instruction set variant has been developed by Cobham Gaisler and is integrated into the device.

The main design goal has been to reduce code size, thereby reducing memory storage needed for the code, and to reduce memory bandwidth needed for the instruction code fetching.

Another design goal is to allow retrofitting the extension in existing LEON3/LEON3FT pipelines and into the existing software/compiler stack, and to provide backward compatibility. User can develop C code as usual (with bare-C or a small RTOS) and the existing

LEON environment (GRMON, compilers etc) can be used for development.

LEON REX is designed to allow gradual transition where existing SW environment can be used unmodified and converted piece by piece to use new instruction set.

The compressed instruction set is an optional extension of the SPARC V8 ISA, and existing code can be used without modification. Compressed and regular code can be mixed in the same application, thus the user can avoid changing critical code that has already been validated.

The first version of the instruction set extension has been specified and tested on prototype hardware and tests has shown that a compression ration of 30-50% compared to normal SPARC V8 code is achievable in a real world scenario.

LEON/REX and Runtime improvements

The new LEON/REX alternate window pointer feature (AWP) support and the improved interrupt single vector trap handler (SVT) have been tested and characterized in a series of measurements running on prototype hardware.

By delaying a timer interrupt N clocks into an overflow or underflow trap handling the interrupt latency and interrupt latency jitter as a result of SAVE/RESTORE can be quantified.

Five different software runtime configurations were benchmarked:

- Current BCC SVT
- Improved BCC SVT
- Improved BCC SVT with AWP
- Current BCC MVT
- Current BCC MVT with AWP

In order to understand where the latencies comes from the time from the interrupt is asserted to the time the ISR is reached is split up in three parts presented in the plots below:

- Interrupt assert to acknowledge (assert to first instruction of trap executed)
- Acknowledge to the Interrupt Service Routine (first instruction of trap to first instruction of ISR)
- Total latency (Assert to ISR first instruction)

The worst case interrupt latencies seen when an interrupt is asserted on top of a window underflow/overflow handler are presented in the table below. The highlighted rows are estimates results that can achieved in the LEON/REX environment.

Latency / Config	Assert to Acknowledge		Acknowledge to ISR		Total – Assert to ISR	
	Overflow	Underflow	Overflow	Underflow	Overflow	Underflow
CWP, SVT	134	143	539	281	673	424
CWP, new SVT	70	62	296	166	366	228
AWP, new SVT	**35**	**34**	**202**	**166**	**207**	**200**
CWP, MVT	60	52	262	152	322	204
AWP, MVT	**25**	**24**	**188**	**152**	**193**	**176**

Table 1: Worst case latencies measured

The new LEON/REX architecture also improves the “context” switching by allowing partitioning of the register file (the windows) to different “contexts”. By assigning windows to software threads or interrupts the software execution don't have to wait for the LEON3FT processor to store used windows on the stack.

Benchmark on prototype systems shows a large reduction of software execution time of switching “context”

Programmable DMA controller

Cobham Gaisler has developed a DMA controller able to preform concurrent programmable sequences of data transfers between any on-chip peripherals in the AMBA address space. The DMA controller is able to transfer data both between peripherals, between peripherals and memory and between memory areas. If the accessed memory is internal or external does not matter, as long as the memory is mapped into AMBA address space reachable from the AHB bus where the core is mapped.

The DMA controller has been specifically designed to offload the CPU and provide DMA capabilities to peripherals that do not have an internal DMA engine. The CPU is offloaded by the fact that the peripheral event is directly routed to the DMA controller. By routing events directly to the DMA controller or even directly between peripherals, these interrupts are in effect offloaded from the CPU. These reduce also the number of concurrent interrupts the CPU must handle and that may erode the system determinism.

Pin-multiplexing

The device shall be an attractive solution for a wide range of applications. Because of the small package and high number of interfaces, the functionality of the pins must be configurable and the pins must be shared between several peripherals. The number of configurable user pins has been chosen to be 64.

Clocking, reset and maximum frequency

The maximum operating frequency for the AMBA system is 50 MHz. The device can have separate clock signal inputs for system, SpaceWire, CAN and MIL-STD-1553B interfaces. The clocks signals can also be derived from single source via clock multipliers and dividers inside the device.

In order to avoid problems with reset sequencing, the device has one single reset input that is sequenced internally to provide reset signals to the different clock domains within the device.

SUPPORT FOR PROFILING AND DEBUGGING

The device provides debug interfaces via the JTAG and UART. The dedicated Debug bus allows non-intrusive debugging since the DSU, trace buffers and performance counters can be accessed without causing traffic on the Processor AHB bus.

The design also supports filtering for both the AHB and instruction trace buffers.

The LEON3 statistics unit provides performance counters, with support for filtering, for a large number of events, including:

- Data write buffer hold
- Branch prediction miss
- Total/Integer/Floating-point instruction count
- Total execution count
- AHB bus statistics for Processor AHB bus and Master I/O AHB bus

The interrupt controller in the design supports interrupt time stamping with time stamps interrupt line assertion and processor interrupt acknowledge.

SUPPORT FOR PROM-LESS APPLICATIONS

The device provides an easy access for systems that want to avoid having a boot-PROM connected to the device and prefer to upload software remotely.

The device can be accessed and remotely configured via SpaceWire, SPI, UART and I2C.

TARGET TECHNOLOGY AND PACKAGE

The technology used is UMC 180 nm, using the DARE library from IMEC, and the package is a 132 pin CQFP

SOFTWARE SUPPORT

The architecture is already supported by all operating systems and tool-chains provided by Cobham Gaisler.

CONCLUSION

The device in development is a SPARC V8 microcontroller that is based on the well known LEON architecture. The device is a prototype for a possible future device targeted at microcontroller applications and will have several new features that are not found in contemporary LEON devices. This includes architectural features to improve determinism, availability of the device in a low pin-count package, and support for the reduced instruction set.

Digital Programmable Controller (DPC) : from Concepts to Space Applications

AMICSA 2016

Th. Van Humbeeck, A. Van Esbeen, M. Fossion
Thales Alenia Space Belgium
Emails: firstname.name@thalesaleniaspace.com

Abstract

Thales Alenia Space has completed the development of a radiation hardened mixed-mode circuit: the DPC (Digital Programmable Controller). This system on chip is a major breakthrough in the availability of radiation hardened highly integrated European micro-controller. This component uses the IMEC RHBD DARE on UMC 0.18µ library [6] and analog IP designed full custom by ICsense [4]. The formal Qualification against ESCC9000 is under completion while the first flight models are launched in the manufgactruing process.

First DPC ASIC's were assembled in March 2014. Since this major project milestone, the device has successfully been integrated into quite a large range of applications.

Evaluation board was built allowing end-users to quickly start developing their application. The board is a rich self-contained prototyping tool (i.e. no other devices needed than a USB plug on the SW development PC). It contains a large set of analog peripherals together with classical interfaces used in space applications such as mil-1553, dual CAN, RS4xx … Hence external designers start developing with the DPC in an space system context within less than 2 working days [10] including learning curve of the associated software development tools.

The DPC is an essential building block for the development of intelligent avionics modules that for the first time allows to implement space grade-1 decentralized control such as promoted in the ESA-SAVOIR reference architecture for RTU. DPC is now the core controller of next generation avionics product from Thales Alenia Space where it is used to control power distribution, motor, thrusters, pyro for LEO and GEO satellites.

The DPC plugin module is a small space grade board containing the DPC, drivers, power supply and protection circuit. The designer of a new avionic module for specific scientific missions can easily plug it onto its customized mother board and has only to take care of high voltage or power interfaces.

The DPC has already been transferred outside Thales group to third parties like ONERA for the design of gyro module [10] and to DLR for the design of motor controllers for robotic arm.

I. DPC OVERVIEW

A. Development strategy

The construction of the DPC is the result of a 4 parties project involving IMEC, ICsense and Thales Alenia Space under an ESA development.

IMEC not only has provided the RHBD DARE+ on UMC 0.18µ library, but also extended it with additional features. Dual port memories are being used to transparently perform memory scrubbing in a seamless manner for the processing unit. The DPC embeds 60kbytes of memory split over several banks. Clock gating cells have been also added. As the DPC embeds a large range of features, power consumption may become an issue if all of them would be active simultaneously. At boot time, a hardware configuration is loaded in the circuit to only deliver clock toward functions relevant to the target application.

IMEC also performed top level layout integrating digital netlist and analog macros, performing DRC to check for compliance to particular radiation hardening rules and finally the interface with UMC foundry.

ICsense has designed a large set of analog IP blocks which were included on the die and successfully tested to reach targeted performances.

A. DPC architecture

Figure 1 depicts the DPC internal architecture. Intentionally, the DPC embeds a very large set of functions. As compared to a µC from the industrial world this may be overkill. However, the economics of space components is very much different. Production volumes are very low as compared to consumer or industrial markets. Hence the silicon area accounts for a very small amount in the total cost breakdown of such a project. The circuit was therefore equipped with so many features, that it is nearly impossible to find a concrete application using all the available resources at once.

As a drawback, not only silicon area increases with the number of functions but also power consumption. Therefore, prior to firmware execution, the DPC enters a hardware configuration cycle. During this phase, a "hardware configuration" map is loaded from the non-volatile memory that defines which functions should be active (useful for the application) and which functions will be made sleeping (clock gating and full sleep mode of analog blocks). Furthermore, operating frequency can be defined such as to match exactly speed performance and processing power needed for the target application. Using these mechanisms, the DPC power consumption can vary up to a factor 7, from minimalist low

end use cases up to the unrealistic worse case where all functions are used at maximum operating frequency.
It is really important to underline that the DPC is not a "multicore architecture" as named in µprocessors. The DPC- which is OS free- allows to program simply and separately 3 µC that are interconnected through DPRAM(mailboxes).

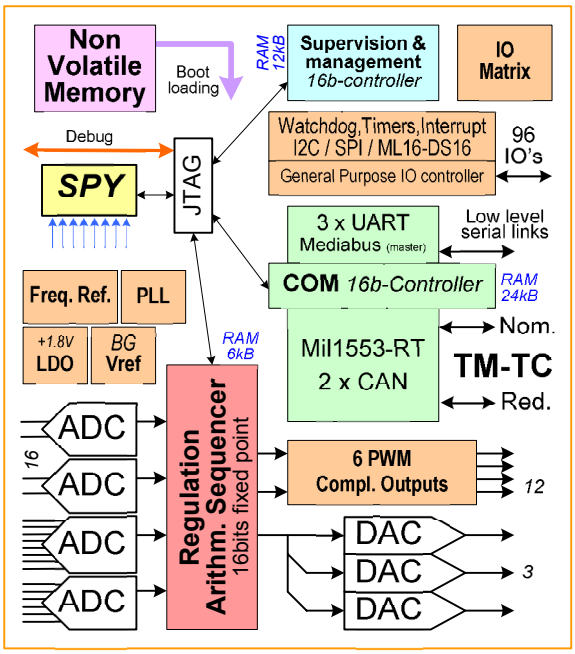


Figure 1: Block Diagram of the DPC

B. *On chip analog blocks*

The DPC is a mixed-mode circuit that contains the following analog blocks:

- Reference voltage and current generation
- Power-management block with LDO's
- 120 MHz frequency reference system (PLL) to provide the clock to the digital part
- 100kHz reference oscillator
- 4 flexible 13 bit , 1MSps ADCs with extensive input muxing capabilities
- 3 12 bit, 3.75 MSps DAC current-mode outputs
- Power-on-reset circuit and under voltage detector
- Rail to rail comparators, PGA (20dB)

Test results of the analog blocks (PLL, ADC, bandgap) can be found in [5]. The blocks design have been explained in more details in [4].

Thanks to careful design with either taking into account Vth shift with total ionising dose or using ELT transistors at specific positions of the analog design & the ICsense proprietary, automated SET hardening simulation environment (used to assess and decrease the SET sensitivity of the analog IP) the chip turned out to first time right in being radiation hardened.

C. *Digital processing*

Processing is based on several instances of the OpenMSP430 fixed-point 16bits CPU core. This processor features the instruction set of the PDP11 (1970) from Digital Equipment Corp. The openMSP430 [0] is a synthesizable 16bit microcontroller core written in Verilog. It can execute the code generated by any MSP430 tool-chain in a near cycle accurate way. To fasten the execution, the CPU is equipped with one hardware 32 bits MACC function and one integer divide unit.

On one hand, digital control is offering new possibilities in driving smarter and more efficient systems. On the other hand connectivity is being more and more present in all applications. In order to avoid searching for complex and touchy compromises between robust loop control and communications or host functionality the architecture offers one CPU per task, as presented on figure 1

For communications to the outside world, the CPU has several hard wired units: 3 x UART, 2 x CAN bus and a MIL-1553b remote terminal function.

Another CPU instance (the "RAS") is intended to execute a configurable and repetitive sequence of basic mathematical or logic instructions within a short cycle. This sequence can be programmed so that any mathematical expression typical of regulation scheme is realized: structures such as Proportional, Integral and Derivate (PID). This sequence can also be programmed to acquire and post-process multiple sensors or pre-process signals before being generated to hardware signals.

Finally one CPU is available to perform all local (host) supervision & management functions.

The highly flexible hardware unit "USI" (Universal synchronous Serial Interface) is able to drive with quite various timing requirements the following communication protocols: SPI, I2C, ML16-DS16, serial in-parallel-out IO extenders.

Figure 2: The DPC ASIC

D. *DPC status*

The development of the DPC was a long story that was initiated back in 2008 with a relatively long definition process investigating many applications needs and defining the requirements for future product generations of satellite equipments using micro-controller technology.
Started in 2012 in the frame of an ESA Artes 5.2 contract, the main development of the Digital Programmable Controller DPC has reached major milestones in 2015 : The ASIC successfully passed the analog characterization and the radiation tests covering heavy ions, protons, and Total

Ionisation Dose tests, allowing to proceed with the formal qualification process.

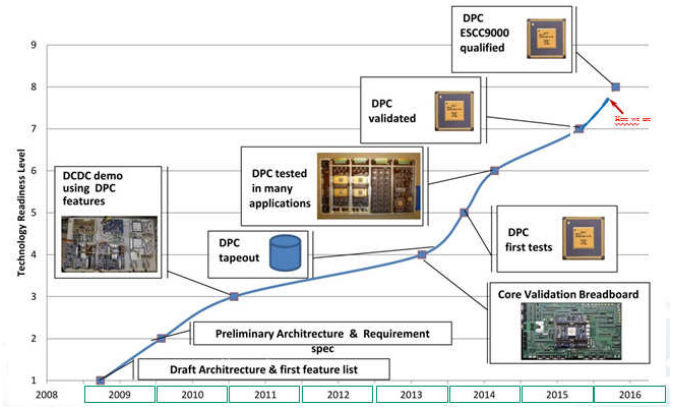


Figure 3: The DPC ASIC TRL maturation timeline

Intensive tests plans were successfully passed in order to validate the DPC performances under extreme temperatures and under radiation environment. The formal qualification for space use process (in the frame of an ESA Artes 3-4 contract) is under completion and first space grade 1 devices are in production.

Up to now, more than 400 DPC ASICs have already been produced for test, evaluation, supply chain validation and qualification purposes.

II. Using the DPC

A. *DPC Reference Kit: hardware*

In order to support the DPC dissemination, a DPC reference kit (DRK) has been built. This board allows the designer to takeover the DPC features and to start programming in a convenient and friendly environment.

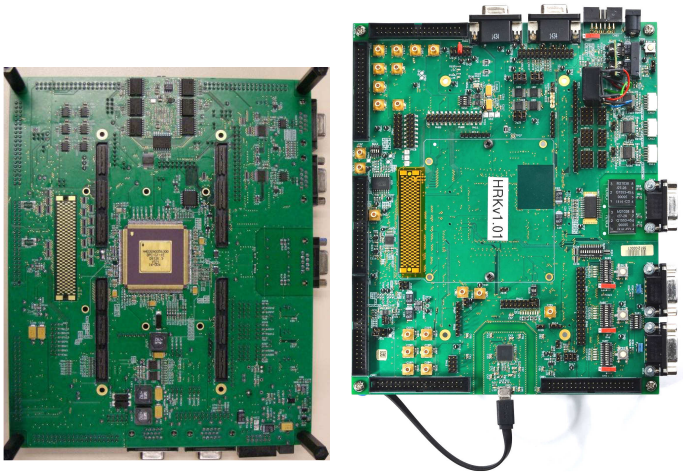


Figure 4: The DPC user Reference Kit hardware

The board is a very rich self-contained prototyping tool (i.e. no other devices needed than a USB plug on the SW development PC). It contains quite large set of analog peripherals together with classical interfaces used in space applications such as mil-1553, CAN, RS4xx … The USB to JTAG bridge allow a direct connection to a USB port of the software development PC. Buffers are foreseen at the output of the PWM generators and at output of the DAC to drive directly strong load connected to the DPC.

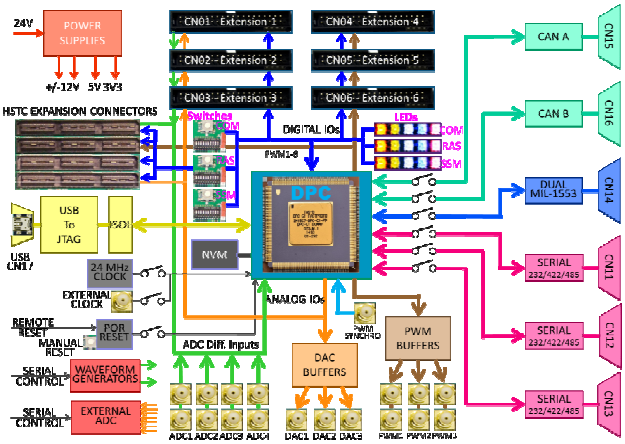


Figure 5: Content of the Dpc evaluation board

B. *DPC Reference Kit: Software suite*

The DRK is made available with a SW development toolkit including compiler , debugger, boot loader, … as listed here below in the table.

Tool Name	Function
msp-gcc	Open source tools for MSP-430, including: • compiler: msp430-gcc • Linker: msp430-ld • Object dumper: msp-objdump • Debuggers: msp430-gdb • Instruction simulalor: msp-debug • Size analysis: msp430-size
dpc-minidebug	Hardware-oriented graphical interface tool enabling simple interaction with the DPC openMSP430 cores. Allows examining and patching registers and memory, setting breakpoints, halt, run and step by step execution.
dpc-gdbproxy	Provides the proxy function for GDB. Replaces the msp430-gdbproxy provided by the mspgcc toolchain.
dpc-pkt	Transforms .elf file in a format compliant to the packet definition.
dpc-programmer	NVM programmer tool and global loader. Writes hardware configuration and program packets in the NVM or loads them directly in the DPC and cores memory through the boot manager.
dpc-configuration	Hardware configuration packets editor.
dpc-crc16	Utility to compute and check the CRC on hardware configuration and programming packets.
Mspdebug	Used in DPC as a MSP430 simulator.

Figure 6: Content of the DPC SW development suite

C. *DPC plugin module: Flight models*

After prototyping, the designer works comes to flight model design. A building block has been developed and is proposed for quick & easy integration of the DPC into equipment. This makes designer life easy as the DPC comes in the form of a mezzanine board that simply needs to the plugged onto the main PCB of new applications. The designer can focus on the main news parts of its system and can rely on a pre-validated & space qualified control module. In term of design effort, it saves therefore the effort of creating an electrical design and tricky layout of analog parts of the DPC and its peripherals and it seriously reduces risks.

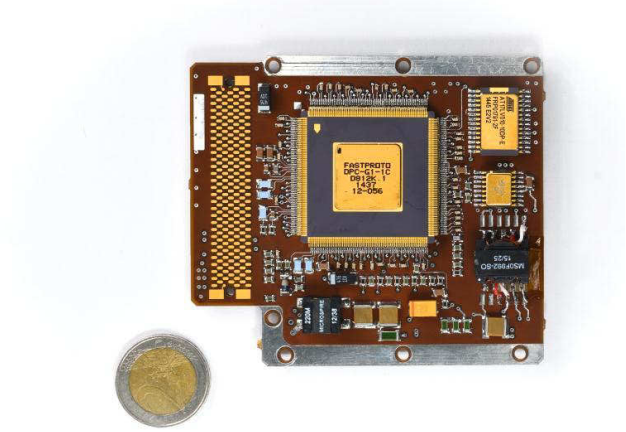


Figure 7: The DPC plugin module

Next to the controller, the DPM (DPC Plugin Module) contains (See figure 8) a 28V dc-dc power supply together with a latching current limiter such that it allows a fail-safe direct connection to an LEO unregulated bus. The board comes also with a dual CAN driver interface to address nominal & redundant communication bus that may for example be used as a backplane data bus [9] into a RTU.

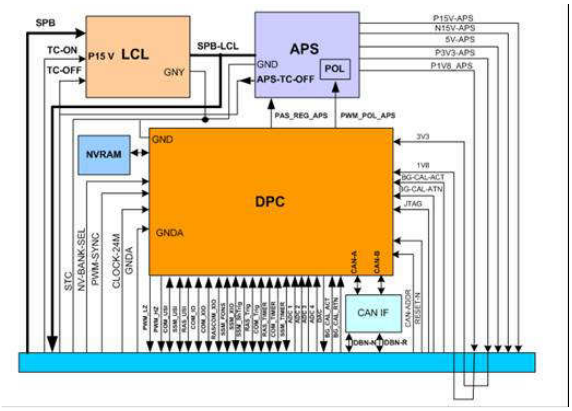


Figure 8: The DPC plugin module architecture

This modularity also simplifies the firmware development process & firmware pre-validation that pay take place at DPM level (without) the main application board. Finally a standardized controller board makes teaming agreements between different companies a much easier job, as each party can focus on its sub-module & associated functions without having to take care of the backplane interface and control.

III. USE CASE EXAMPLES

A. *Avionics*

In parallel with the DPC ASIC, Thales Alenia Space has developed a new generation of "high power" avionic equipment intended to be at the heart of the Spacebus NEO solution, the SDIU MK2 [8].

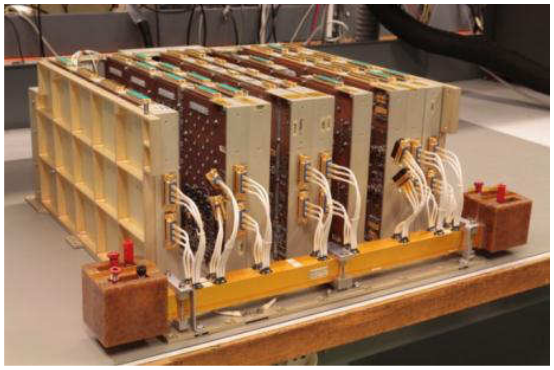


Figure 9: High power avionics using DPC

Thanks to the intrinsic versatility and flexibility of the DPC, the controller module was implemented with each of the different boards of the SDIU, covering a wide range of applications :

- Interface to the on board computer (external 1553) & data relay from/to the back plane bus. via CAN bus. All CAN communications being performed by DPC's.
- Full step motor drive is mainly for the positioning of the steerable telecom antennas, but the same module is able to cover both that functionality
- Distribution of power to platform units,
- Distribution and control of heaters
- Interfacing with the 4 reaction wheels on the satellite.
- Command and control of all of the elements of the chemical propulsion: valves
- Micro Step solar Array Drive: command and control of the solar array deployment and the solar array mechanism motor driving in micro-step mode.
- Monitoring of Li-Ion cell and battery voltages, and command and control of cell bypass and cell balancing elements.

All these functions are distributed over several boards such that there are no 2 identical boards: hence 7 different application software have been developed to perform these functions. This is a major breakthrough as the function was implemented in previous generation of the product using 6 different specialized ASICs.

The DPC ASIC is currently used in the new Thales Alenia Space RTU avionics product range, consistent with SAVOIR roadmap.

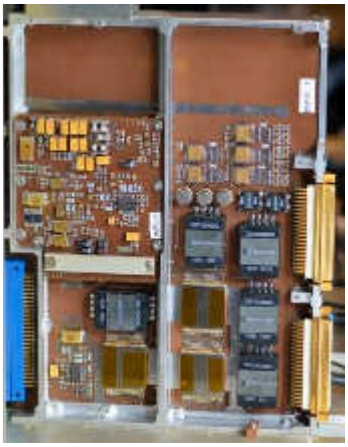


Figure 10: RTU board with the plugin module @ center left

B. Gyroscope acquisition & processing (ONERA)[10]

ONERA has been developing vibrating MEMS inertial sensors for various applications. The VIA cell (Vibrating Beam Accelerometer family) is already in use in the French civil and defence industry. The VIG cell (Coriolis Vibrating Gyroscope family) has been proposed for space applications, in the frame of low cost assistance gyroscope associated with star trackers on satellite platforms : detumbling, slowing down satellite rotation to allow star tracker acquisition, but also safe mode, short term navigation, with higher performances.

Electronic architecture of the gyroscope has been mapped on the DPC cores and peripherals, and requirements set in terms of A/D D/A converters, voltages, CPU usage, and communication with host. The required digital signal processing functions perfectly match the intentional asymmetric core design of the DPC, and all three cores are in use in the application. The program memory is tiny for each core (4K, 8K, 16K), but keeping an eye on assembler generated by the compiler allows the programmer to write clean yet efficient code.

The performance of several functions of the DPC have been evaluated in real conditions, such as ADC resolution. the word length of a single acquisition is 13 bits; when measuring a constant voltage, the ADC resolution is 0.1 lsb after averaging, which is equivalent to 16 bits at 10 ms, limited by 1/f noise. But when measuring a modulated signal on a carrier, the 1/f noise disappears and the resolution is 0.0005 lsb at 100 s (corner frequency is about 0.1 Hz), which is equivalent to 23 bits. Therefore we conclude on the use of the DPC for metrology applications

This work [10] has been funded by CNES, with special support of Thales Alenia Space Belgium.

C. Robotic arm motor control: (DLR

The DLR Institute of Robotics and Mechatronics is going to develop a new multi-sensorial robotic arm with seven joints for space applications like On-Orbit-Servicing. Each joint of this robot shall consist of a Force-Torque-Sensor, an absolute position sensor for the drive side and a motor commutation sensor for the used BLDC motor. All these sensor data are processed at each joint with the control loop frequency of 1 kHz. In addition, the motor commutation shall be performed at a rate of 40 kHz. Therefore two processors are used to decouple the basic tasks: Joint Control and Motor Control. The DPC from Thales Alenia Space Belgium is under prototyping as candidate for performing the Motor Control task.

The new multi-sensorial robotic arm CAESAR (Compliant Assistance and Exploration Space-Robot) shall consist of seven joints in an alternating rotational and bending arrangement. A CAD rendering of the intended design with an applied gripper at the tool center point is shown in figure 11.

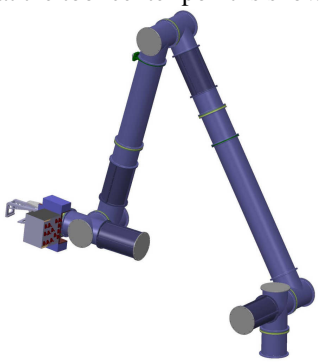


Figure 11: Multi-sensorial robotic arm CAESAR

Contrary to the preceding ROKVISS experiment [11] in which standard automotive part where used and performed well in outer space for more than 5 years, CAESAR shall be capable to meet multiples mission requirements. Additionally, since the design and manufacturing of the ROKVISS joints is now several years old, some of the used components are obsolete. Together with changed mission parameters, the envisaged improvements and changes in the design it is necessary to redesign the electronics of the robotic arm.

The approach for CAESAR is to use space qualified components where possible. If space qualified components are not available with the same functionality we will use military or automotive rated components which are radiation tested and if necessary protected against latch up. This approach is the only feasible way to build complex joints with the same functionality as the ROKVISS joints.

The main subsystems of each joint are:

- local power supply with latch-up protection
- motor power inverter
- communication and control unit
- joint torque and position sensor for each joint
- motor commutation sensor

The motor control of the BLDC motor is based on a current control algorithm and a Space-Vector-Modulation for the current set-point vector. The whole current control loop (incl. the Space-Vector-Modulation) must be performed at a rate of

40 kHz in order to enable a motor speed of 50000 electrical revolutions per minute.
The base of the current control loop are the measured current values of all three motor phases and the inverter voltage which must be sampled in parallel at one step to minimize the phase errors. In addition, some communication tasks and housekeeping data monitoring at a lower frequency must be performed, too.

For this challenging task, the DPC from Thales Alenia Space has all required peripherals on chip. DLR is right now evaluating the DPC in this robotic arm context.

IV. Analog IP transfer

In the frame of this DPC development, several analog function have been implemented in the DPC. These are available in the form of IP blocks [4] & [12].

As an example, Thales Alenia Space UK is currently running a ASIC development program based on the IMEC DARE+ library. That development will leverage on the DPC to reduce the risk involved with mixed mode design by integrating ADC, PLL & voltage reference from the DPC program.

The ESA SSDP development program will also re-use analog IP from the DPC.

V. Conclusions

Thanks to an efficient cooperation with IMEC, ICsense and ESA, Thales Alenia Space Belgium has built an innovative highly integrated mixed signals controller.

Its high level of configurability and its large set of communication interfaces allow the usage of the Digital Programmable Controller (DPC) in a broad range of applications such as scientific payload control, motors, actuators, battery management, power management … wherever a decentralized control makes the overall solution more efficient.

The outcome of the project is not only as a space qualified component but mainly a set of tools making end users life easier and reducing risks: a Reference Kit for rapid prototyping and a Plugin Module for quick integration into new designs. The software development toolkit includes all standard tools such as compiler , debugger, boot loader, …

These tools have been already extensively be used by Thales Alenia Space as “local” customer but also transferred to alpha customers: Onera & DLR. The DPC is now ready for large deployment into any space application.

VI. Acknowledgements

The authors would like to warmly thank:

ESA project team from both µE and power divisions for their great support and many advices in conducting this project.

Mr. Olivier Girard who spent hours in the design of the openMSP430 core and has finally posted it in free BSD licence [1] available to anyone’s usage on internet (http://opencores.org/project,openmsp430).

M. Durvaux for its clever guidance in the selection of this processor, the top-level chip architecture and the associated patent [2].

ONERA and specially Dr Jean Guerard for the feedback he provided as “customer using the DPC” that helped us to improve the efficiency of the DPC development tools.

Mr. Hans Juergen Sedlmayr from DLR for his kind support in publishing this preliminary information on testing the DPC in a robotic context.

VII. REFERENCES

[1] OpenMSP430 technical data by Olivier Girard http://opencores.org/project,openmsp430

[2] “Device with power electronics control circuits” European Patent EP20100171077 (2012-02-15*)* *M. Fossion M. Durvaux*

[3] “ Radiation Hardened Mixed-signal IP with DARE technology” G. Thys, S. Redant, E. Geukens, Y. Geerts, M. Fossion, M. Melotte, in Proc AMICSA 2012.

[4] Bram de Muer ICsense “Rad-hard, high-performance analog and high-voltage IP in 0.18um CMOS (DARE)” ESA IP-cores day Sept 2013

[5] "A mix-signal radhard micro-controller: DPC", *Marc Fossion Alain Van Esbeen, Richard Jansen, Eldert Geukens, Steven Redant, Claudio Monteleone, Yves Geerts,* June 2014 AMICSA @ CERN Zurich

[6] Introduction to the DARE platforms Mr. Steven Redant IMEC @ DARE User Day ESTEC 8 December 2014

[7] “Digital Programmable Controller – DPC” *M.Fossion & A. Van Esbeen* @ CCT CNES Nov. 2014

[8] “DPC application in Avionics / RTU” A. Nairn & Ch. Maillard @ 9th ESA Workshop on Avionics, Data, Control and Software Systems ADCSS2015

[9] "CAN Backplanes and the DPC "*Van Humbeeck Thierry & Lizin Gilbert*@ CAN in Space ESA workshop, 10 March 2016

[10] “MEMS Gyroscope Demonstration for Space Application, using a DPC” Dr. Jean GUERARD *(ONERA) @ AMICSA 2016*

[11] Verification of Advanced Light Weight Robotic Joints and Tele-Presence Concepts for Future Space Mission *K. Landzettel and A. Albu-Schaffer and B. Brunner and A. Beyer and E. Kramer and C. Preusche and D. Reintsema and B.M. Steinmetz and H.J. Sedlmayr and G. Hirzinger* 9th ESA Workshop on Advanced Space Technologies for Robotics and Automation ASTRA 2006

[12] “Radiation hardened high-voltage and mixed-signal IP with DARE technology” Eldert Geukens, Jan Dielens, Bram De Muer, Geert Thys, Steven Redant(1) *@ AMICSA 2016*

MEMS gyroscope demonstration for space application, using a DPC

J. Guérard[a], M. Larroque[a], G. Lizin[b], L. Verstraeten[b], G. Delavoipière[c]

[a]ONERA, 92322 Châtillon, France
[b]Thales Alenia Space, 6032 Charleroi, Belgium
[c]CNES, 31400 Toulouse, France

jean.guerard@onera.fr

Abstract

This paper reports the prototyping and performance evaluation of a MEMS Coriolis Vibrating Gyroscope developed by ONERA, connected to the Digital Programmable Controller (DPC) delivered by Thales-Belgium (TAS-B), in a gyroscope application.

The electronic architecture of the gyroscope has been mapped on the DPC cores and peripherals, and main functions developed and characterized. First a Direct Digital Synthesizer (DDS) has been implemented with a resolution better than 0.001 Hz, in order to accurately drive at resonance the high quality factor vibrating cell. A pair of ADC are operated synchronously with the synthesizer to acquire the amplitude and phase of Drive and Sense signals coming out of the vibrating cell, that are digitally demodulated in real time (over 200 kHz) using the hardware Multiplier/Accumulator of the DPC, and deliver in-phase and quadrature components to the second DPC core.

Further processing is then performed, such as an embedded PLL for the resonator, and a decimation filter to scale down the raw data stream to the sampling rate configured by the user, which takes place in a standard desktop computer running the demonstration OBC software. The gyroscope data frames are composed and transmitted by the third core on a serial port.

I. MEMS GYROSCOPES FOR SPACE APPLICATION

The main sensor of an Attitude and Orbit Control System (AOCS) in a satellite platform is a star tracker. These optical instruments are very accurate on a long term since they deliver absolute angles of the satellite reference frame with respect to far stars (the *attitude* of the satellite). However, in some cases, an inertial gyroscope (blind) may complement the star tracker :

- At the beginning of flight operations (orbit insertion), detumbling of the satellite in order to allow star trackers to acquire stellar fields;
- During operations, when star trackers are temporarily dazzled by Moon or Sun, or shadowed by Earth;
- Other safe modes, when star trackers are unavailable.

Low to Medium performance Angular Rate sensors (gyroscopes) are used for such assistance. Several technologies are available, such as Fibre Optic Gyroscopes (FOG) and Ring Laser Gyroscopes (RLG), both based on Sagnac effect, or Hemispherical Resonating Gyroscopes (HRG) based on Coriolis effect.

Performance improvements of MEMS CVG, another family based on Coriolis effect, associated with their native advantages in small size and low power consumption, led to their progressive introduction into markets dominated by other technologies. The replacement of low to medium performance gyros by MEMS CVG is today foreseen in a growing number of systems [1] [3], including space applications, from micro satellites, obviously, to medium size or even geostationary platforms [3].

II. CORIOLIS VIBRATING GYROSCOPE

The CVG sensor head is a mechanical resonator vibrating at resonance using the In-plane Drive mode (Figure 1). When the gyroscope is exposed to an angular rate in the z-direction, the Coriolis acceleration ($\overrightarrow{A_c} = 2\vec{\Omega} \wedge \vec{V}$) initiates the Out-of-plane Sense mode. Although it is forced to the drive pulsation ω_x, (Sense mode resonance pulsation is ω_y), the amplitude Y of this vibration is significant (ω_x and ω_y are close to one another), and proportional to the input angular rate Ω. This architecture requires very little subsystems and is known as the Open Loop mode.

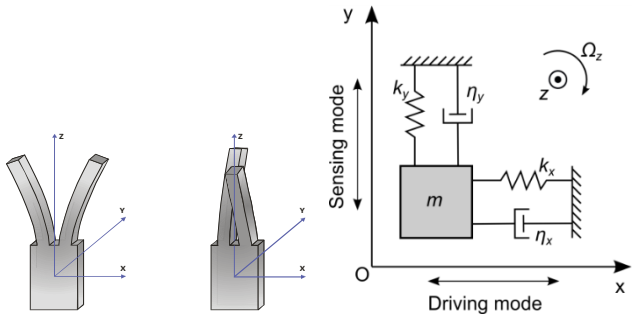


Figure 1 : Tuning fork gyroscope principle (left), showing Drive and Sense modes. Equivalent mechanical system (right), with two degrees of freedom.

Other more sophisticated modes are available, for higher performance, as *force rebalance* or *closed loop* (controlled sense mode), and *whole angle* (no difference between drive and sense, isotropic vibration) [4].

ONERA has been developing vibrating MEMS inertial sensors for various applications. The VIA cell (Vibrating Beam Accelerometer family) is already in use in the French civil and defence industry. The VIG cell (Coriolis Vibrating Gyroscope family) has been proposed for low cost assistance gyroscope in the frame of the NEOSAT program (Figure 2).

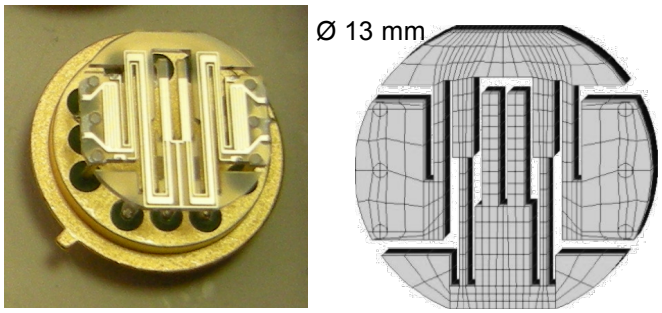


Figure 2 : VIG quartz cell mounted on socket (left). Mechanical model for Finite Element simulations (right).

During previous activities several aspects of the VIG have been investigated, in the objective of a future qualification. The gyroscope quartz cells endured radiations successfully up to geostationary dose (100 krad), and could also withstand launcher vibrations. Shocks were also acceptable with intercalated passive damping layer. Concerning electronics, the design and realization of an ASIC was initiated, but prohibitive cost prevented from further development. Nevertheless it was assessed that the electronic architecture of the ONERA gyroscope was compatible with the Digital Programmable Controller (DPC) developed by TAS-B. Once the chip was released last year, the opportunity to build a demonstrator was found with CNES, the French space agency.

III. ONERA MEMS CVG ARCHITECTURE

The piezoelectric material of the resonator allows both action and detection, using respectively the reverse (voltage to force) and direct (deformation to charges) piezoelectric effects (n_x on Figure 3). Electric charges are collected by gold electrodes and converted to voltage by charge amplifiers and demodulated. The Drive in-phase signal (Φ) is controlled down to zero by the Phase Locked Loop (PLL), to ensure Drive resonance at all time. The Drive quadrature signal (Q) is optionally used in an independent Automatic Gain Correction (ACG) loop. The "cos θ" and "sin θ" coupling terms take into account little errors of cell realization, in the etching process, whose overall effect is a rotation of mechanical vibration axes with respect to the electrode frame. A small amount of Drive motion may thus be coupled into Sense signal, which is known as *quadrature error* [5].

At least a passive re-injection of Drive voltage (V_D) through a tuned impedance is necessary to avoid voltage saturation at Sense amplifier level, before processing. Quadrature residuals are then efficiently rejected by the synchronous demodulation.

Apart from charge amplifiers, which are simply built on discrete operational amplifiers, all other functions are digital, including analog-to-digital converters.

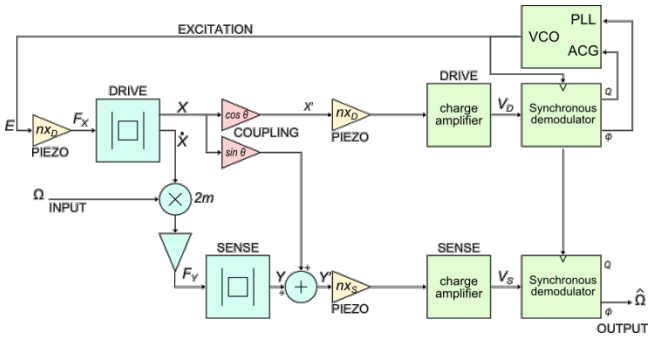


Figure 3 : Coriolis gyroscope architecture. Blue : mechanical resonators; yellow : action and detection transduction; green : electronics

IV. DPC INSIDE

The DPC is an innovative highly integrated mixed signals controller. It targets several applications mostly related to sensing and power conditioning. This includes power conversion (DC-DC, AC-DC, DC-AC, AC-AC), motor control (DC, stepper motors, AC with up to 6 phases), multi-standard communication between several clients and protocol translation, and remote sensors [6].

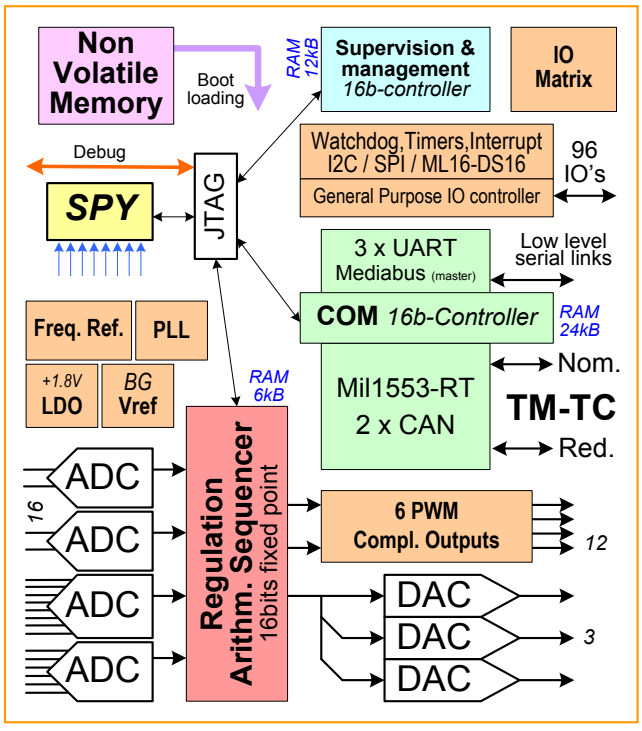


Figure 4 : DPC architecture. Three specialised cores can run simultaneously : RAS, SSM, and COM. The fourth core, SPY, is intended for debug.

The microprocessor architecture, MSP 430, may be considered “old fashioned”, but actually answers two issues :

- After 10 years development, 10 years production, and 15 years in orbit, compiler tools shall be still available to upload new software; only an open source architecture can guarantee this.
- Modern 32 bits architectures are versatile and attractive, but also RAM consuming, and features like memory management for multi-task OS are out of scope for the targeted applications. Here a 16 bits architecture was a good trade-off

Besides, the architecture is not orthogonal and the three cores are actually dedicated to their peripherals.

Knowing that, electronic architecture of the gyroscope has been mapped on the DPC cores and peripherals, and requirements set in terms of A/D D/A converters, voltages, CPU usage, and communication with host.

At the lowest level, but also at the highest sampling rate, the sinusoidal excitation signal is calculated by the RAS core and output to the DAC. Two channels are used, to form a differential pair, avoiding an external inverter.

The quartz resonator delivers two signals, in response to the excitation above : drive and sense. They need to be sampled and acquired with strictly synchronised ADC. This is possible in the DPC, where ADC3 and ADC4 (differential voltage input) share a common sequencer, clocked by RAS. As all signals are carried by the resonance frequency, the synchronous demodulation is also performed by RAS.

At higher level, the SSM core is in charge of the decimation, from the sequencer frequency (higher than the sensor head resonance), down to the desired instrument sampling rate. SSM is also in charge of various long term control loops, the most important being the PLL to keep the mechanical head resonating. Processing is more complex, but at lower rate.

When decimation occurs, the SSM data are transferred to the COM core, which will build the data frame to be sent to the OBC on a digital link. Various UART protocols are supported by the DPC, as well as CAN and 1553 buses. COM will also receive and decode commands from OBC.

V. Frequency Synthesis

The first critical function is the frequency synthesizer, based on Direct Digital Synthesis (DDS). Such a synthesizer makes use of a phase accumulator, delivering the instantaneous phase of the desired signal by adding at each sampling time a phase increment. The phase then enters a Look Up Table (LUT) to get the output waveform, generally a sine wave, which finally feeds the DAC. If NA is the binary word size of the phase accumulator (so that 2^{NA} is equivalent to 2π), F_{RAS} the interrupt rate of the RAS core, and W the phase increment, then the output frequency is

$$F = W \frac{F_{RAS}}{2^{NA}} \qquad (1)$$

The best code allowed the RAS job to complete in 5.6 μs, which means a rate of 180 kHz. Coupled with a phase increment word size of 32 bits, the resolution of the synthesizer was 40 μHz, which looks extremely accurate but is actually only acceptable compared to the resonance bandwidth of the quartz cell. The quality factor is indeed around 200 000, so that the resonance bandwidth is 45 mHz, and the synthesizer frequency step shall be small with respect to this value.

When sampling the desired frequency at a fixed rate, the signal is not rigorously periodic, and aliasing occurs : spectral lines of the sampling frequency and multiples are folded back close to the target frequency.

We used a modified version of the DDS, where the number of steps per signal period is fixed integer and the sampling frequency is tuned to match the target. This is done in the DPC by modulating the duration of the RAS main sequencer, which is set by division of the internal 120 MHz reference clock. The RAS cycle can now run up to 220 kHz, leaving 12 samples per period at 17 kHz, the vibrating cell Drive resonance. A 32 bits word is used for the RAS cycle, so that the frequency synthesis resolution is now 85 μHz at RAS level, which means 85 / 12 ≈ 7 μHz on the target frequency.

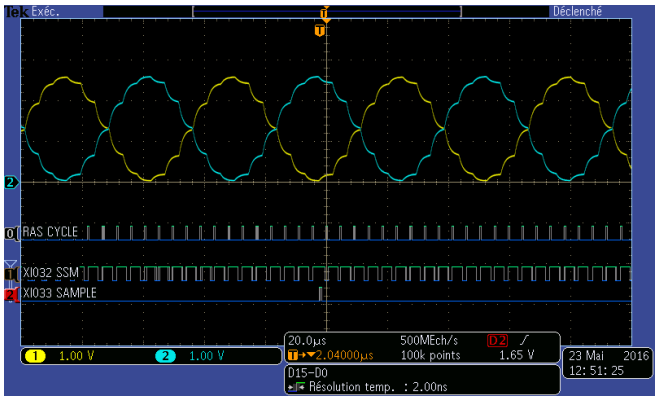


Figure 5 : Sine waveform generated by RAS core, 12 symmetric samples per period, on DAC1 and DAC2. F_{RAS} = 220 kHz max.

VI. Digital Demodulation

Both Drive and Sense signals need to be acquired simultaneously and synchronously. This was the main expected feature of the DPC for the gyroscope architecture : two parallel and identical ADC channels, together with a hardware Multiply/Accumulate unit (MACC).

Let x_k be a sine signal composed of an In-Phase term XP and a Quadrature term XQ, and sampled at the rate Ts ($\theta = 2\pi.F.Ts$) :

$$x_k = XP \cos k\theta + XQ \sin k\theta \qquad (2)$$

The demodulation of x consists in multiplying it with $\cos k\theta$ and accumulate, to get the Phase term, and with $\sin k\theta$ and accumulate, to get the Quadrature term.

$$\widehat{XP} = \frac{2}{N}\sum_{k=0}^{N-1} x_k \cos k\theta$$
$$= XP + \underbrace{\frac{XP}{2N}\sum_{k=0}^{N-1}\cos 2k\theta}_{\Sigma C} + \underbrace{\frac{XQ}{2N}\sum_{k=0}^{N-1}\cos k\theta \sin k\theta}_{\Sigma CS} \quad (3)$$

ΣC and ΣCS will naturally cancel when $N\theta$ is a multiple of 2π (an integer number of periods is covered). For this reason, when the decimation occurs, the SSM just waits for the next end of period to complete the sum, so that it is performed on the expected integer number of complete periods, and the estimators of XP and XQ are accurate. The phase jitter of the instrument sampling time due to this fraction of carrier period is negligible, with respect to the data frame transmission for example.

The DPC designers implemented a MACC function in the RAS on purpose (a second one in the SSM), but unfortunately, the accumulator can only remember one sum; here four accumulators are needed for Drive/Sense, Phase/Quadrature terms. As reloading the accumulator and saving the result each time would have wasted the code performance, the running sums are performed by software. Actually an addition is performed in one CPU cycle, the same as just moving the data.

To keep the high throughput, RAS and SSM have been pipelined (Figure 6) :

- Data transfer from RAS to SSM using mail box;
- Synchronisation using trigger signals between cores (RAS is master)

Therefore the CPU power is doubled for the main operation (low level, high data rate). The resulting data rate is 1.3 Msps (3 acquisition slots per sampling period, 2 channels), the data processing rate is 880 kMACC/s and the inter CPU data flow is 35 Mbit/s.

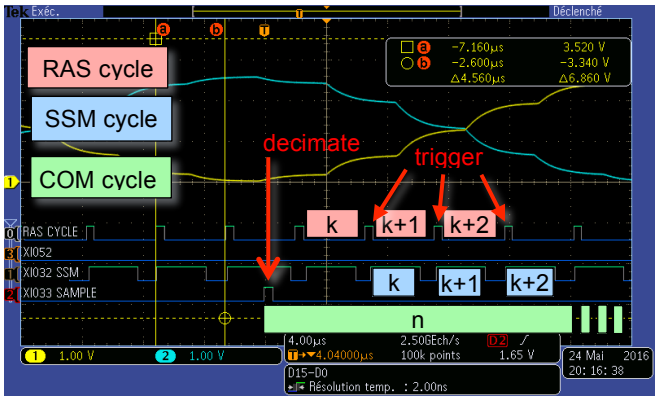


Figure 6 : Pipeline between RAS and SSM. Sampling interval is 4.56 μs (220 kHz). End of RAS activity triggers SSM.

At the decimation rate (~30 Hz for the instrument output), a snapshot of the demodulation accumulators is transferred from SSM to COM. The latter performs data frame formatting for transfer to OBC, via the selected interface. In this study, an RS232 UART was implemented, but CAN, or 1553 are also available.

VII. EXPERIMENTS

A. *Development board*

The board is a DPC Reference Kit (DRK), designed and distributed by TAS-B. . It consists in a true qualified DPC, mounted on an evaluation board with power supplies, I/O connectors and programmer access through JTAG. All I/O signals in the DPC, logic and analog, are accessible on the board connectors (Figure 7, Figure 10).

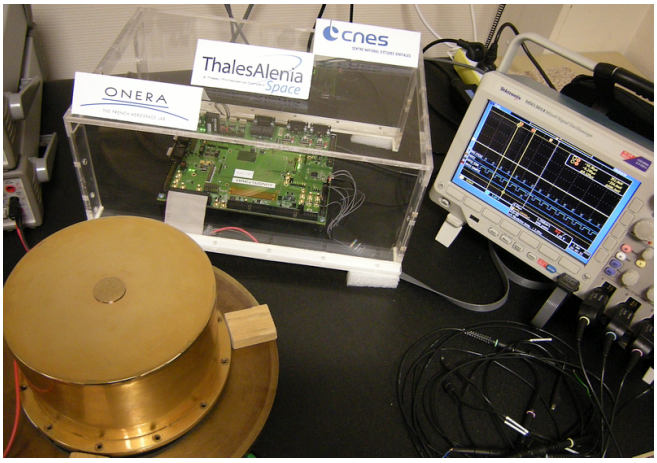


Figure 7 : DRK (under plexiglass case). Digital signals as well as analog signals on the scope are available. The golden cylinder on the lower left is a vacuum chamber for the gyroscope.

B. *Software tools*

The DRK comes together with software tools (compiler, debugger, configuration manager), offering the developer a complete toolchain from C source code to oscilloscope view of signals. Two desktop computers are in place to manage the DRK (Figure 8) :

- The PC-DPC contains software tools for application development : Eclipse based IDE, gnu compilers, JTAG and debug tools;
- The PC-OBC is dedicated to the user application. When embedded codes for all cores are finalized and uploaded in DRK, only PC-OBC is in use.

The PC-OBC should be representative of an on-board computer. For this demonstrator, PC-OBC is able to send commands for parameters, using a basic ASCII format :

S xxxx ↵	set the decimation rate
L xxxx ↵	close / open the PLL
F xxxxxxxx ↵	set synthesizer frequency

Parameters xxxx are written in hexadecimal, which is a good tradeoff between human readability on a terminal and encoding/decoding efficiency in the microcontroller.

The PC-OBC also reads data frames to depacket, plot, analyse and save the gyrometric data. The same

hexadecimal readable ASCII format is used for the frame encoding. Baud rate is not critical and a standard 115200 baud UART can handle the application.

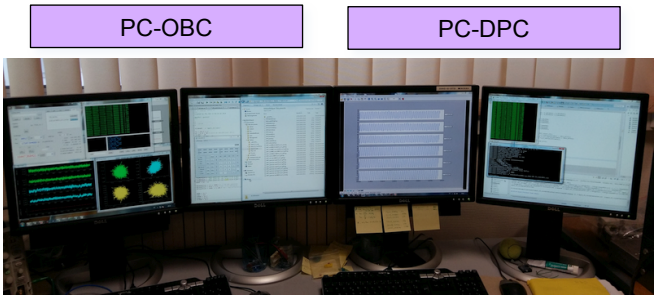


Figure 8 : PC-DPC (embedded software development and debug), and PC-OBC (data collect and line plot).

A graphical user interface has been developed with Python/Qt, so that commands and data can be managed directly from the interface, or scripted in a batch mode.

C. *Gyroscope Demonstration Model*

The VIG quartz cell is mounted on a socket (Figure 2, left), which is then soldered in a copper case. A small pipe allows pumping and offgassing at high temperature, so that the vacuum chamber can be definitely sealed by a pinch-off operation. This is an easy and efficient vacuum encapsulation. The proximity electronics are reduced to front end amplifiers, and are made of operational amplifiers (low noise, low input capacitance). All other functions are in the DPC (Figure 9).

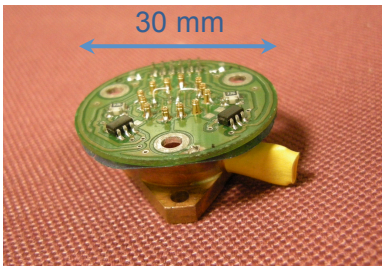


Figure 9 : VIG gyroscope in a copper vacuum package and connected to proximity electronics.

In this Demonstration Model, all analog signals (excitation from DAC and pre-amplified signals to ADC) are connected to the DRK through one of the six ribbon cable available (Figure 10). Obviously this is not an ideal connection and a possible Engineering Model designed for the DPC Plugin Module (DPM) for example, or in this range of size, would be more stable, with shorter wire length, avoiding coupling and stray capacitances.

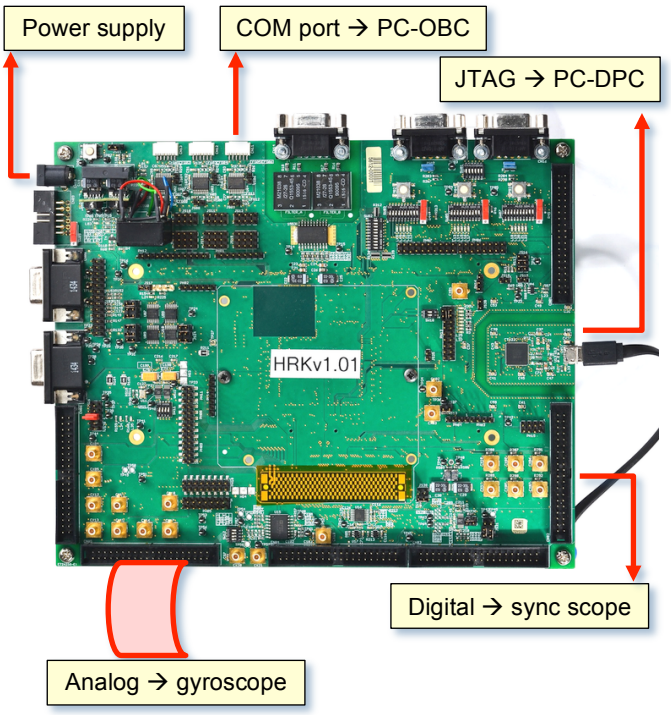


Figure 10 : DRK setup. The upper face is for the DPC Plugin Module (DPM), and the lower face is for a standalone DPC.

One important characteristic of the CVG has to be explained here. Back to Figure 3, the Sense signal, *Y'*, includes Coriolis information as well as a coupling term from the Drive amplitude, which is extensively discussed in the literature [5]. But both are carried by the Drive vibration *X*, amplitude and phase.

$$Y' = \frac{2m\Omega}{\Delta\omega}\dot{X} + \sin\theta \; X \qquad (4)$$

where Ω is the input angular rate, m is the equivalent vibrating mass of the resonator, and $\frac{1}{\Delta\omega}$ is the gain of the Sense transfer function, which is not exactly working at resonance, but $\Delta\omega$ apart. Consequently, dividing Y' by X' (complex division) naturally normalizes the Coriolis detection with respect to Drive fluctuations. No control loop is needed on the Drive amplitude, and PLL stability (the phase of *X*) can be released.

Fortunately, this division occurs only on final samples, after demodulation and decimation, at a low rate, so that it can be handled by the OBC, marking the boundary between low level - simple arithmetic - fast rate operations (inside DPC), and high level - complex arithmetic - low rate post processing (inside OBC). The data frame then transfers Drive Phase, Drive quadrature, Sense Phase, Sense Quadrature to the OBC (Figure 11). Other parameters are for debug : resonant frequency tracking, number of samples in decimation, various multiplexed monitoring values.

The Coriolis signal, result of the division in OBC is plotted on Figure 12. Despite fluctuations of the PLL, that are due to

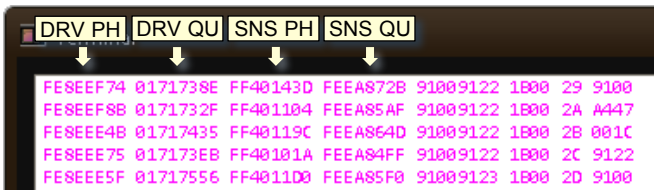


Figure 11 Data frames from DPC to OBC on the UART port (115200 bauds).

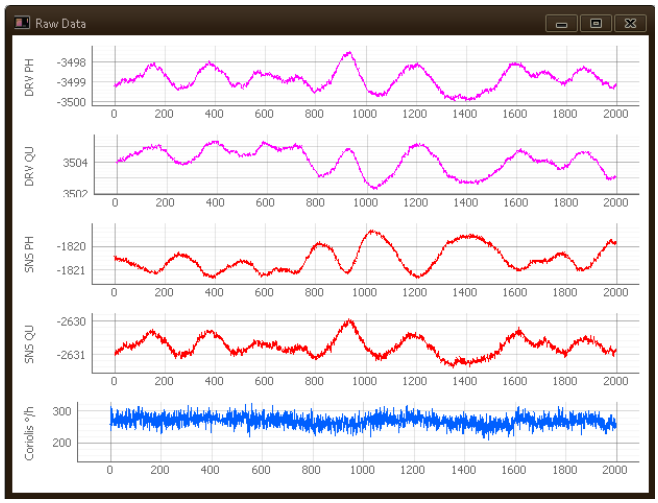


Figure 12 : Drive components (upper), Sense components (middle), and Coriolis output (lower).

D. *Results and performance*

First, the DPC noise floor is measured, connecting ADC3 to the gyroscope pre-amplifier output, but out of resonance, so that only amplifier noise is captured, and ADC4 to ground. Noise spectral density is plotted on Figure 13. The initial resolution of the A/D converters is 13 bits. Thanks to the very high internal sampling rate (~200 kHz), the averaging at the instrument output sampling rate (~30 Hz) is efficient, and thanks to the demodulation, *1/f* noise, or flicker noise, is much reduced. The noise spectral density is better than 1 μV/√Hz for both ADC3 and ADC4, and the long term resolution, after 100 s averaging, is 0.1 μV, while the LSB is 0.3 mV. This is equivalent to a 23 bits conversion. More reasonably speaking, the resolution is 20 bits at 1second.

The internal sampling rate is actually close to the maximum, because the 3 slots available in the RAS cycle are used to acquire data, leading to a raw sampling rate of 600 kHz on each ADC.

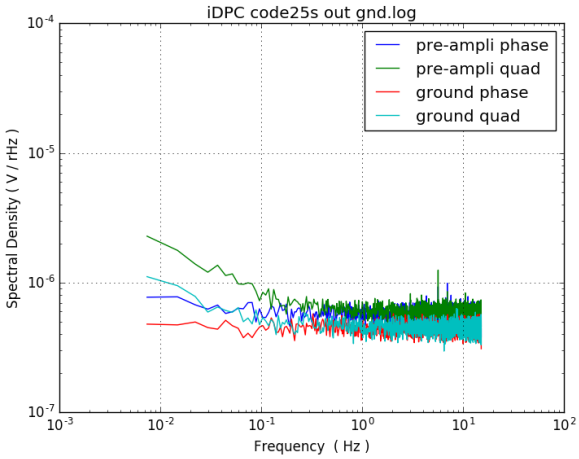


Figure 13 Preliminary characterization of the DPC ADC 3 (pre-amplifier) and ADC4 (ground), for differential voltage measurement.

The performance of a gyroscope is mainly characterized by its Angular Random Walk (ARW). It means the standard deviation of the angle output, integrated from the angular rate, generally after one hour. ARW is extrapolated on the angular rate Allan variance, taking the left asymptote at one hour.

On Figure 14, the black line comes from the previous grounded input, processed with scale factor as if it were the gyroscope signal. It provides DPC noise contribution in this application. The equivalent ARW is 0.01°/√h. Then the blue line is recorded with the pre-amplifier and vibrating cell connected, but away from resonance, so that it is representative of electronics. The equivalent ARW is slightly degraded, 0.03 °/√h, but still satisfactory in the gyroscope application. Finally the system is operated at resonance in the true conditions of the instrument. The ARW is further degraded (red line, up to 0.07 °/√h), yet acceptable; the main disappointment comes from the Allan variance minimum, which is around 15 °/h, and translates to the $1/\sqrt{f}$ slope in the spectral density.

Investigations performed into this degradation revealed that a feature of the DPC may be the cause of the problem. When writing to the DAC, the value is not directly effective on the converter, but is re-sampled by a 3.75 MHz sub-clock of the 120 MHz core clock. While RAS cycle occurrence and sampling times in the ADC are controlled with a resolution of one core clock period (8 ns), the DAC registers are also updated with that precision, but the conversion will be effective after a delay between 1 and 32 clock periods. This causes a small jitter with negligible impact on the out-of-resonance measurement, but with annoying impact at resonance, due to the large amplitudes measured.

When the RAS period is a multiple of 32 core clock periods, then the time of DAC refresh always occurs synchronously with the re-sample sub clock. Now when the RAS period differs from that multiple, DAC refresh time will drift and the resulting excitation signal for the resonator will be modulated.

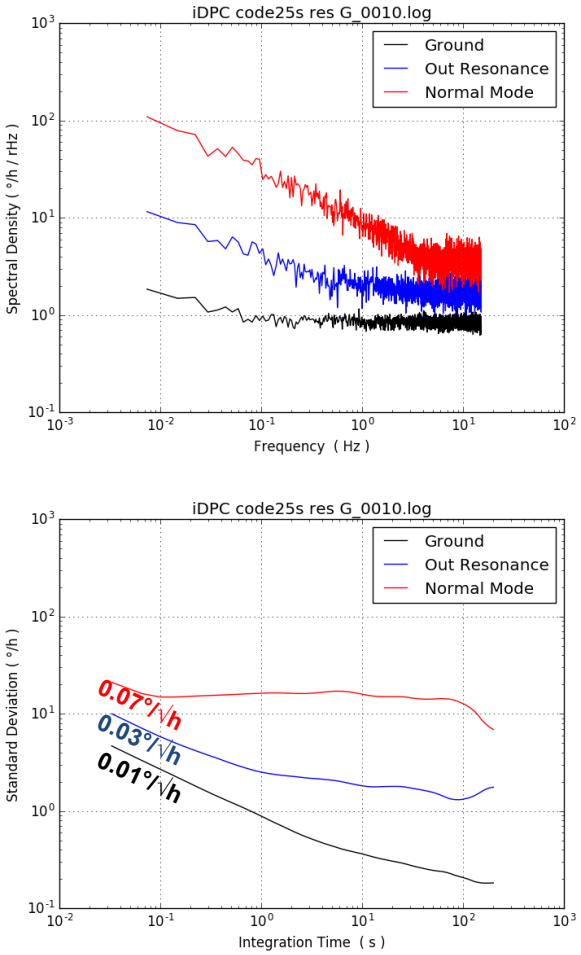


Figure 14 : Gyroscope DM noise performance. The same data are processed for noise spectral density and Allan variance.

This effect is shown on Figure 15. The signal fluctuation can be increased by a factor 10.

Ongoing work is focused on the coherency of RAS cycle period and DAC resample. Workaround can be found, at the expense of synthesizer resolution, but the 7 μHz obtained above can be relaxed thanks to the complex division algorithm.

Besides, the DAC sampling scheme should be revised in version 2 of the DPC ASIC, the best option in our case being a synchronized latch of the DAC with the ADC sequencer.

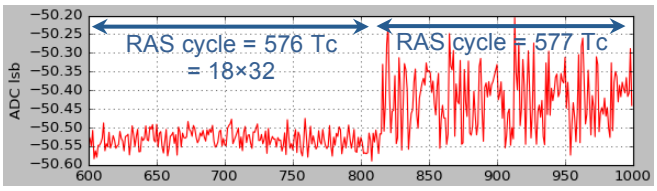


Figure 15 : Effect of DAC re-sampling on one demodulated output.

VIII. CONCLUSION

A gyroscope Demonstrator Model has been built with a DPC as main electronic device connected to the quartz Coriolis Vibrating Gyroscope developed by ONERA, all other components being operational amplifiers. This simplified architecture allows defining a low cost MEMS sensor, targeting applications in the range of assistance to star tracker. It could be included in the star tracker, or integrated in the OBC motherboard.

The DRK allows live power measurement in the DPC. As expected, the current driven is 500 mA on 1.8 V for the digital circuits. Some unused peripherals like 1553 interface and PWM have been disabled. Analog circuits of the DPC require 50 mA on the 3.3 V supply, and external amplifiers require 30 mA. The total power for one gyroscope sensor is 1 W.

The software functions developed for the sensor match the intentional asymmetric core design of the DPC, and all three cores are in use in the application. The program memory is tiny for each core (4K, 8K, 16K), but keeping an eye on assembler generated by the compiler allows the programmer to write clean yet efficient code.

At this time about 30 % of the available program memory is used in the DM, leaving margin for further development (Figure 16).

Figure 16 Percentage of program memory used in each core during development.

Generally speaking, high over-sampling and efficient synchronous demodulation implemented here bring the ADC resolution up to 20 bits, which makes the device interesting for numerous metrology applications, where carriers can be preferred to DC polarisation of sensor heads. The 20 bits performance is obtained in the following conditions:

- Differential pairs to reject common mode parasitic signals;
- Sinusoidal signals and synchronous demodulation to reject bias and flicker noise in amplifiers;
- Renormalisation by division of two parallel channels, to reject reference voltage fluctuations;
- Contiguous decimation synchronised with signal period to preserve averaging efficiency

IX. PERSPECTIVES

The first performance demonstration of the ONERA gyroscope cell in a space architecture design is encouraging, considering the following opportunities of improvement :

- The excitation level of the quartz cell is currently ±1.25V, limited by the DAC range (no cascaded amplifier). It can be increased by a factor 2 or more without damage to the quartz cell, increasing the signal to noise ratio;
- The quadrature term was very important in the generation of quartz cell of the demonstrator. It implies external re-injection of drive into sense to compensate for the $\sin\theta$ term, at least to de-saturate the pre-amplifiers. The next generation cells will have reduced quadrature terms;
- The size of the cell can be increased for free, as long as it remains smaller than the DPC device. An x times larger cell delivers x^2 times more piezoelectric charges.

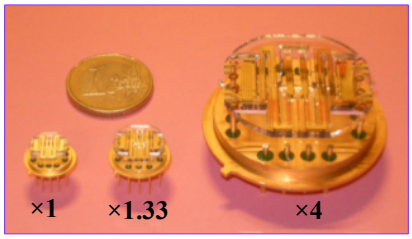


Figure 17 : scaled gyroscope cell for stronger signal. The DM cell is the 1.33 scale.

After this demonstration, ONERA is ready to return the DRK and build an Engineering Model, in an integrated design, so as to perform environment characterisations.

This work has been funded by CNES, with special support of TAS-B.

X. REFERENCES

[1] N. Barbour, “Inertial Navigation Sensors”, NATO report RTO-EN-SET-118, 2011

[2] C. Goodall, S. Carmichael, B. Scannell, “The battle between MEMS and FOGs for precision guidance”, Technical article MS-2432, Analog Devices, 2013

[3] Next Generation Platform NEOSAT, ESA ARTES programme, https://artes.esa.int/neosat/overview

[4] A. Shkel, “Type I and Type II micromachined vibratory gyroscopes”, Position, Location, and Navigation Symposium (PLANS), San Diego, 2006

[5] M. Descharles, J. Guérard, H. Kokabi, “Closed-loop compensation of the cross-coupling error in quartz Coriolis Vibrating Gyroscope”, Sensors & Actuators A: physical, vol 181, 2012

[6] M. Fossion, A. Van Esbeen, T. Van Humbeeck, Y. Geerts, E. Geukens, S. Redant, R. Jansen, C. Monteleone, “A Mixed-Signal Radhard Microcontroller: the Digital Programmable Controller (DPC)”, AMICSA, Geneva, 2014

Development of a Digital Temperature Transducer ASIC in a 28 nm FD-SOI CMOS Process for a Spaceborne Low Power Sensor Bus

P. P. Bora[a] , M. Roner[b], D. Borggreve[a], A. Hurni[b], E. Isa[a], L. Maurer[c]

[a]Fraunhofer EMFT, 80686 Munich, Germany
[b]OHB System AG, 82234 Oberpfaffenhofen, Germany
[c]Universität der Bundeswehr, 85577 Neubiberg, Germany

pragoti.bora@emft.fraunhofer.de

Abstract

A digital temperature transducer ASIC is being developed and prototyped in a 28 nm Fully Depleted Silicon on Insulator (FD-SOI) CMOS process. It features high performance and robustness at low power consumption. A thorough analysis defines the requirements for the transducer development, which are imposed by a future spacecraft application. The new serial bus sensor network architecture and harsh environmental conditions are the main challenges.

In order to achieve the required measurement inaccuracy of up to ±1 °C, over an extended temperature range spanning from -40 °C to +125 °C, several design measures are considered. A resolution of 0.1 °C is specified for the read-out circuitry. An integrated circuit "AMBER1" was developed in the frame of the European research project THINGS2DO, in order to prototype the central components of the temperature transducer. Among the various analog/mixed-signal and RF circuit blocks, a 1st order sigma-delta modulator and its constituent operational transconductance amplifier were integrated in AMBER1. The integrated circuit, in the new semiconductor process, was taped out in November 2015.

I. Introduction

Future spacecraft shall make use of electrical sensor networks based on serial buses, which provide both flexible and efficient ways to monitor important parameters. Since spacecraft housekeeping data is vital to a space mission, the reliability of such new sensor systems is crucial for their success. Traditional architectures rely on highly reliable sensors, interconnections and interrogators. It is usually difficult to improve the cost efficiency of such a design. A partial reduction of the temperature sensor count by improving the thermal design and heat transfer of the satellite was investigated at OHB System AG. Future spacecraft sensor networks, predominantly temperature measurement systems, shall however primarily reduce the cost of sensors, their interfaces, and interrogators, thus allowing to achieve high reliability by higher redundancy with better performance and cost effectiveness [1].

Large geostationary satellites typically employ several hundred resistive temperature sensors. These sensors are point-to-point wired to an acquisition unit, which is often a single central interrogator system. The application of platform temperature sensing was well suitable to introduce a new concept which shall reduce harness complexity and mass, while keeping system reliability, cost, and power consumption in mind.

Digital temperature sensors fabricated as integrated circuits (IC) have become a popular choice for use in thermal management systems in many commercial applications, featuring serial interfaces [2]. The temperature sensor and the digital interface circuitry for bus-type interfaces can be integrated on a single chip; thus enabling modularity and simplicity in the system design. Implementing a sensor network, in which the point-to-point connected resistive sensors are replaced with serially connected digital temperature

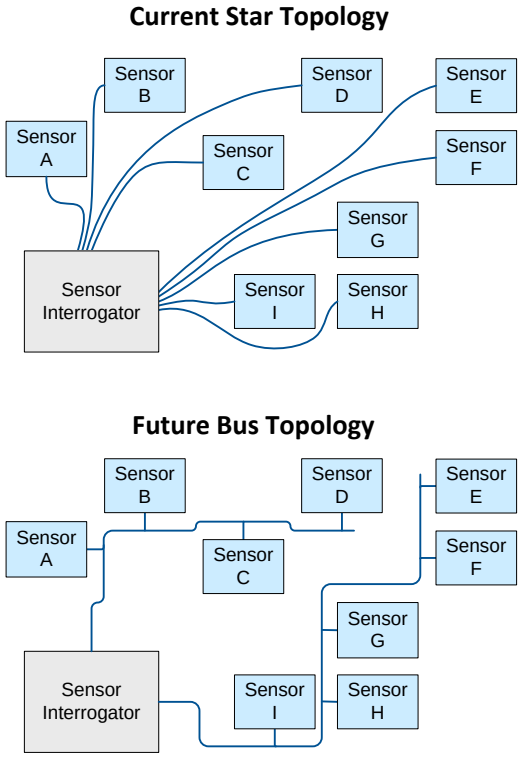


Figure 1: Replacing the star topology of the temperature sensor network with a bus topology

sensors, can result in a significant reduction in the amount of wiring. Figure 1 illustrates how the prevailing point-to-point star topology of the sensor-network shall be replaced with a bus topology.

The prevalence of portable electronics has caused a huge demand for process technologies that offer high performance at lower supply voltages and low leakage power. The 28 nm fully depleted silicon-on-insulator (FD-SOI) CMOS technology has become a state-of-the-art answer to this question. Apart from the various low power features offered by the FD-SOI devices, the inherent high robustness against transient radiation effects makes this CMOS process attractive for space electronics. The work carried out in the European research project called "Thin but Great Silicon to Design Objects (THINGS2DO)" project aims at realizing a sustainable ecosystem for the design and development of semiconductor components based on this modern technology in Europe [3]. An integrated circuit (IC) called "AMBER1" featuring various analog/mixed-signal and RF circuits blocks in the 28 nm FD-SOI CMOS process from STMicroelectronics was developed in the scope of this project [4].

This paper presents the system-level requirements of a temperature transducer (sensor) application-specific integrated circuit (ASIC), currently being developed in the 28 nm FD-SOI CMOS process. It shall become a part of a low power sensor bus system of a future spacecraft, where all the serially connected transducer ICs will communicate with sensor bus interrogator units. Section II gives a system-overview of the ASIC and describes its design requirements. A discussion about the FD-SOI CMOS technology and its radiation hardness properties is provided in section III. Section IV describes the AMBER1 IC that has been developed as an initial step towards realizing the temperature sensor ASIC. The target with AMBER1 was to design and validate some of the core components of the final system. The work presented in this paper is summarized in section V.

II. System Overview

A. System-level requirements

The sensor network architecture on-board future spacecraft, introduced in section I, induces several requirements on the transducer, whose structure is depicted in Figure 2.

To maximize the benefit gained by the new concept, the packaging and wiring of the sensors needs to be optimized for a more cost-effective harness design and integration in the spacecraft. The main focus at the current stage of development, however, are the performance requirements and the reliability of the sensor system.

The targeted temperature measurement range is from -40 °C to +125 °C. The acquisition of temperature with a high resolution of 0.1 °C is desired in order to track dynamic temperature changes. A worst case measurement inaccuracy of ±1 °C is specified for the nominal operational temperature range of -20 °C to +20 °C. A maximum inaccuracy of ±3 °C is allowed for measuring temperatures outside this range. In order to meet the accuracy requirement, the analog-to-digital converter (ADC) has to provide a specific resolution, depending on the linearity of the temperature sensor. The required target resolution of 0.1 °C translates to a minimum ADC resolution of 11 effective number of bits (ENOB).

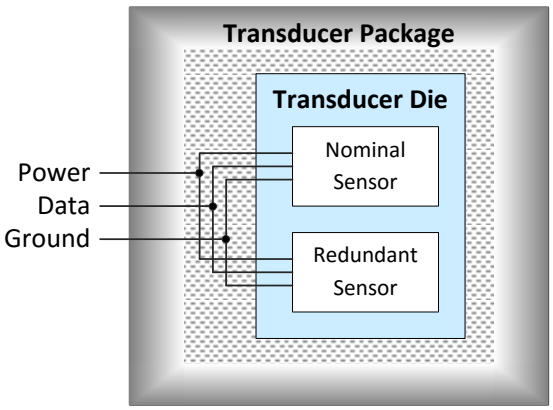


Figure 2: Packaged temperature transducer as final product

The temperature transducer shall provide a serial interface, which allows the creation of sensor networks with up to 30 nodes, implemented as stubs. An optional analog input for an external temperature sensor is foreseen for higher flexibility in testing and developing new solutions based on the present transducer ASIC.

The application on geostationary satellites, with a typical lifetime of 15 years in-orbit operation, requires the sensor to support a 20-year lifetime which includes ground storage, manufacturing and testing.

High-energy particles are major concern for electronics in space, especially semiconductors with small feature sizes. Since the introduction of 65 nm and smaller gate lengths, single event effects (SEEs) have increasingly become a concern in ground based applications too. An SEE occurs when a sensitive node collects a sufficiently high charge from the carriers which are generated by an ionizing particle. If no suitable design provisions are implemented, the trend of lower critical charges in SRAM memory cells leads, in many CMOS technologies, to higher soft and hard error rates. One unit of measurement for the SEE sensitivity is the linear energy transfer (LET) threshold and the corresponding cross section, which is the probability of an SEE at a certain LET value. Digital space electronics aim at raising the SEE LET threshold on device level above the typically encountered particle spectrum. In geostationary orbit, lying in the equatorial plane at 6.6 Earth-radii and hereby outside the radiation belt with higher particle energies, the probability of encountering particles such as protons with 10 MeV or more is very low, except during solar events [5, 6]. The demanding geostationary transfer orbit (GTO) passed by the spacecraft is more crucial for the SEE tolerance requirement.

In the present case of the temperature transducer, a high LET threshold for hard faults, especially single event latchup (SEL) is required in order to allow not only a reliable operation of each sensing device, but also to avoid fault propagation of the sensor bus. Therefore, the used CMOS technology shall be classifiable as SEL-hard with an SEL-LET threshold >100 MeV·cm²/mg. Single Event Upsets (SEUs) in memory cells are of less concern because the digital design of transducer is required to provide error detection and correction for single faults. Occasional Multiple Bit Upsets (MBUs) which lead to

corrupted data are, on the other hand, identified by the measurement system and are thereby tolerable. After the application of error detection and correction (EDAC) mechanisms, an SEU LET threshold of >20 MeV·cm²/mg is deemed sufficient.

From the perspective of total ionizing radiation dose (TID), in order to determine the expected requirements, the placement of the transducer devices on the satellite has to be investigated. An analysis of the current geostationary satellite missions at OHB System AG showed that components mounted inside the spacecraft are subjected to radiation levels not higher than 100 krad for a 15-year mission. However, components outside the protective shielding can be subjected to over 5 Mrad. The strategy to not exceed the radiation load supported by the device is to optimize the packaging and operating place of the transducer in coordination with the obtained TID hardness of the device. In order to provide a certain flexibility in the application, a TID hardness of 300 krad is requested at die level.

B. System-level description

For implementation in CMOS technology, various temperature sensing concepts based on resistors, thermal diffusivity of silicon and MOSFET operating in the weak inversion region, are proposed in the literature [7]. However, the majority of the state-of-the-art digital temperature sensors employ parasitic bipolar transistors as the sensing element. With a single-point thermal calibration, inaccuracies less than ±0.2 °C have been reported for such sensors in the temperature range of -40 °C to 125 °C [7]. Figure 3 shows the working principle of a parasitic PNP bipolar transistor based temperature sensor. The difference between the base emitter voltages ΔV_{BE} between the two transistors are combined to generate a voltage V_{PTAT} that is proportional to the absolute temperature. The reference voltage V_{REF} is generated by adding V_{PTAT} to the base-emitter voltage V_{BE} of one of the transistors. The measured temperature is converted by the ADC as a ratio μ of the V_{PTAT} and V_{REF}, which is also proportional to the absolute temperature. It can be expressed as:

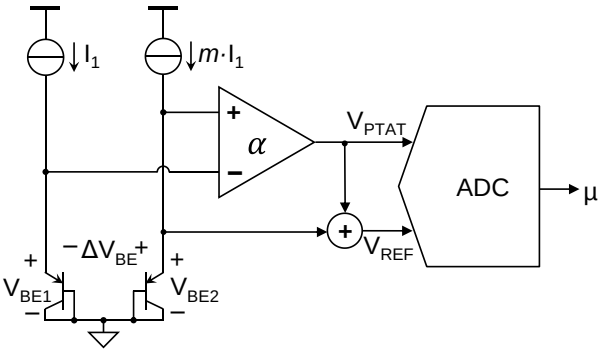


Figure 3: Working principle of a bipolar transistor based temperature sensor [8]

$$\mu = \frac{V_{PTAT}}{V_{REF}} = \frac{\alpha.\Delta V_{BE}}{V_{BE}+\alpha.\Delta V_{BE}} \qquad (1)$$

The measurement rate of the temperature sensors is limited by the thermal time constants of their packages; which are typically in the order of a few seconds. Therefore, sigma-delta ADCs are popularly used in such sensors because of their ability to trade low speed for high resolution [8].

On the system-level, the temperature transducer ASIC discussed in this paper, consists of three major design blocks: a bipolar transistor-based temperature sensor, a sigma-delta ADC, and a digital serial communication interface. Additionally, circuit blocks for the generation of the internal bias currents and low power digital calibration are included. The block diagram of the system is shown in Figure 4. A resolution of 14 bits is specified for the sigma-delta ADC.

The various design strategies that are considered for the mitigation of the radiation induced effects are as follows:

- System-level: Redundancy techniques such as triplicated clock tree, triplicated combinatorial logic and triplicated registers [9].

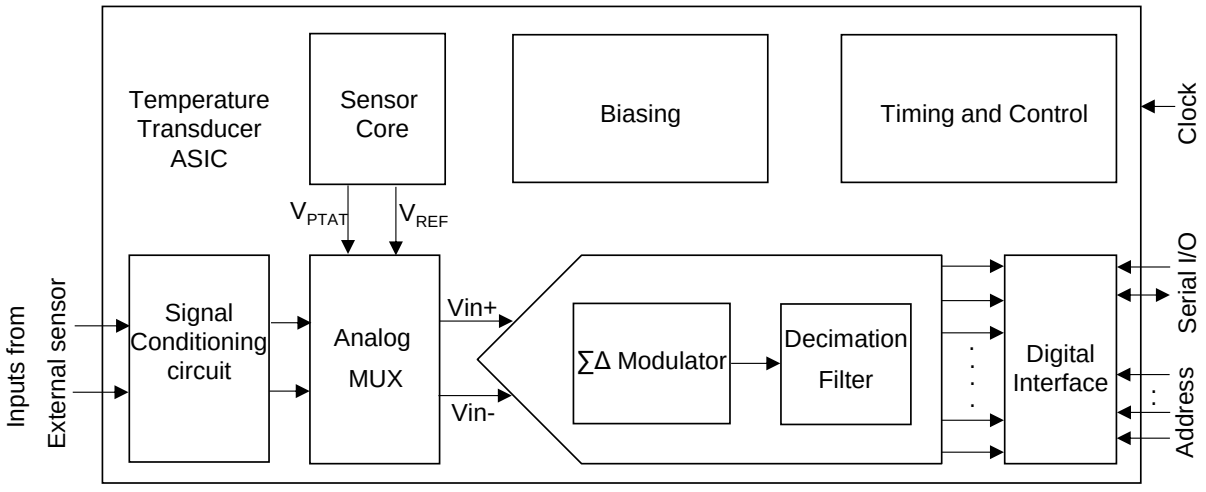


Figure 4: Block diagram of the temperature transducer ASIC

- Circuit-level: Optimal transistor sizing [10], circuit techniques for the compensation of leakage current [11], flicker noise and offset-compensation [12].
- Device-level: Design implementation on FD-SOI CMOS technology.
- Layout-level: Placement of guard-rings [13].

III. FD-SOI TECHNOLOGY

The 28 nm FD-SOI CMOS technology from STMicroelectronics features devices fabricated in a planar process with a 7 nm thin silicon film on a 25 nm Buried Oxide (BOX) [14] as shown in Figure 5. A minimum physical gate length of 24 nm can be achieved. The devices are fully depleted as the channel is left undoped because of the ultra-thin body. The construction of FD-SOI devices enables better control over the short channel effects. The 28 nm CMOS process offers many attractive features in this regard, namely, fast switching, low leakage currents, poly biasing and back-gate biasing for efficient power regulation, and expected latch-up immunity [15]. With the help of techniques like poly biasing and back-gate biasing the threshold voltage Vt can be effectively controlled to tune the circuit to achieve optimum performance and power-efficiency. Thanks to the BOX layer, these devices have reduced leakage currents and provide robustness against latch-up.

FD-SOI devices are found to be inherently resistant against transient ionizing radiation as a virtue of their construction. Reduction in the soft error rate (SER) is reported for designs based on these devices [16]. This can be attributed to the reduction in the effect of parasitic bipolar amplification, smaller sensitive volume for the ionizing particle to traverse, and inherent latch-up immunity [16, 17]. Figure 6(a) depicts how the charge generated due to an incident ionizing particle is collected into the drain region of a transistor in a bulk process. Figure 6(b) illustrates how the BOX layer is responsible for limiting this effect in an FD-SOI transistor. The FD-SOI devices are reportedly more susceptible to TID effects due to charge trapping in the BOX. However, the ability of these devices to withstand TID up to 1 Mrad has also been reported [18].

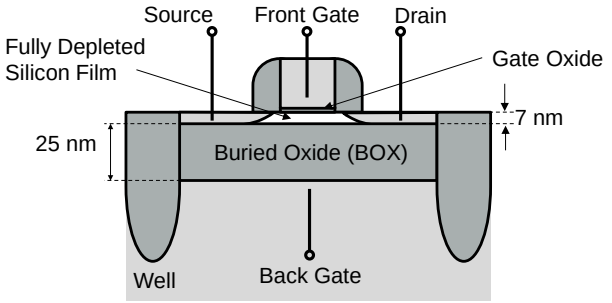


Figure 5: FD-SOI transistor cross-section

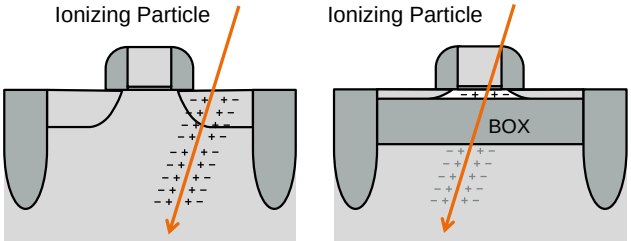


Figure 6: Effect of an incident ionizing particle on (a) bulk transistor (b) FD-SOI transistor

IV. AMBER1 IC

An IC named AMBER1 was developed in the 28 nm FD-SOI CMOS process and was taped-out in November 2015. RF blocks (Voltage Controlled Oscillator, Mixer, Low Noise Amplifier) and analog/mixed-signal test structures, realized at Fraunhofer EMFT, IIS, and EAS institutes, were integrated in it [4]. AMBER1 is developed to demonstrate the low-power features offered by this technology, and to design and validate some of the essential circuit blocks of the temperature transducer ASIC. As shown in Figure 7, the physical dimensions of AMBER1 are 1800 µm x 1800 µm. In total this IC contains 92 pads for the supplies and the signals. The analog and mixed-signal blocks are powered by 1.0 V nominal supply. However, for the digital input/output signals a supply voltage between 1.5 V and 1.8 V is required for the I/O ring.

A 1st order sigma-delta modulator and its constituent operational transconductance amplifier (OTA) were integrated on AMBER1. The sigma-delta modulator is fully-differential, switched-capacitor based circuit that features 1-bit quantization and operates with a bandwidth of 500 Hz at a sampling frequency of 200 kHz. The building blocks of the modulator include a fully differential single stage current-mirror OTA, a dynamic comparator, and a non-overlapping clock generator. Correlated double sampling technique was employed to reduce low-frequency noise and offset-compensation at the input-stage of the OTA.

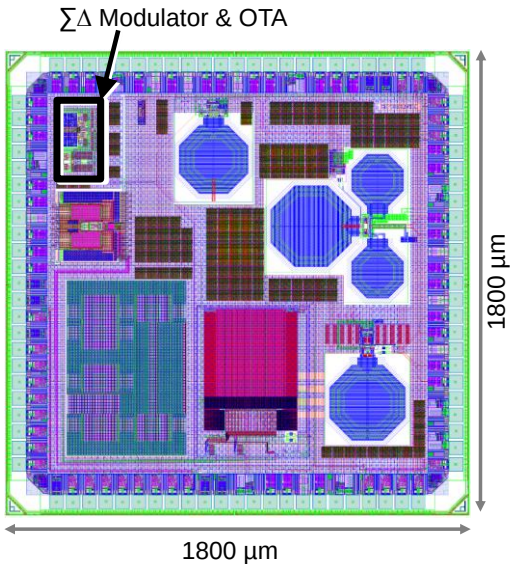


Figure 7: Layout of the AMBER1 IC

V. Conclusion

In this paper, we discussed the system-level requirements of a low-power digital temperature transducer ASIC targeted for incorporation in a sensor bus system of a future spacecraft. Temperature measurements, with a resolution of 0.1 °C, in the extended range of -40 °C to +125 °C is targeted. Accuracy requirements of ±1 °C in the -20 °C to +20 °C range and ±3 °C for the remaining temperatures are specified. The block level description of the ASIC and the strategies considered to mitigate the effects of radiation were also presented. The implementation of this ASIC is being carried out in the 28 nm FD-SOI CMOS process of STMicroelectronics. We discussed various features of this technology, pertaining to low power and radiation hardness. An IC named AMBER1, was realized with the goal to design and validate the crucial circuits of the final transducer system. A 1st order sigma-delta modulator and an OTA were integrated on AMBER1. It was taped-out in November 2015. Its silicon validation is planned for June 2016.

VI. Acknowledgement

The THINGS2DO project is funded by the European Commission (EU GA No. 621221) and the Bundesministerium für Bildung und Forschung (BMBF) (BMBF GA No. 16ES0240) within the framework of the European Initiative, ENIAC.

VII. References

[1] Hurni, A., Lemke, N.M.K., Roner, M., Obermaier, J., Putzer, P. and Chami, N.K., 2014, October. "Fiber-Optical Sensing On-Board Communication Satellites," in International Conference on Space Optics (Vol. 7, No. 10.10).

[2] Bakker, A., 2002. "CMOS smart temperature sensors-an overview," in Sensors, 2002. Proceedings of IEEE (Vol. 2, pp. 1423-1427). IEEE.

[3] http://things2do.space.com.ro/

[4] Bora, P. P., Borggreve, D., Isa, E. and Maurer, L., 2016, May. "Design of Analog-to-Digital-Converters in 28 nm Fully Depleted Silicon On Insulator CMOS Technology," in CDNLive EMEA 2016, Munich.

[5] http://ccmc.gsfc.nasa.gov/modelweb/magnetos/AP-8-min-max-76-6.pdf

[6] Tylka, A.J., Adams Jr, J.H., Boberg, P.R., Brownstein, B., Dietrich, W.F., Flueckiger, E.O., Petersen, E.L., Shea, M.A., Smart, D.F. and Smith, E.C., 1997. "CREME96: A revision of the cosmic ray effects on micro-electronics code," in Nuclear Science, IEEE Transactions on, 44(6), pp.2150-2160.

[7] Makinwa, K.A.A. "Temperature Sensor Performance Survey," [Online]. http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls.

[8] Pertijs, M.A. and Huijsing, J., 2006. "Precision temperature sensors in CMOS technology. Springer Science & Business Media.

[9] Garg, R., Jayakumar, N., Khatri, S.P. and Choi, G., 2006, July. A design approach for radiation-hard digital electronics. In Proceedings of the 43rd annual Design Automation Conference (pp. 773-778). ACM.

[10] Zhou, Q. and Mohanram, K., 2004, April. "Transistor sizing for radiation hardening," in Reliability Physics Symposium Proceedings, 2004. 42nd Annual. 2004 IEEE International (pp. 310-315). IEEE

[11] Cao, Y., De Cock, W., Steyaert, M. and Leroux, P., 2013. "A 4.5 MGy TID-tolerant CMOS bandgap reference circuit using a dynamic base leakage compensation technique," in Nuclear Science, IEEE Transactions on, 60(4), pp.2819-2824.

[12] Enz, C.C. and Temes, G.C., 1996. "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization," in Proceedings of the IEEE, 84(11), pp.1584-1614.

[13] Jing, W., Zuocheng, X., Ping, H., Tianran, W. and Guitao, F., 2010, October. "Practice on layout-level radiation hardened technologies for I/O cells," in Information Networking and Automation (ICINA), 2010 International Conference on (Vol. 1, pp. V1-365). IEEE.

[14] Planes, N., Weber, O., Barral, V., Haendler, S., Noblet, D., Croain, D., Bocat, M., Sassoulas, P.O., Federspiel, X., Cros, A. and Bajolet, A., 2012, June. "28nm FDSOI technology platform for high-speed low-voltage digital applications," in VLSI Technology (VLSIT), 2012 Symposium on (pp. 133-134). IEEE

[15] Magarshack, P., Flatresse, P. and Cesana, G., 2013, March. "UTBB FD-SOI: A process/design symbiosis for breakthrough energy-efficiency," in Proceedings of the Conference on Design, Automation and Test in Europe (pp. 952-957). EDA Consortium.

[16] Roche, P., Autran, J.L., Gasiot, G. and Munteanu, D., 2013, December. "Technology downscaling worsening radiation effects in bulk: SOI to the rescue," in Electron Devices Meeting (IEDM), 2013 IEEE International (pp. 31-1). IEEE.

[17] Alles, M.L., Schrimpf, R.D., Reed, R.A., Massengill, L.W., Weller, R.A., Mendenhall, M.H., Ball, D.R., Warren, K.M., Loveless, T.D., Kauppila, J.S. and Sierawski, B.D., 2011, October. "Radiation hardness of fdsoi and finfet technologies," in SOI Conference (SOI), 2011 IEEE International (pp. 1-2). IEEE.

[18] Gaillardin, M., Martinez, M., Paillet, P., Raine, M., Andrieu, F., Faynot, O. and Thomas, O., 2014. "Total Ionizing Dose Effects Mitigation Strategy for Nanoscaled FDSOI Technologies," Nuclear Science, IEEE Transactions on, 61(6), pp.3023-3029.

Development of a Satellite TV receiver for fibre optic distribution system

G. Leach[a] , I. Watson[a]

[a]Riverbeck Ltd, SN2 8BW Swindon, United Kingdom

Email : graham.leach@riverbeck.com, ian.watson@riverbeck.com

Abstract

In this paper we highlight the design work performed by Riverbeck Ltd on the Romeo and Juliet chipset paid for by Global Invacom and the European Space Agency.

Romeo and Juliet are application specific integrated circuits developed as the receiver element of a satellite TV, terrestrial TV and FM radio fibre distribution system. Fibre distribution of media signals is particularly attractive to multi-dwelling units where any TV or radio channel can be demanded by any dwelling. This requires the entire signal bandwidth be provided to all dwellings. A fibre system reduces the infrastructure cabling, is immune to electrical interference, suffers from less signal loss and can be passive split without detriment to reception.

The fibre distribution transmitter (not within scope of this paper) frequency shift and modulates terrestrial radio, TV, and satellite signal using a 1310 nm semiconductor laser.

Romeo and Juliet amplify the received photodiode signal, filter and frequency shift the 5GHz bandwidth to provide a set top box with the same data were it directly connected to a LNB. Romeo is a dual gain, low noise amplifier with differential outputs. Juliet provides broadband programmable RF gain, wideband continuous time filters to clean up the output spectrum, RF power detectors, 75Ω and 50Ω line driver outputs, phase locked loops to frequency shift the received spectrum, monitoring circuits and digital interfaces.

I. INTRODUCTION

European satellite television is broadcast in Ku band between 10.7 - 12.75GHz using two polarisations providing 4.1GHz bandwidth [1]. The bands are named vertical low (VL), vertical high (VH), horizontal low (HL) and horizontal high (HH). Within each band TV channels are broadcast as phase modulated transponders where each transponder is ~30MHz.

Historically the distribution of TV channels has been realized by F type coax, but the cable bandwidth is less than the signal bandwidth. To allow arbitrary channel choice multiple parallel cables are installed. A historic installation is shown in figure 2.

To reduce the coax cabling in single occupancy but multi tuner homes manufacturers now offer digital channel stacking (DCS) technology [2]. DCS reduces the coax cabling requirements but limits the number of TV channels concurrently available. By comparison fibre optic distribution of TV provides all channels to all users concurrently and removes the electrical limitations of coax cabling.

The proposed architecture shown in Figure 1 radically changes the satellite IF architecture. The conventional satellite TV LNB is replaced with an optical LNB that frequency stacks all satellite bands 950MHz – 5.45GHz onto a fibre optic cable (In additional terrestrial TV and radio can be stacked onto the fibre optic at <800MHz). At the receiver the satellite bands are moved to their original frequency locations so the frequency stacking is transparent to the set top box (STB).

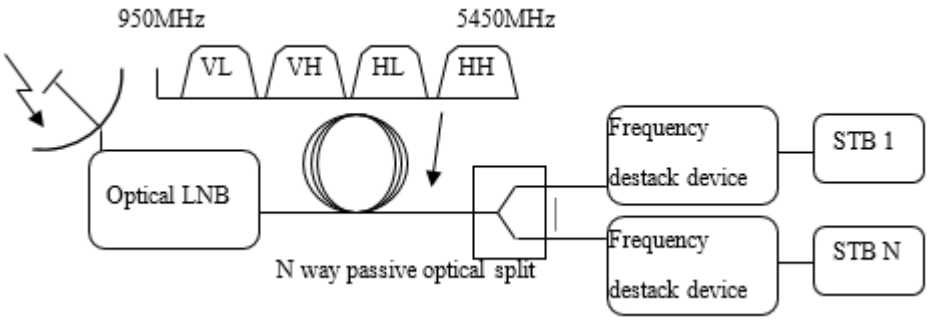


Figure 1: Proposed Satellite television distribution system

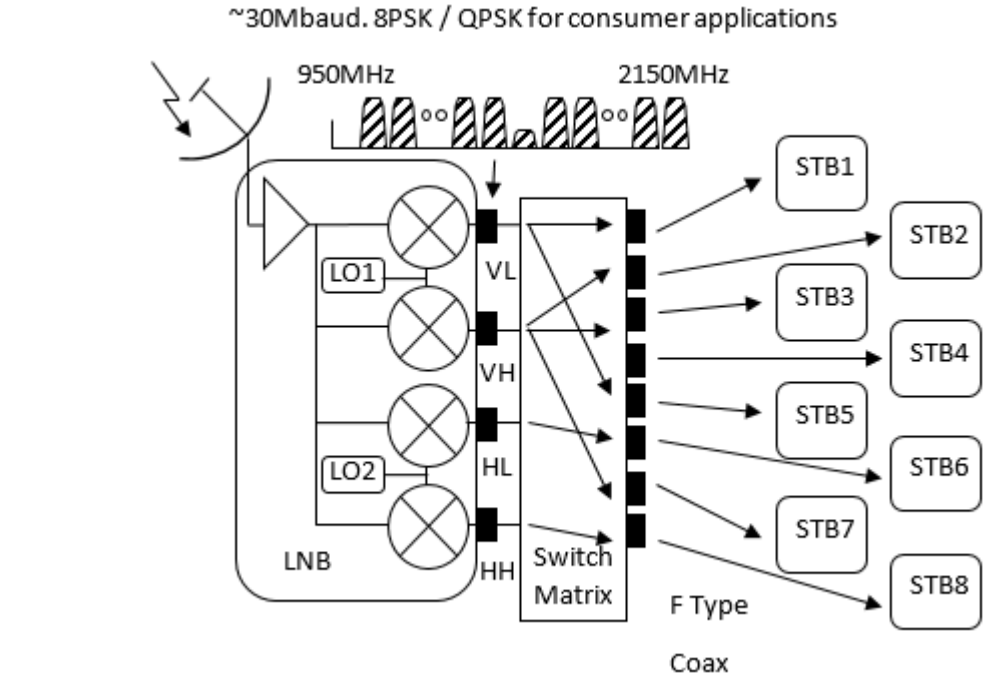


Figure 2: Legacy Satellite television distribution system

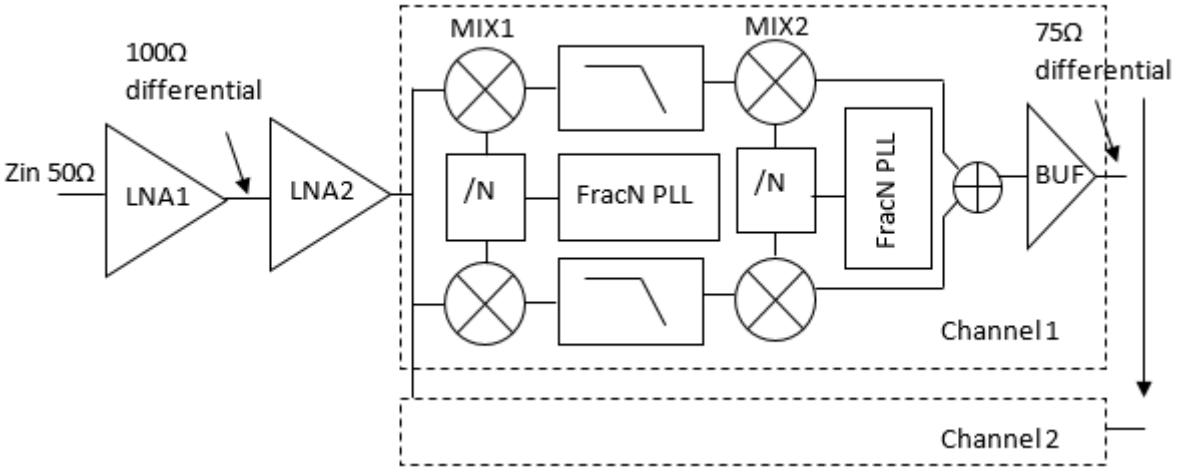


Figure 3: Block Diagram of Frequency destack device

Figure 3 shows a block diagram of the chipset architecture. It is a two integrated circuit solution implemented in 180nm BiCMOS. Whilst both integrated circuit were implemented in the same technology LNA1 is a separate device to improve electrical isolation. Between the devices is a pair of 100 Ω differential microstrip lines. The overall gain is programmable from 15 dB – 45 dB, see Figure 5.

On the main integrated circuit is a homodyne receiver with 1GHz complex IF bandwidth, programmable gain stages and continuous time channel filters followed by a homodyne transmitter. By mixing down the signal to baseband and up converting to the output frequency the lowest order channel filter to meet the attenuation requirements can be implemented. The architecture also allows the frequency shift to be defined by the difference in mixer local oscillator (LO) frequencies. Integrated low phase noise, but wide frequency tuning fractional N, LC PLLs provide the LO requirements.

The output buffer provides -18dBm at 4dBm OIP3 into 75Ω via a 1:1 balun to drive a STB. An output balun improves electrical isolation and removes common mode mixer energy from the output spectrum.

Figure 3 shows the main integrated circuit is a two channel device. Either output can output any band (VL, VH, HL or HH) to the STB.

II. LNA

The low noise amplifier (LNA) is a dual gain amplifier. The amplifier is constructed from two parallel input stages with different gains and a common output stage. Depending on the

gain selection, the appropriate amplifier is enabled. The inactive amplifier has high input impedance when off and does not affect the active amplifier.

A simplified schematic of the high gain amplifier is shown in Figure 4. The input transistor and main amplifying transistor is Q0. A cascaded device Q1 reduces the voltage gain of Q0 to reduce miller effect of Q0 cbc. R0 is the load resistor. Q2, and Rfb form a negative feedback loop that define the input impedance Zin=Rfb/(1+A). The LNA return loss is better than 10dB from 50MHz – 5.45GHz.

The low gain LNA is a similar design except Q0 has series feedback to reduce gain and provide higher linearity but has higher noise figure.

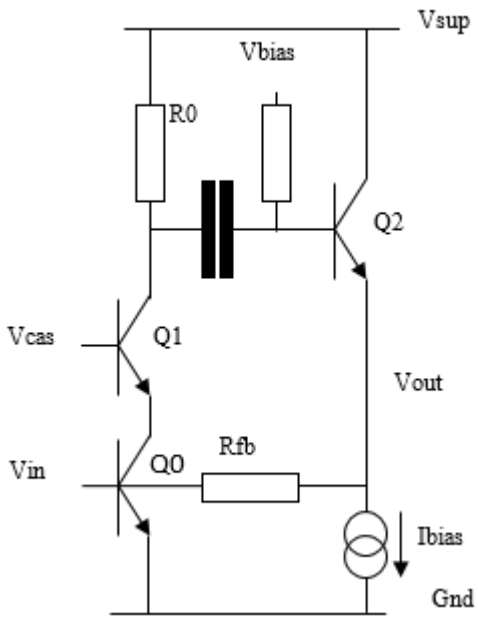


Figure 4: LNA Schematic

III. PGA AND GAIN CONTROL

On chip RF log power detectors measure the total input power and power in bands VL VH, HL and HH. The power detector measurements are digitised and drive a single loop digital gain control loop.

The overall gain is the sum of gain blocks LNA1, LNA2, MIX1, MIX2 and BUF in Figure 3. These cells provide high resolution gain control that maximises system signal to noise ratio over process, voltage and temperature variations
Rain fade affects received power level but can be tracked as the effect is a slow time constant.

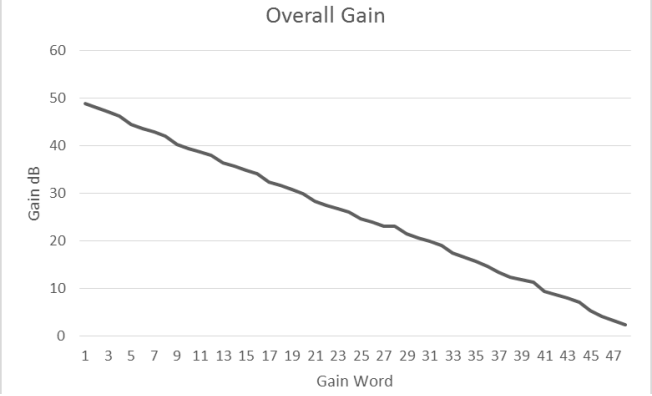


Figure 5: Overall Gain versus Gain Word

IV. LC VCO, PLL AND FREQUENCY PLAN

Due to the wide frequency spacing of VL, VH, HL and HH bands the MIX1 LO must tune 1.45GHz - 4.925GHz. MIX2 LO must tune 1.45GHz – 1.625GHz.

To reduce the oscillator tuning range (and silicon area) the oscillators were designed to run at 2x and 4x LO frequency. The MIX1 LO tuning frequency range remains too large for a single VCO so the additional tuning range is implemented as an oscillator array with overlapping frequency coverage. A negative resistance NMOS LC oscillator topology was selected for each oscillator as shown in Figure 6. Periodic noise analysis showed significant phase noise contributed by the bias network and to remove this a large external capacitor was added to the design. Phase noise is typically -90 to -95 dBc at 100KHz offset from the LO frequency.

During the PLL lock time, a search algorithm selects the lowest phase noise VCO when multiple oscillators oscillate at the target frequency.

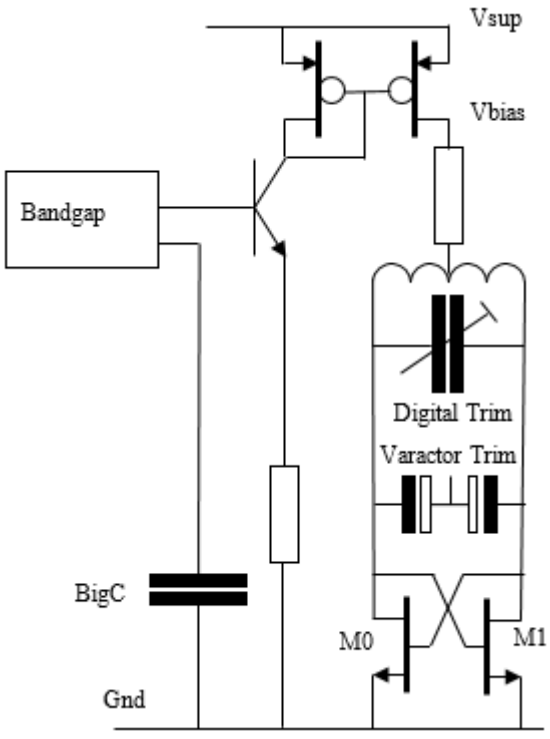


Figure 6: VCO Topology

The digital trim provides coarse frequency VCO tuning whilst the varactor controlled by the charge pump and PLL loop dynamics provides fine frequency tuning.

The high speed PLL dividers are implemented as CML logic and the low speed dividers in CMOS. The overall PLL architecture is a conventional Type II charge pump design.

When both channels are active, four LC VCO PLLs operate concurrently. If two VCO frequencies are within ~10MHz of each other the PLL loop dynamics interact and cause catastrophic in band spurs [3]. In this application we mitigate this issue as the frequency shift is controlled by the difference in LO MIX1 and LO MIX2 and not the absolute frequency of either LO. Software is used to detect potential clashes and move LO frequencies.

V. Channel Filter

The Channel filter is a 3rd order transconductance capacitance (gmC) filter with cut off frequency tunable from 500MHz – 720MHz. The filter is trimmed by measuring the frequency of a slave oscillator constructed from the same components as the filter. The transfer function is shown in Figure 7.

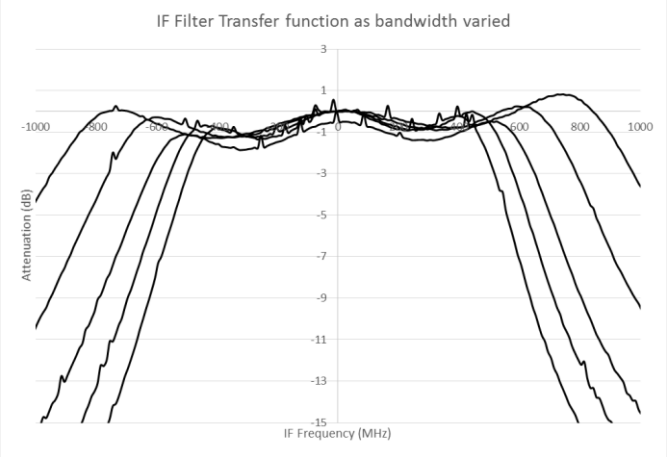


Figure 7: IF Filter Transfer Function

The gmC filter transconductance cell is implemented using resistively degenerated long tail pairs with current source loads. In Figure 8 M0, M1, R3 and R4 provide the current load and common mode feedback. Transistors Q0 and Q1 are degenerated by R1 and R2 respectively.

Many high frequency gmC filters use Nauta's gm cell [4], but in this technology the bipolar ac performance is far superior to the CMOS.

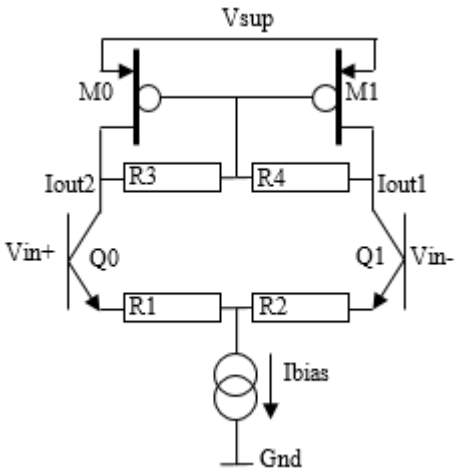


Figure 8: Transconductor Schematic

VI. Conclusions

In this paper we present a new method to distribute satellite TV signals within multi dwelling buildings. The solution provides the entire signal bandwidth to all users at all times.

As demand for satellite TV bandwidth grows due to introduction of more high definition and ultra high definition content we expect this technology to be widely adopted.

This development is a great example of silicon up integration. Analogue blocks that historically required many discrete components can now be realised as a system on chip.

VII. Acknowledgements

The authors would like to thank Malcolm Burrell, Gary Stafford, Andrew Collar and Grigoriy Shestak at Global Invacom Limited, Richard Jansen from ESA and Rob Sneddon and Ruiyan Zhao for their contributions to the success of this project.

VIII. References

[1] https://www.dvb.org
[2] Pierre Busson et al (2010, Jan) A 1GHz Digital Channel Multiplexer for Satellite Outdoor Unit IEEE J. Solid-State Circuits Vol. 45 No.1 P.84
[3] Behzad Razavi (2003) A Study of Injection Pulling and Locking in Oscillators. Custom integrated Circuits Conference P.305 http://www.seas.ucla.edu/brweb/papers/Conferences/RCICC2003.pdf
[4] Bram Nauta. (1992, Feb) A CMOS Transconductance-C Filter Technique for Very High Frequencies. IEEE J. Solid-State Circuits Vol.27 No.2 P.142

DiReRa: New Rad-Hard Chip-Set for Radiometers

F. Piazza[a] , A. Consoli[a], R. Materni[a]

[a]Saphyrion Sagl, 6934 Bioggio, Switzerland

francesco.piazza@saphyrion.ch

Abstract

Current RF front-ends for L-band radiometers are implemented using discrete or low integration level devices, which leads to quite large complexity, size, weight and cost of such front-ends. This paper describes the first prototypes of an RF front-end chip-set – called DiReRa – which consists of an L-band RF down-converter and a 1-bit AD-converter, and which can be used to implement the RF subsection of a radiometer in a much more compact and simpler way. Although developed specifically for radiometer applications the DiReRa chip-set is general enough to cover also many other applications, mainly in the telecommunications domain.

This project is a collaboration between Saphyrion Sagl and TRYO Aerospace (former MIER Comunicaciones). Saphyrion is in charge of developing the DiReRa chip-set, while TRYO Aerospace contributed with the specification of the chip-set and is in charge of developing and manufacturing the next generation radiometers that will use the DiReRa chip-set in their RF subsystem. LICEF-3 EM units from the SMOS program will be used to verify the functionality and performances of the prototype chip-set.

Currently a 1st prototype chip-set, manufactured on the AMS S35 HBT SiGe process as MPW and electrically tested and characterized is available. The DiReRa chip-set demonstrated rather good performances, as well as good agreement between simulations and measured results. The next steps should be to first finalize the design of the chip-set, then proceed with its qualification and industrialization.

I. Introduction

Saphyrion Sagl is developing under an ESA contract [1] a new chip-set for L-band radiometer applications. The chip-set consists of an RF down-converter, which is called DiReRa, and a latched comparator (1-bit AD-converter), called DADC. The chip-set is being developed in collaboration with TRYO Aerospace, who will use it on their next generation of radiometers.

The objective of this work is to integrate the RF front-end subsystem of the L-band radiometer into a chip-set, such that its complexity, power consumption, size, weight and cost can be reduced substantially with respect to those of current discrete implementations. The devices will then be manufactured and assembled using a SiGe process [2] and techniques compatible with Space operation and qualified to ESCC9000 [3]. Such chip-set would have substantial potential in applications that need a large number of small highly integrated radiometers, such as the Soil Moisture and Ocean Salinity (SMOS) mission, with further potential e.g. in the SMOS-Ops, GEO-sounders or the Sentinel-3 missions.

In order not to compromise the performances or the radiometer the performances of the IC implementation of the RF front-end should be comparable to the ones achieved by the current discrete implementations. Since an integrated circuit is very different from a discrete design, some changes to the RF subsystem are needed to achieve such objective. It is quite fundamentally impossible to design an exact 1:1 replacement of a discrete design in IC form.

In this paper the architecture of the new chip-set and the radiometer including it, as well as the design choices and trade-offs, will be presented, followed with some circuit details. Results from the electrical characterization will be presented next. As a conclusion the remaining steps towards industrialization and space qualification to ESCC9000 of the chip-set will be shown, together with the planned road-map.

II. Circuit Description

A. IC Characteristics and Constraints

An IC is very different from a discrete design. When specifying an IC it is therefore important to consider these differences, otherwise the resulting specification is very likely not realizable. The most important characteristics that shall be taken into account when specifying an IC are these:

- **Single process must fit everything,** which means that all blocks shall be designed using the same component types with the same characteristics.
- **Limited component values with large tolerances.** Typically there are just 1-2 transistor types, resistors are limited to a few 10Ω to a few 100kΩ and have 20-25% tolerance, capacitors are limited to some 10pF and 10-15% tolerances, while inductors range between about 200pH and 5nH and have low Q. Distributed components (couplers, power splitters, etc.) do not exist at all at low GHz frequencies.
- **Excellent component matching:** this is a characteristic peculiar to ICs. Relative tolerances in the 1% to 0.1% can be achieved rather easily despite the large absolute tolerances of IC components.

- **Coupling through the substrate.** All components in an IC must share the same substrate. The achievable isolation between them depends on frequency and is limited to about 20-30dB at frequencies of 1-2GHz. This limits e.g. maximum gains, crosstalk between channels or attenuation of filters. Balanced circuits are almost always required.
- **Limited number of pins.** In RF circuits package and pins parasitics have a large influence on RF performances. The only way to reduce their influence is to use very small packages with short pins and bonding wires, which in turn limit the number of pins.

B. Radiometer Architecture

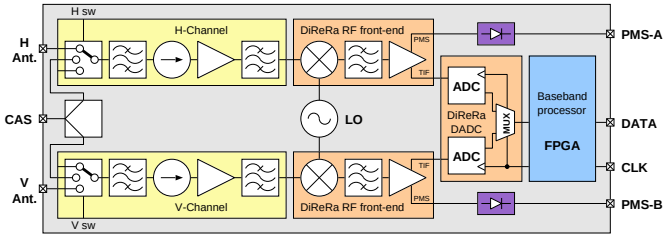


Figure 1: Block diagram of the radiometer.

A simplified block diagram of a future radiometer core using the DiReRa chip-set is shown in Figure 1: it implements full H-V polarimetric mode and is able to measure both H and V polarizations at the same time.

The RF subsystem consists of two identical RF front-ends that include a discrete RF path (LNA, isolator and filters) and a down-converter (mixer, IF-strip) implemented with the DiReRa chip-set, shown in orange in the figure. The local oscillator and PLL are implemented again with discrete components. In order to obtain the best possible isolation between H and V paths separate front-ends are used, which will be enclosed in separate cavities.

The outputs of the DiReRa RF ASIC then go to the power measurement subsystem (PMS) and to a DiReRa DADC 1-bit AD-converter (dual comparator) chip, where it is sampled and digitized. Baseband processing is finally implemented on an FPGA, whose output goes to a digital correlator.

The use of the DiReRa chip-set in the RF subsystem is expected to lead to a quite substantial reduction of weight and size of future radiometers. LICEF-3 EM units from the SMOS program will be used to verify the functionality and performances of the prototype.

C. Semiconductor Process Selection

The choice of a semiconductor process for DiReRa cannot be done based on performances alone, but also needs to consider additional parameters, both technological and non-technological. The most important requirements are:

- Proper RF performances at GHz frequencies.
- Available in quantities compatible with Space applications, i.e. a few 100 pieces yearly at most.
- Can be radiation hardened.
- Sufficiently low NRE costs, in particular the price of the full mask-set.

A space-qualified process fulfilling all requirements could not be found, thus the commercial AMS S35 process [2] was selected on the basis of the good experience made with the design and qualification of the SY10x7 GNSS chip-set [4], [5] that are designed using this same process.

The AMS S35 is a 0.35µm HBT BiCMOS process that includes NPN BJT with a transit frequency of 38GHz, 3.3V CMOS transistors, as well as high and low ohmic resistors and high quality MIM capacitors. Rad-hard standard cells and I/O pads libraries previously developed and tested by Saphyrion during the SY10x7 project were also readily available.

D. DiReRa RF Front-end Architecture

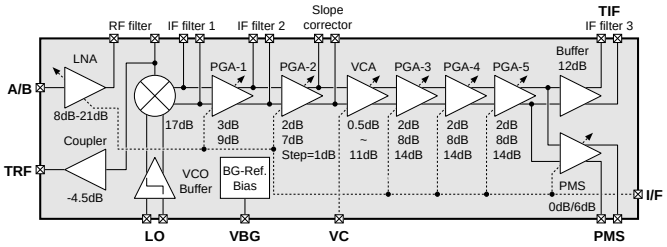


Figure 2: Block diagram of the DiReRa RF front-end.

The DiReRa RF front-end ASIC is a single conversion superheterodine RF front-end that includes all blocks needed to build the RF section of the L-band radiometer.

Figure 2: shows the block diagram of the ASIC. It contains a programmable gain LNA (2 different gains), a double-balanced active RF mixer with active input signal coupler (transmission-line couplers do not exist in IC form), an IF-strip comprising digitally programmable gain stages (PGAs) and a VCA stage, and finally an IF output buffer with linear power measurement amplifier and the output for the 1-bit AD-converter.

1) Frequency Plans

The DiReRa RF front-end is a wideband design with no on-chip filtering, it thus supports a wide range of frequency plans. Some possible frequency plans – based on ESA and TRYO Aerospace requirements – are shown in Table 1:

Table 1: Some possible frequency plans for the DiReRa chip.

RF Freq.	LO Freq.	IF Freq.	fs.	Unit
1200-1600	1180-1580	25-35	130	MHz
1413.5	1396	17.5	55.84	MHz
1200-1600	1167.5-1567.5	32.5	130	MHz
1200-1600	1037.5-1437.5	162.5	130	MHz
1413.6	1288	125.6	55.84	MHz

Basically good frequency plans for an RF receiver with IF sampler are obtained by placing the IF roughly in the middle of a useful band of the AD-converter, i.e. IF=fs*(1+2N)/4,

with N an integer. Since due to the requirement to support widely different frequency plans the DiReRa ASIC does not contain any image reject mixer and has to rely uniquely on external RF filtering, frequency plans with a low IF that place the image frequency very close to the desired RF frequency will lead to rather challenging RF filter design.

2) Circuit Design

The main circuit blocks of the DiReRa chip, as well as the required external filters are described here. Support blocks such as the interface (parallel, combinational) or bias and band-gap reference circuits are omitted.

- **LNA:** It is a single stage inductively degenerated cascode amplifier, which provides 2 programmable gains. Such architecture was chosen to achieve good noise figure and linearity at the same time. It provides G = 18.0dB and NF = 1.7dB for the high gain setting, G = 6.5dB and NF = 2.3dB for the low gain setting. The ports are 50Ω unbalanced and require external matching networks.
- **Mixer:** An active double-balanced mixer has been used. Double-balanced active mixers provide good linearity, good local oscillator and common-mode rejections (substrate coupling, isolation from LNA) without requiring high LO drive levels at the expense of noise figure. All ports are balanced, the input port is 50Ω, the output port is 600Ω, while the local oscillator port is high impedance to simplify bridging of two channels on a single LO signal. The mixer has an SSB voltage gain = 14.5dB and NF = 12dB.
- **IF-strip:** it is a 7-stage amplifier chain consisting of 5 PGAs, a VCA, an output buffer and a PMS amplifier. A differential amplifier structure has been used throughout, in order to achieve rejection to common-mode signals and noise. The gain of the IF-strip can be programmed digitally in 1dB steps, while a VCA analogue input provides a further regulation over a 10.5dB span. The overall gain can be set from 19.5dB to 71dB nominally. All I/O ports are 600Ω balanced, and given the rather high gain that the IF-strip can achieve it is important that all ports are kept well balanced, otherwise instability or oscillation due to substrate coupling may occur.
- **Filters:** The DiReRa front-end is a wideband design and requires external filters to select the channel and remove the image frequency. At RF a SAW filter can be used quite effectively and has a small size, while at IF a coupled resonators LC-filter has been selected. This filter topology is particularly suitable for use with an IC receiver since the resonators will present a low impedance outside their bandwidth (i.e. the ports become shorted), thus improving rejection to substrate coupled signals.

Currently the 1st prototype of the DiReRa chip has been completely designed, integrated using the MPW program of the foundry (AMS) and successfully tested and characterized.

E. DADC AD-Converter Architecture

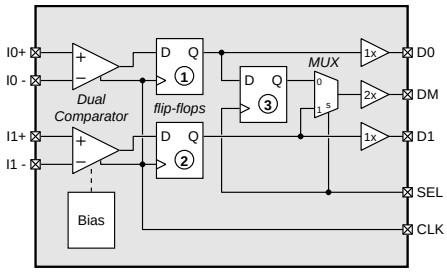


Figure 3: Block diagram of the DADC AD-converter.

The DADC 1-bit AD-converter is a dual latched comparator operating at up to 130MHz. It is meant to digitize the IF signal coming from the DiReRa front-end (TIF output). The most critical requirement is a 0-1 imbalance of 0.5% that should be obtained with no on-line calibration.

Figure 3: shows the block diagram of the DADC chip. The device includes two 1-bit AD-converters (comparators). The output of these comparators is stored in flip-flops 1 and 2 before being delivered to the output directly and through a multiplexer. The select input for the multiplexer is also the clock of flip-flop 3 and is available externally. An external delay shall be added between signals CLK (main clock) and SEL (delayed clock).

1) Circuit Design

Again only the main circuits – i.e. the comparators and the latching and deglitching circuits are described here.

- **Comparators:** they are latched regenerative comparators. Such comparator structure has been chosen since it provides high sensitivity (it can resolve signals <1mV rather easily), high speed and a clean low jitter sampling together with low power consumption. A rather careful design of the comparator is necessary to fulfil the specified 0.5% 0-1 imbalance specification. The intrinsic matching between transistors (a characteristic of the process) will become the limiting factor. The comparators are clocked with the CLK signal.
- **Latches and deglitching:** in order to have stable values the output of the comparators is latched into flip-flops (1 and 2 in Figure 3:) before being output. The outputs D0 and D1 change on the rising edge of CLK. The two comparator's output also go to a multiplexer. A deglitching flip-flop (3) – clocked by pin SEL – was requested by TRYO Aerospace for compatibility with their existing radiometer designs. In order to operate properly, a delay of ≥2.8ns is necessary between CLK and SEL.

Also the DADC chip is currently completely designed and was integrated together with the DiReRa chip in the same MPW. It has been successfully tested and characterized.

F. Chip Layout

The layout of the DiReRa chip-set is completely made by hand. Since the AMS process used is not rad-hard and thus no rad-hard library was available, all cells and I/O pads were re-designed from scratch following design rules developed by Saphyrion and briefly described in the following Section III.

Figure 4: shows the layouts of the DiReRa RF front-end (left) and the DADC dual comparator (right). The DiReRa RF chip has 42 pads and a size of 1280µm x1200µm. It is meant to be packaged in a hermetic 40 pins CQFN package of ceramic-metal construction (2 pads will be bonded to the die attach pad only). The DADC dual comparator has 16 pads and a size of 610µm x 880µm. It is meant to be packaged in a 16 pins CQFN package, again of ceramic-metal construction.

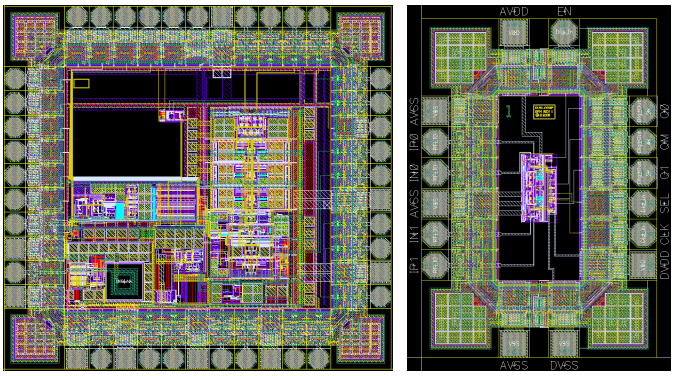


Figure 4: Layouts of DiReRa (left and DADC (right).

III. Radiation Hardening

The DiReRa chip-set is meant for use on board of satellites, thus a rad-hard design and Space qualification (to ESCC9000 [3]) is necessary. On the other hand a process with good RF performances at GHz frequencies is needed while whatever rad-hard technique used shall not degrade electrical performances or dimensions of the chip unduly. Since a commercial process had to be used (Section C), radiation hardening was done completely in-house by Saphyrion.

G. Total Dose

Robustness against total dose effects is mainly a characteristic of the semiconductor process used. Basically thin base BJTs and thin oxide MOS transistors give improved robustness. The process selected for DiReRa is the AMS S35 process, i.e. the same process used for the SY10x7 GNSS chip-set [4], [5] for which extensive TD tests with successful results up to >100kRad(Si) are available.

On the circuit design side, effective design techniques that give good robustness against TD degradations are e.g.:

- The use of balanced signal paths designed with carefully matched differential pairs, such that eventual parametric drifts are compensated,
- The use of active bias circuits that compensate β degradation of bipolar transistors.

These techniques have been used throughout where applicable in the design of the DiReRa and DADC chips.

H. Heavy Ions

SEE can be critical. Customers put indeed much weight on SEE, as previous experience has demonstrated. At the best SEE requirements must be based on existing standards and handbooks [6],[7],[8].

1) Single Event Latch-Up

SEL is a potentially destructive event for which no circuit design tricks exist to counteract it. Devices that show SEL <60MeV·cm²/mg shall be protected against SEL with external circuitry [7]. Our objective is pass at LET ≥85MeV·cm²/mg.

Achieving such an objective is possible also if a bulk (not SOI) process is used, as demonstrated by the SY1017C [5] device, if the following rules are followed:

- Continuous, uninterrupted guard rings are used to separate all opposing N and P areas.
- Good (distributed) substrate/well contacts are placed near to all transistors sources.

Figure 5: shows an example of such rules applied to digital standard cells. In order to save space the cells only contain the horizontal section of the guard ring, which is completed once the cells are assembled into lines. These rules were followed thoroughly in the design of the DiReRa chip-set.

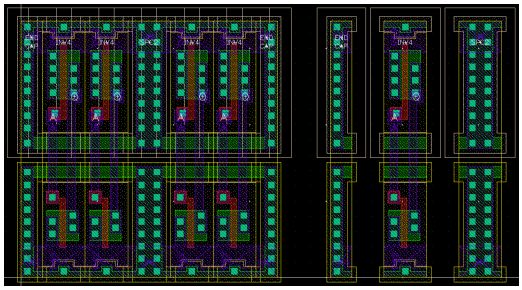


Figure 5: Rad-hard cells with continuous guard rings (example).

2) Single Event Transient, Upset

The DiReRa ASIC is an analogue RF chip that contains no sequential circuit. All control lines are combinational and level sensitive, thus SEU cannot happen. SET have the following effect on DiReRa:

- SET on RF/IF amplifiers and the mixer stage cause mostly noise.
- SET on enable lines may cause a circuit block to turn off and back on.

For the 1st case no particular countermeasure needs to be taken. The 2nd case is somewhat more delicate, as off/on transients on low speed blocks (bias, band-gap reference) may cause long recovery transients. Enable and control lines are protected with *drive strength hardening*, bias circuits are designed to recover quickly from transients, while the band-gap reference is protected with a large (external) capacitor.

The DADC chip contains latches (the comparator itself and the flip-flops) and is thus subject to both SET and SEU. Such effects will cause errors that however result only in

noise. The same protection strategies used on the DiReRa, i.e. drive strength hardening and fast recovery circuits were used also for the DADC. The use of TMR, especially on the sensitive comparator stage, was considered but not implemented due to the little advantage it would have provided.

IV. Test Results

The DiReRa chip-set was electrically tested and characterized in Saphyrion's laboratory. Since the DUTs operate at GHz frequencies, in order to characterize them specific RF test fixtures (PCBs) were prepared. The DiReRa and DADC bare dies were assembled in plastic scoop&goop QFN packages and soldered to the test PCBs. Finally filters and matching networks were aligned.

All measurements gave good results and showed a good agreement between simulated and measured performances. Also the rather critical 0-1 imbalance requirement (<0.5%) for the DADC seems achieved at least under typical conditions. Due to these results no major modifications or adjustments are therefore needed. The chips can therefore be completed and finalized using the unmodified circuit blocks. A summary of the measured results is shown in Table 2:.

V. Conclusions

The DiReRa RF front-end and DADC dual comparator 1st prototypes were designed, manufactured as MPW and electrically tested. Good results were achieved, which would suggest to proceed with the finalization of the design and if no problems are found to proceed with the industrialization. The remaining necessary steps will be the following:

- Do a *preliminary* irradiation test on the current prototype to mitigate any radiation-related risk and to characterize possible radiation-induced drifts.
- Finalize the chips using the current MPW-1 design data, then do an *engineering run*. Production ASICs will be taken from this engineering run.
- Develop and procure the *ceramic-metal hermetic packages* for both ASICs, then assemble a 1st lot.
- Develop *production screening* and run it on the 1st production lot.
- Do a *qualification* of the two devices, possibly in parallel to make better use of resources and save time and money. This involves endurance, environmental and radiation (total dose and heavy ions) tests.
- Prepare the necessary *documentation*, which comprises data sheets, procurement specifications, qualification and irradiation test reports.

At the end of this still quite long process, the DiReRa and DADC chip-set will be ready to be used in an actual radiometer system and will be introduced in Saphyrion's catalogue of Space-qualified ASICs.

VI. References

[1] ESA/ESTEC, *Digital Receiver for Radiometers*, ITT 1-7589/13/NL/GLC, 04 June 2013.

[2] AMS AG, *0.35µm HBT BiCMOS Process Parameters*, Document No. ENG219, Rev. 5, 14 May 2009.

[3] ESA/ESCC, *ESCC Generic Specification No. 9000*, Issue 8, February 2016. Available: https://escies.org

[4] Saphyrion Sagl, *SY1007 GNSS RF Front-End Datasheet*, Literature No. DS-SY1007, Rev. 1.4, 31 January 2014.

[5] Saphyrion Sagl, *SY1017C AD/DA-Converter Datasheet*, Literature No. DS-SY1017C, Rev. 1.5, 30 January 2014.

[6] ESA/ECSS, *Space product assurance, Electrical, electronic and electromechanical (EEE) components*, ECSS-Q-ST-60C, Rev. 2, October 2013.

[7] ESA/ECSS, *Space engineering, Methods for the calculation of radiation received and its effects, and a policy for design margins*, ECSS-E-ST-10-12C, November 2008.

[8] ESA/ECSS, *Space engineering, Calculation of radiation and its effects and margin policy handbook*, ECSS-E-HB-10-12A, December 2010.

Table 2: Summary of measured results.

Parameter	Conditions	Value	Unit	Notes
DiReRa RF front-end				
LNA gain	High gain setting	18.3	dB	Noise matched, 50Ω.
	Low gain setting	6.5	dB	
LNA noise figure	High gain setting	1.7	dB	Noise matched, 50Ω.
	Low gain setting	2.3	dB	
RF mixer SSB voltage gain	Balanced input, 50Ω	14.7	dB	Balanced output, unloaded.
RF mixer SSB noise figure	Balanced input, 50Ω	12.3	dB	
IF-strip overall gain range	TIF output	23.5 to 81.6	dB	PGAs+VCA, balanced I/Os, unloaded.
IF-strip PGA gain step		1	dB	Balanced I/Os, unloaded.
IF-strip VCA gain range	VC = 0V to 2V	12	dB	Maximum gain is limited.
Output 1dB compression point	PMS output, unloaded	−4.5	dBu	Referred to 600Ω.
DADC 1-bit AD-converter				
Sampling frequency	Maximum	130	MHz	Operates from ≈0Hz to 130MHz.
DC-offset	Input referred	±3.7	mV	Measured at DC, 2 samples.
0-1 imbalance	−4dBu, −40 to 125°C	0.5	%	Band-limited AWGN.

High Resolution Radiation Hardened DAC in CMOS-SOI Featuring a Return-To-Zero Matrix

M. Karaolis[a] , A. Stafylidis[a] , O. Dokianaki[a] ,
K.Papathanasiou[a] , K. Makris[a], D. Fragopoulos, C. Papadas[a] , B. Glass[b]

[a]I.S.D. S.A.32 Kifisias Av., Atrina Center, Building B, 15125, Marousi, Greece
[b]European Space Research and Technology Center – Microelectronics Section (TEC-EDM),
Postbus 299, 2200AG Noordwijk, The Netherlands

kmakris@isd.gr, dfragop@isd.gr, mkara@isd.gr, astafylidis@isd.gr, dokianak@isd.gr,
kpapatha@isd.gr, papadas@isd.gr, boris.glass@esa.int

Abstract

We present a current-steering, low-noise, radiation hardened Digital-to-Analogue converter, optimized to operate in the frequency range between DC and 50kHz. The DAC receives 24-bit sampled data in a synchronous serial format and converts it into a differential current analog signal. It uses a third-order multi-bit Sigma-Delta modulator, which provides superior noise and linearity performance. The embedded interpolator follows a multiple-stage architecture and consists of an FIR equiripple low-pass filter followed by two cascaded stages of Half-band equiripple filters. The last stage is a programmable SINC filter, which provides variable interpolation ratios allowing sampling rates as high as 310kHz. The system operates on a single clock domain, which is provided externally. The output current matrix features a Return-to-Zero (RTZ) technique to improve the linearity by ensuring that each elementary current source is zeroed, regardless the data value of the sample sequence. The DAC is implemented in a rad-hard 150nm CMOS-SOI process, exhibits an SNR figure of better than 108dB, and consumes 62mW of power.

I. INTRODUCTION

Digital-to-Analogue (DAC) converters based on ΣΔ modulation are excellent alternatives to conventional current steering architectures, especially for low frequency applications. ΣΔ DACs are based on digital shaping of the quantization noise to the high frequency end of the spectrum, where it is suppressed by means of analog filtering. The work presented here concerns the design of a high resolution, radiation hardened, 24-bit DAC, which continues the work presented in [18]. The device is designed with the ATMX150RHA 0.15 μm CMOS-SOI technology of Atmel® .The presented DAC aims at high-reliability instrumentation and control applications where high accuracy and low noise operation are required.

ΣΔ architecture is an attractive way of realizing high accuracy and low power data converters. Oversampling architectures with noise shaping of quantization error are suitable for low and medium speed applications when there is a trade off between accuracy and speed [10]. A loss in dynamic range occurs if 1-bit quantizer is used in order to guarantee stability of the loop. To overcome this problem a multibit quantizer with a high-order ΣΔ modulator is employed resulting in little loss of dynamic range. As the internal signal swing is reduced with the increase in number of bits, the multibit ΣΔ modulator requires a lower slew rate and thus less power for analog circuits than the 1-bit case. However, the overall resolution of the converter is determined by the internal digital to analog conversion linearity. To improve the accuracy of the internal DAC many techniques have been proposed and analysed [2]-[6].

II. SYSTEM ARCHITECTURE

A. Overview

The architecture includes an interpolation filter with a noise-shaping loop which are digital, while the output stages include an internal DAC and a reconstruction low-pass filter which are analog. The reconstruction filter and the I/V converter are realized externally to aid the design flexibility and device integration according to the target application's requirements. The system block diagram is shown Figure 1.

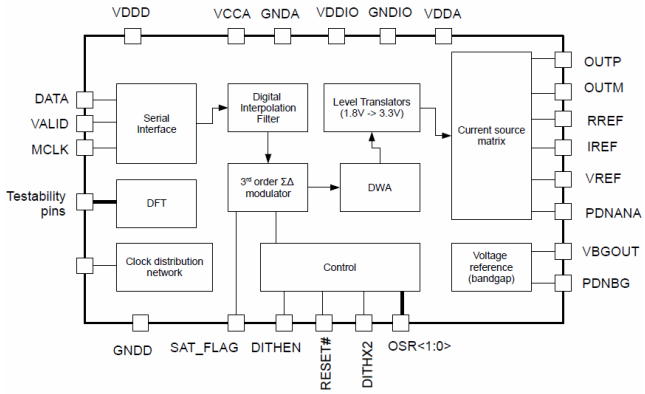


Figure 1: Block diagram of the DAC

B. *Digital Interpolator Filter*

The first block of the DAC is the interpolator. The digital signal interpolation is a fundamental operation to signal processing when a conversion between sampling rates is required. The interpolation stage can be considered as a combination of up-sampling and low pass filtering processes. Thus, the interpolation stage does not only increase the signal frequency by a factor of the Over-Sampling Ratio (OSR), but also has to suppress the image replicas. Many implementations have been reported for the realization of interpolators in the literature [7]-[10]. In this design, the interpolator is implemented efficiently using a multiple stage architecture. This reduces computational complexity, since a one stage implementation would result in a very high order filter. Typically, the order of a low-pass filter is a function of the required ripples δ_p and δ_s in the pass-band and stop-band respectively and inversely proportional to the normalized width of the transition band [11].

Finite Impulse Response (FIR) filters are preferred because they have linear phase response, which results in symmetric coefficients. The partitioning of the interpolation stage is shown in Figure 2.

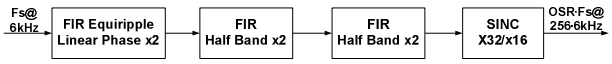


Figure 2: Multistage implementation of interpolator

The first stage is implemented using a 40th order FIR equiripple filter, whereas the second and third stage is implemented by a 30th and 18th order equiripple Half Band (HB) filter respectively. HB filters are FIR structures which allow every second tap weight except the central one to be zero and hence are very efficient in terms of implementation. Moreover, their pass-band and stop-band ripples are the same and their cut-off frequencies are symmetrical around π/2. The last stage is a second order Sinus Cardinal (SINC) filter, which offers variable Oversampling Ratios. The supported OSR values are x32, x64, x128 and x256 selectable through dedicated pins. The specifications of the filters are summarized in Table 1.

Filter Type	Upsampling factor	Fs	Pass-band frequency	Stop-band frequency	Pass-band ripple	Stop-band attenuation	Order of filter
Equiripple	x2	12 kHz	1 kHz	3 kHz	0.0001 dB	130 dB	44
HB equiripple	x2	24 kHz	3 kHz	9 kHz	0.00001 dB	130 dB	30
HB equiripple	x2	48 kHz	3 kHz	12 kHz	0.00001 dB	130 dB	18

Table 1: Specifications of interpolation filters

Each of the first three filters perform x2 interpolation and are implemented using a Multiply-Accumulator (MAC) architecture and polyphase decomposition which is described hereinafter. The transfer function H(z) of the filter can be expanded as shown in (1):

$$H(z)=\sum_{n=-\infty}^{\infty}h(n)z^{-n}=\sum_{n=-\infty}^{\infty}h(2n)z^{-2n}+\sum_{n=-\infty}^{\infty}h(2n+1)z^{-2n-1} \quad (1)$$

By defining the polyphase component filters as follows:

$$E_0(z)=\sum_{n=-\infty}^{\infty}h(2n)z^{-n}$$
$$E_0(z)=\sum_{n=-\infty}^{\infty}h(2n+1)z^{-n} \quad (2)$$

where $E_0(z)$ and $E_1(z)$ are the polyphase components of the decomposition, (1) can be re-written as the sum of the odd and even terms:

$$H(z)=E_0(z^2)+z^{-1}\cdot E_1(z^2) \quad (3)$$

Using the Noble identity [13], it is possible to reverse the order of upsampling and filtering as shown in Figure 3.

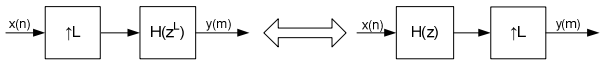


Figure 3: Illustration of Noble identity

Finally, the overall structure can be simplified by using a switch as shown in Figure 4 operating at the high frequency, whereas the polyphase components operate at the low frequency signal resulting in computational and power cost savings.

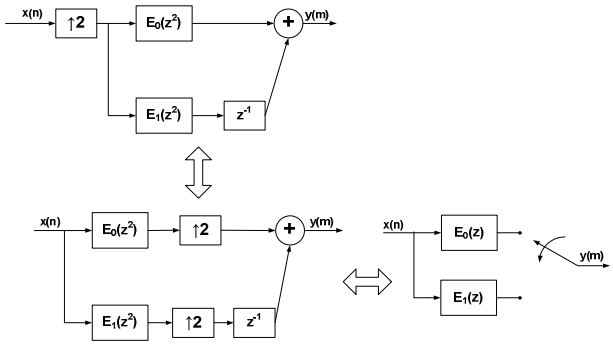


Figure 4: Polyphase implementation

C. *ΣΔ modulator*

The ΣΔ modulator is a fundamental component of the DAC. Several architecture considerations must be taken into account for determining the modulators characteristics, in order to achieve the desired SNR. An important design

decision is the resolution of the quantizer. Single bit modulators have the advantage of inherent linearity, low complexity and low implementation cost. On the other hand, multi-bit modulators exhibit better dynamic performance and overcome some stability problems associated with single bit modulators, provided that the appropriate architecture is chosen. They also introduce a reduced amount of quantization noise. For these reasons Multi-bit modulators are usually preferred [11], [14]. For low orders of modulation, error feedback and error feed-forward structures are preferred while for higher orders, Multi-stAge-noise-SHaping (MASH) architectures are generally used [11],[14]. Equation (4) associates the order (L) of the modulator, the resolution (B) the oversampling ratio (OSR) and the desired Signal-to-Noise Ratio.Equation (4) indicates that in order to achieve the desired Signal-to-Noise Ratio (SNR) the order (L) of the modulator, the resolution (B) of the quantizer and the Oversampling Ratio (OSR) should be increased.

$$SNR_{dB} = 10\log_{10}\left[\frac{3}{2}(2^B-1)^2\frac{(2L+1)OSR^{2L+1}}{\pi^{2L}}\right] \qquad (4)$$

A third order feed-forward ΣΔ modulator with a 5-bit internal quantizer was chosen. The initial sampling frequency is specified at 6 kHz and the OSR at x256, assuming the nominal clock frequency of 1.536 MHz. The input signal can be sampled up to 48 kHz when the OSR is adjusted to x32.

The most important design consideration for realizing a high order ΣΔ modulator is the feedback loop stabilization. For high order loops, stability considerations can reduce the achievable resolution to a lower value than that given by (4). In a third order ΣΔ topology, the Noise Transfer Function (NTF) H(z) is given in (5):

$$H(z) = (1-z^{-1})^3 \qquad (5)$$

Proper modulator operation is assured, if the loop filter remains linear and if the internal quantizer is not severely overloaded. A multibit internal DAC greatly relaxes the stability problem. The first criterion is to ensure that the closed-loop is stable according to the linear systems theory. Since the Signal Transfer Function (STF) is a pure time delay, stability is guaranteed. The second criterion is to ensure that the level of the input signal x(n) does not overload the quantizer. Considering a quantizer with M-step, (M+1) level, the modulator does not experience overload for any input u(n) [14] such that:

$$\max|u(n)| \le M + 2 - \|h\|_1 \qquad (6)$$

where:

$$\|h\|_1 = \sum_{n=0}^{\infty}|h(n)| \qquad (7)$$

and h(n) is the inverse z-transform of H(z) given in (5).

An other aspect of the ΣΔ architecture requiring attention is the generation of idle tones caused from the periodic output patterns at the output of the modulator. The linear noise model of the quantizer is valid only under specific conditions (large and random variations) on the input of the quantizer, which can be satisfied, if the input to the loop meets similar conditions. This means that the modulator under DC excitation or with very low frequency signals may produce periodic patterns, which give rise to idle tones. In practice DC patterns occupy few levels when the input is small. Under these conditions the behavior of multibit ΣΔ architectures is similar to that of a single bit ΣΔ modulator. To break the tones a pseudo-random 19-bit signal produced by a 35-bit Linear Feedback Shift Register (LFSR) is used. Assuming that the random signal to be introduced has a white noise type spectrum, then the most suitable place to add the dithering signal is just before the quantizer. The reason for adding it at this location is that the dithering becomes noise-shaped and thus a large amount of dithering can be added with negligible SNR degradation. The noise power of the dithering signal is similar to the quantization noise power. For assuring stability (8) should be satisfied [14]:

$$\|x\|_\infty \le 1 - \frac{1}{M}\left(1+\frac{\delta}{\Delta}\right)\|h\|_1 \qquad (8)$$

where δ and Δ is the amplitude of the dither and the input signal respectively, $\|x\|_\infty$ is the input maximum peak value, M corresponds to the quantizer steps and $\|h\|_1$ is given in (7). The output of the modulator is normalized to 1 in the previous equation. The time domain and frequency response of the output of the modulator are displayed in Figure 5 and Figure 6 respectively for a sinusoidal input of 750 Hz.

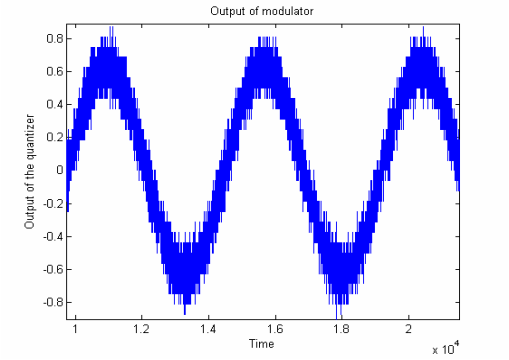


Figure 5: Output of the modulator with dither

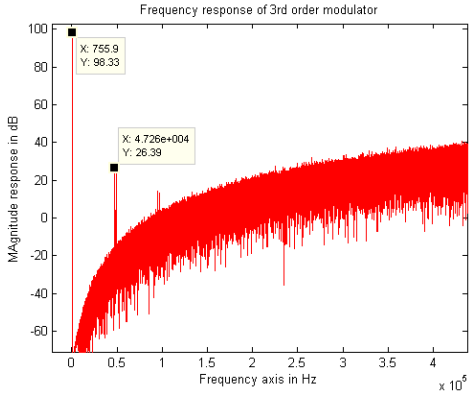


Figure 6. Frequency response of the modulator

D. *Dynamic Element Matching*

The use of a multibit ΣΔ modulator implies the use of an internal multibit DAC. This component, whether it is implemented with resistors or capacitors, exhibits non-linear transfer characteristics with respect to DNL and INL, due to element mismatch. There are two different architectures for the implementation of the DAC: the binary weighted code and the thermometer code. Both architectures offer a trade-off between the DAC's linearity, mismatch error, complexity and area overhead.

Binary weighted topologies have very small complexity, and can be applied to DACs with high resolution. Their disadvantage is the non-linearity of the output caused by unwanted glitches when big transitions happen in the current sources. This affects strongly the DNL performance.

Thermometer code topologies, on the other hand, overcome the differential non linearity problem. The price paid for them is the large area consumed by the sources and the extra decode logic on the digital part of the DAC.

Output linearity is one of the basic DAC features, therefore thermometer code architecture is preferred. In order to avoid element mismatch, which can severely degrade the static performance, different Dynamic Element Matching (DEM) algorithms were studied.

One of the most efficient algorithms to implement DEM is the Data Weighted Averaging (DWA) technique, which is applied in this DAC [1]. Unlike other techniques, which are based in the random element selection, DWA follows a cycled rotation approach. The algorithm's purpose is to achieve in long-term, an equal usage of the elements and, since the mismatch error is a random variable, the mean value is zero. Table 2 displays an example of the DWA algorithm applied to seven elements.

Time	Input	Index	1	2	3	4	5	6	7
1	5	1	•	•	•	•	•		
2	6	6	•	•	•	•		•	•
3	3	5					•	•	•
4	5	1	•	•	•	•	•		
5	2	6						•	•
6	3	1	•	•	•				
7	6	4	•	•		•	•	•	•
8	5	3			•	•	•	•	•
9	5	1	•	•	•	•	•		

Table 2. DWA algorithm example

The advantage of the DWA algorithm is that it uses only one index, which is updated with the addition of the input at every clock cycle

III. ARCHITECTURE OF THE ANALOG PART

A. *Description*

The 32 bit output of the DWA block drives the current sources in the analog section. The output of each analog sub-block of the DAC is the current summation of the 32 elementary current sources in a common node. Figure 7 shows the architecture of the analog part.

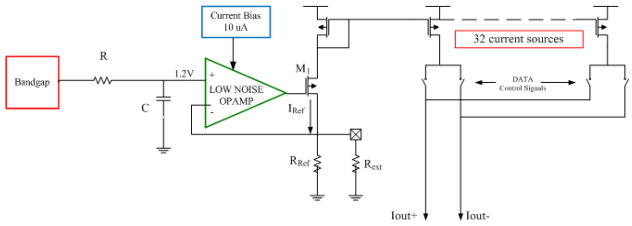


Figure 7. Architecture of the analog part

The components of the analog part of the DAC are a bandgap block, an RC low pass filter, a low-noise operational amplifier (OPAMP) and a current matrix consisting of 32+32 PMOS differential current sources.

The purpose of the bandgap block is to provide an accurate and temperature insensitive voltage output, which is then used as a reference point for generating and maintaining the reference current. The output voltage is 1.25V with a low temperature coefficient. The voltage reference is based on subtracting the voltage of a forward biased base-emitter junction PNP transistor having a negative temperature coefficient, from a voltage that is proportional to absolute temperature, which has a positive temperature coefficient. The noise of the bandgap block is decreased with the addition of a series RC low pass filter.

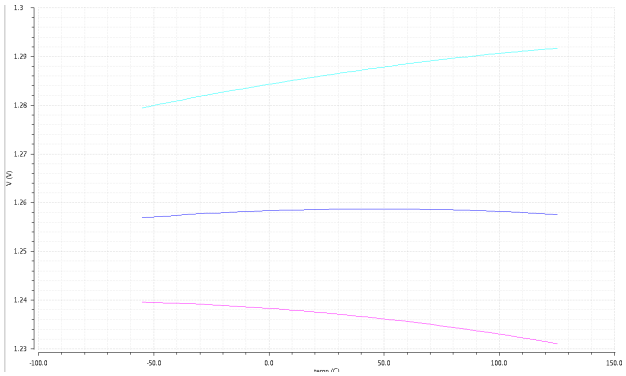


Figure 8: Bandgap output versus temperature at FF -55C 3.6V, SS 125C 3V and TYP 25C 3.3V conditions

The purpose of the operational amplifier is to fix the reference current I_{REF} across transistor M_1. The amplifier senses the voltage drop across the resistor RREF and fixes the I_{REF} by biasing the transistor M_1. RREF is an integrated resistor used to set the reference current value. As an alternative option, this resistor can be bypassed and an external component of different value can be used instead. This approach has the advantage of selecting the maximum value of the sourced current and consequently determining the power drawn from the analog supply. The OPAMP is a two-stage implementation consisting of a first differential stage followed by a push-pull output stage. The amplifier has an open loop gain of 85 dB, a phase margin of 60 degrees, a gain margin of -11.7 dB, and 42 dB Power Supply Rejection Ratio (PSRR). The amplifier is biased by a 10 uA current, generated internally.

The elementary current source cells used in the DAC,

are the basic components of the analog part. Each current source steers 198.1uA of current, resulting in a full-scale output of 6.34mA when all the 32 elements are on. In order to achieve good linearity figures, the elementary current sources should be well matched. In this implementation, we followed a centroid and symmetrical matrix layout by using an arrangement of spare and dummy cells. For the implementation of the current sources, the Regulated Cascode Topology is used as illustrated in Figure 9 [16].In this topology, the M_2 transistor is kept stable in order to have high overall output impedance against channel length modulation. To keep the transistor stable, a feedback loop is used consisting of an amplifier (M_3 and M_4) and M_1 acting as a follower. The use of oversized PMOS transistors, results in lower flicker noise and high linearity [17].

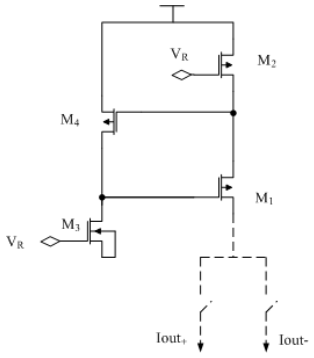


Figure 9. Regulated Cascode Topology

B. *Return-to-Zero Matrix*

The objective of the functionality is the current output to exhibit an RTZ characteristic for each sample. The adapted technique to achieve this is based on splitting the entire CS matrix into two equal and synchronized RTZ CS sub-matrices, with their outputs tight together in a common summing node. The expected advantage of this scheme is the adequate suppression of the harmonic distortion products at the output [20]. Both matrices are driven with the same data; the first one (denoted as LEFT 'o_out_L') contributes to the output during the first half period of the clock cycle while the second one (denoted as RIGHT 'o_out_R') contributes during the second half period. This is graphically represented in Figure 10.

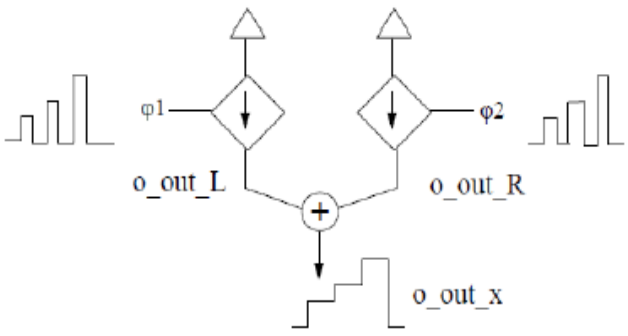


Figure 10: RTZ CS architecture

This functionality implies the utilization of two synchronized anti-phase clocks (φ1, φ2), each one dedicated for each sub-matrix . The two phases can be derived from the main clock input with φ1 to trigger the L matrix, and φ2 to trigger the R matrix. This scheme permits the two matrices to operate in a complementary fashion for each sample.

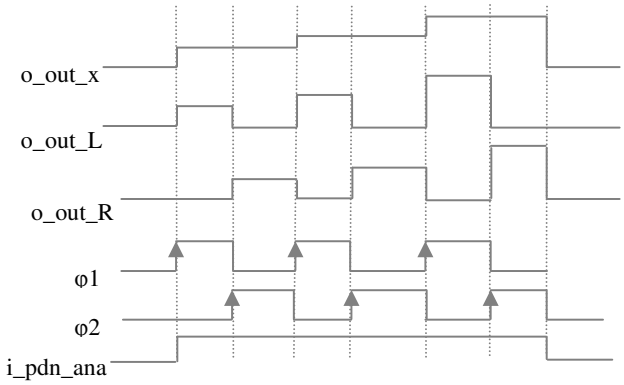


Figure 11 : RTZ Timing Diagram

The entire matrix consists of two thermometer coded sub-matrices, each one composed of 32 equal elementary differential CS cells.

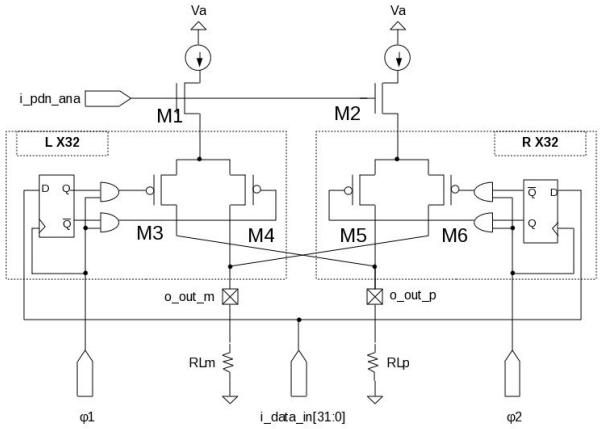


Figure 12: CS matrix simplified schematic

The positive and negative polarities are tied together in the common summing nodes denoted as 'o_out_p' and 'o_out_m' respectively. This yields to a single differential current steering output. The switches of each elementary CS (M3-M4, M5-M6) are driven in a complementary fashion from a common flip-flop and generate the differential polarities. The Left flip-flop (L) is clocked from φ1 while the Right flip-flop (R) is clocked from its complement φ2. The data line is common for both sub-matrices.

Each flip-flop output passes through an AND gate with its corresponding phase clock signal to guarantee, that when L branch is active, R is completely disabled and vice-versa. The 'i_pdn_ana' signal has a global power down effect, as it blocks the current path from the analog power supply rail Va via switches M1, M2.

IV. ON THE PROCESS FLOW

A. *Analog Part*

The analog part of the design has been processed separately, in order to obtain the analog physical views (cds.lib) that were used in the top design flow. For each cell of the analog part, we run the following steps. Firstly, the schematic of the cell is created by using the Virtuoso Schematic Editor XL™ tool. Then, a set of tests, in a wide range of process, voltage and temperature (PVT) corners, is run to ensure the correct functionality of the resulted schematic. Cadence Spectre™ simulation platform is used. In a next step, the layout is generated by using the Virtuoso Layout XL™ tool. The physical design implementation is done according to the predefined rad hard design rules. A set of checks is done that concerns LVS (layout versus schematic), DRC (design rule checking) and ARC (antenna rule checking). This physical verification is done by the Assura™ tool.

As soon as the processing for all the cells has been completed, an equivalent process flow is run for the analog top part. The first step is to generate the analog top schematic and then, a set of tests is run to ensure the correct functionality (Spectre tool). After having generated the analog top layout (Virtuoso Layout XL), a set of checks is done concerning LVS, DRC and ARC. In the next step, the calculation of the parasitic effects in the design (parasitic extraction) is done by using Assura RCX tool. The final step concerns the post-layout simulations by using the Spectre tool.

B. *Digital Part*

The digital part of the design has been processed separately, in order to obtain the GDSII file to be used in the top design flow. Starting from a verified RTL (written in VHDL), the design is synthesized by using the Design Compiler™ tool. The RTL is translated to gates from ATMX150RHA-MAX+MIL+NLDM library. In the same step, the scan chain is inserted in the design (DFT). The results of these steps are a netlist and a corresponding SDC (Synopsys Design Constraints) file. Post-synthesis verification (Modelsim™), static-timing analysis (Primetime™) and functional equivalence (Formality™) are run by using this netlist and SDC, in order to ensure the correctness of the synthesis.

The next step of the process flow concerns the physical implementation. In Encounter™ tool, we have performed: routing of special nets-power supplies, placement of the cells and spare cells, clock tree synthesis, routing of the design, filler insertion, geometry/connectivity/timing verification, extraction of GDS/netlist. One more step is needed for our design concerning some manual corrections in the layout, to anticipate from errors appearing in Virtuoso during top design flow, but not existing as issues in Encounter). The final GDSII is used in the next step of the process flow.

V. RADIATION HARDENING

The DAC is implemented in the single-poly, 5-metal, 0.15μm CMOS on SOI radiation hardened process of Atmel. The digital part is synthesized using the robust cells from the library, including latches and flip-flops with increased area. Triple Modular Redundancy (TMR) is used for every flip-flop and finite state machine along with voting scheme, as a highly effective fault tolerance technique in masking Single Event Effects (SEE). As an added measure, the reset is synchronized with the clock.

The analog part is hardened using relaxed layout rules, guard rings and extensive use of enclosed layout NMOS transistors (ELT). ELT transistors can greatly improve the analog degradation due to TID effects, which can be caused by radiation induced charge trapping in the oxides or at the Si interface [19]. The layout is almost totally immune to Single Event Latch-up (SEL) thanks to the deep trench isolation option (DTI). Each CMOS structure is isolated using a deep trench extending down to the buried oxide of the SOI, as shown in Figure 13. This arrangement cuts away the parasitic SCR devices inherently present in the CMOS structure that may trigger SEL events. The target LET for SEL immunity is greater than 70 MeV/mg/cm^2. The target figure for TID tolerance is 100 krad (Si). Hardening against Single-Event Transient effects (SET) is achieved by placing capacitors of the appropriate size to every sensitive analogue node. The value of each capacitor is optimized for each node through time domain SET simulations.

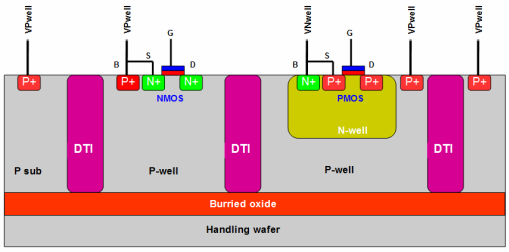


Figure 13: layout cross-section

VI. IMPLEMENTATION & SIMULATION RESULTS

The total area including the core and the I/O pads measures 17.5 mm^2. (x:3.5mm, y:5mm). All the capacitors in the signal path are of MIM type. In Figure 14 the floorplan of the chip is shown.

The dynamic performance of the SDM was evaluated by running post layout transient simulations in Spectre™. Figure 15 shows the output current when the 32 current sources open in sequence. Each current source steers 198.15 μA, which corresponds to a full scale current of 6.34 mA when all 32 sources are open. In the figure, point 1 shows the negative output, while point 2 shows the positive one. Points 3 and 4 corresponds to 32 open sources, while points 5 and 6 to 0 open sources. In the part of point 7, the master clock is shown. Finally, the input thermocode is shown at point 8.

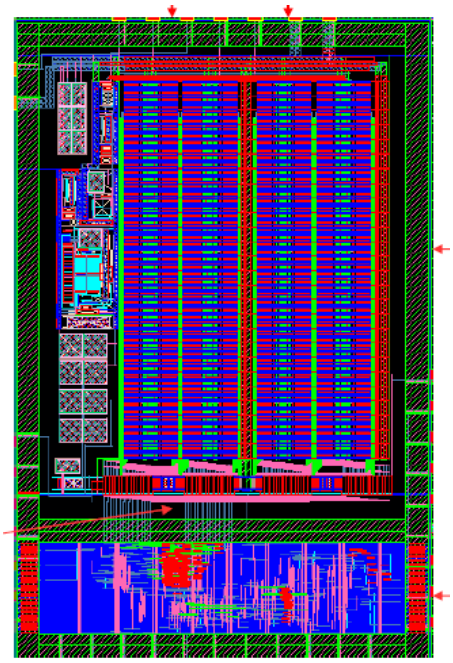


Figure 14: DAC chip floorplan

Table 3 summarizes the characteristics of the DAC obtained after simulation. The radiation tolerance limits are attributed to the target specifications.

Specifications	Value
Dynamic Range	> 108dB
Signal-to-Noise Ratio	> 108 dB
Sampling rate	Up to 310 kSps
Monotonicity	Full code range
Power dissipation	62 mW
LET for SEL immunity	$\geq$ 70 MeV/mg/cm^{-2}
SEU immunity	Protection of critical memory cells
SET immunity	Protection of the digital part
TID tolerance	$\geq$ 100krad
Temperature range (functional)	-55 °C < T < 125 °C
Temperature range (full performance)	0 °C < T < 50 °C

Table 3: DAC Performance summary

VII. CONCLUSION

The design of a high resolution ΣΔ DAC has been presented. The DAC is designed to exhibit more than 108 dB of SNR over its entire analog bandwidth while remaining tolerant to space radiation. The chip validation in silicon will demonstrate how closely the theoretical performance limit could be reached by this DAC, and will evaluate the effectiveness of the RTZ feature in terms of dynamic performance.

VIII. REFERENCES

[1] Dynamic element matching for high accuracy monolithic D/A converters, Van de Plassche, R. J., IEEE Journal of Solid-State Circuits, Volume 11, Issue 6, pp. 795–800, Dec. 1976.

[2] F. Chen and B. H. Leung: A High Resolution Multibit Sigma-Delta Modulator With Individual Level Averaging, IEEE Journal of Solid-State Circuits, Volume 30, Issue 9-11, pp. 101–102, Jun. 1994

[3] R. T. Baird and T. S. Fiez: Linearity enhancement of multibit ΔΣ A/D and D/A converters using data weighted averaging, IEEE Transactions on Circuits and Systems II,Volume 42, Issue 12, pp. 753–762, Dec. 1995.

[4] An audio ADC Delta-Sigma modulator with 100-dB peak SINAD and 102-dB DR using a second-order mismatch-shaping DAC, E. Fogleman, J. Welz, and I. Galton, IEEE Journal of Solid-State Circuits, Volume 36, Issue 3, pp. 339–348, Mar. 2001.

[5] A 2.5-V ΣΔ modulator for broadband communications applications, K. Vleugels, S. Rabii, and B.A. Wooley, IEEE Journal of Solid-State Circuits, Volume 36, Issue 12, pp. 1887–1899, Dec. 2001.

[6] Decimation for Sigma Delta Modulation, J. C. Candy, IEEE Transactions on Communications, Volume 34, pp. 72–76, Jan. 1986.

[7] A stereo audio sigma-delta A/D-converter, T. Ritoniemi, E. Pajarre, S. Ingalsuo, T. Husu, V. Eerola, and T. Saramaki, IEEE Journal of Solid-State Circuits, Volume 29, Issue 12, pp. 1514–1523, Dec. 1994.

[8] A Low-Power, area-efficient digital filter for decimation and interpolation, B. P. Brandt and B. A. Wooley, IEEE Journal of Solid State Circuits, Volume 29, Issue 6, pp. 679–687, Jun.1994

[9] A stereo audio chip using approximate processing for decimation and interpolation filters, C. J. Pau, IEEE Journal of Solid-State Circuits, Volume 35, Issue 1, pp. 45–55, Jan. 2000.

[10] Delta-Sigma Data Converters, Theory, Design, and Simulation by Steven R. Norsworthy, Richard Schreier, Gabor C. Temes, IEEE Press, 1997

[11] An economical class of digital filters for decimation and interpolation, E. Hogenauer, IEEE Transactions on Acoustics, Speech and Signal Processing, Volume 29, Issue 2, pp. 155–162, Apr. 1981

[12] Multirate Digital Signal Processing, R. Crochiere and L. Rabiner, Prentice-Hall, Englewood Cliffs, NJ, 1983.

[13] Understanding Delta Sigma Data Converters, Richard Schreier, Gabor C. Temes, Wiley-IEEE Press, 2004

[14] Data Converters, Franco Maloberti, Springer, 2007

[15] A high-Swing, high-Impedance MOS Cascode circuit, Eduard Sackinger, Walter Guggenbuhl, IEEE Journal of Solid-State circuits, Volume 25, Issue 1, pp. 289-298, Feb. 1990

[16] Yannis Tsividis, "Operation and Modeling of the MOS Transistor (Hardcover)", Oxford University Press, USA 2nd edition, june 26, 2003

[17] Adams R., Nguyen Q. K., Sweetland K., A 113-dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling, IEEE Journal of Solid-State Circuits, VOL.33, No.12, December 1998.

[18] D. Mitrovgenis, K.Makris, D.Fragopoulos, G.Tsiligiannis, C.Papadas, *On the Design of a Very High Resolution DAC at 1kHz for Space Applications,* Proceedings of the Second International Workshop on Analog and Mixed Signal Integrated Circuits for Space Applications (AMICSA), August – September 2008, Cascais/Sintra, Portugal, pg. 47 – 54.

[19] Faccio F., and Cervelli G., "Radiation-Induced Edge Effects in Deep Submicron CMOS Transistors", IEEE Trans. on Nuclear Science, Vol. 52, No.6, pp. 2413 – 2420, Dec. 2005.

ACKNOWLEDGMENTS

The authors would like to thank Mr. Michel Porcher (Atmel), Rok Dietrich and Richard Jansen (ESA) for their continuous support and valuable suggestions.

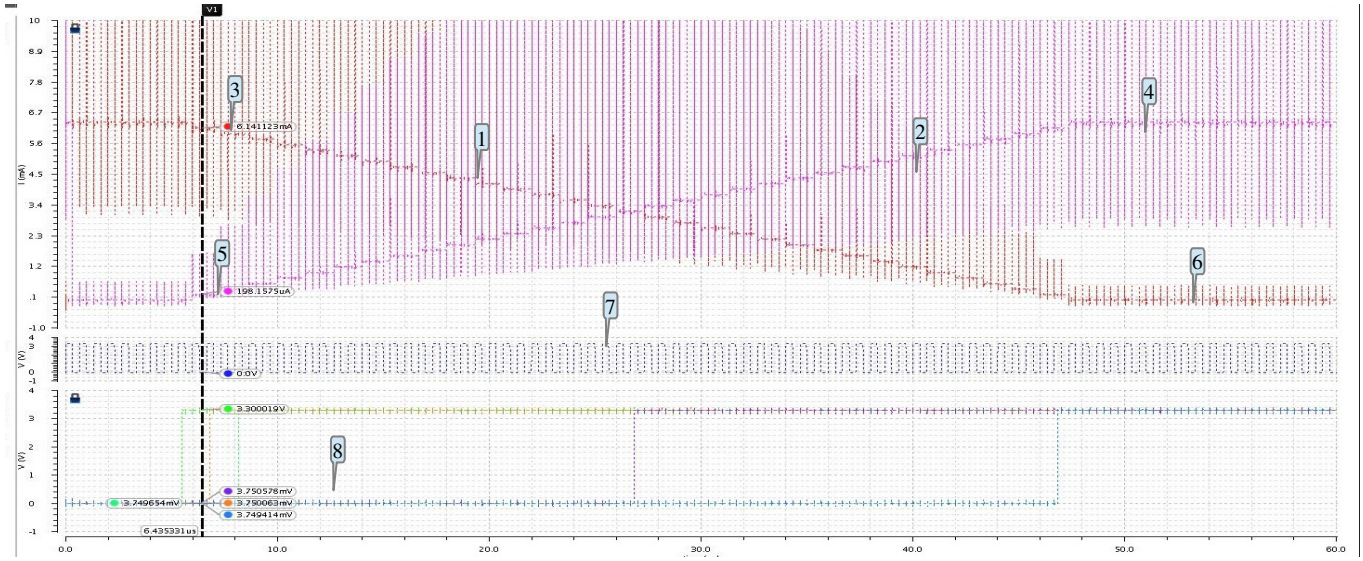


Figure 15: Differential Output Transient Simulation

AMICSA: Radiation-hardened technologies for analogue and mixed-signal ICs

Radiation-Hardened SiGe BiCMOS Technologies for Analogue and Mixed-Signal ICs

M. Cirillo[a], F. Teply[a], G. Fischer[a], R. Sorge[a], J. Schmidt[a], M. Krstic[a], V. Petrovic[a]

[a] IHP, Im Technologiepark 25, 15236 Frankfurt (Oder), Germany

cirillo@ihp-microelectronics.com

Abstract

There is a strong need in the Space market, where size, power and weight are a strong concern, for high performance microelectronic processes capable of integrating complex digital functions together with very high operating frequencies even into the THz range [1].

Silicon-Germanium (SiGe) Heterostructure Bipolar Transistor (HBT) devices are well known for their radiation tolerance [3] [4] [5] and their capability to perform in harsh environments [2].

The integration of SiGe HBTs into Bipolar-Complementary Metal Oxide Semiconductor (BiCMOS) technology platforms have proven a valuable technology for the design and implementation of highly integrated Microwave Monolithic Integrated Circuits (MMICs) and Application Specific Integrated Circuits (ASICs) operating at very high frequencies (into the THz range). Integration with low power complex CMOS functions and Emitter-Coupled-Logic (ECL) bipolar digital functions allows MMICs with unprecedented complex functionalities unavailable in other process (i.e. III-V) technologies.

I. Introduction

IHP provides un-restricted access for research and educational purposes as well as for commercial fab-less companies, to Process Design Kits (PDKs) on proprietary high-performance 0.25µm and 0.13µm SiGe-BiCMOS Technologies for prototyping through Multi-Project-Wafer (MPW) and Low Volume Production (LVP).

For the 250nm node, a Radiation Hardened (RH) PDK SGB25RH has been developed and evaluated in accordance to the ESCC-2269010 Basic Specification "Evaluation Test Programme for MMICs" and requesting EPPL listing ,while for the 130nm, PDK SG13RH is presently completing radiation testing (TID, DD, SEEs) in accordance with ESCC-2269010. EPPL for SG13RH can be foreseen within 2020.

The RH PDKs provide tested library elements where Radiation Hardened by Design (RHBD) techniques at layout, circuit and architecture level to the standard commercial processes have been implemented. For example, Enclosed-Layout-Transistor (ELT) for N-Channel MOS devices are available as well as special layout designs for the CMOS library memory elements, i.e. D-Flip-Flops (DFFs) and known DICE FFs.

II. IHP SiGe BiCMOS Technologies for Space

The proposed processes have completed commercial qualification derived from JEDEC JP001.1 for Level-2 Technological Qualification which includes Device Reliability Tests (CMOS+HBT) and Intrinsic Reliability Tests.

Table 1 and Table 2 summarize the Process and Standard-Cell Digital Library options of the offered SiGe BiCMOS Technologies by IHP. In addition both processes include a range of passive devices like Poly-Si resistors, Metal-Insulator-Metal (MIM) capacitors, MOS varactors and other.

Table 1: SGB25RH PDK Process and Library Options

Features	**SGB25V / SGB25RH**
Backend (BEOL)	5 Layer Al incl. 2 µm and 3 µm thick metal layers (TM1, TM2)
Bipolar ($f_T/f_{MAX}/BV_{CEO}$)	High-speed HBT : 75 GHz / 95 GHz /2.4 V Medium Voltage HBT : 45 GHz / 90 GHz / 4.0 V High Voltage HBT : 25 GHz / 70 GHz / 7.0 V
CMOS	Vdd = +2.5 V T_{OX} = 5.8 nm
CMOS Digital Standard Cell Libraries	SESAME-LP2 Dolphin Library + Rad-Hard Library extension elements (~ 70 cells) (TMR-FF, DICE-FF) SAPHYRION SAGL Standard Cell Library (~25 cells)
CMOS Digital Standard Cell IO Cells	SESAME IO Pads +2.5 V IHP25 RH +3.3 V IO Pads

Table 2: SG13RH PDK Process and Library Options

Features	**SG13S / SG13RH**	
Backend (BEOL)	7 Layer Al incl. 2 µm and 3 µm thick metal layers (TM1, TM2)	
Bipolar ($f_T/f_{MAX}/BV_{CEO}$)	High-speed HBT : 250 GHz / 340 GHz /1.7 V High Voltage HBT : 50 GHz / 130GHz / 3.7V	
CMOS	Vdd = +1.2 V T_{OX} = 2 nm	Vdd = +3.3 V T_{OX} = 7 nm

Features	SG13S / SG13RH
CMOS Digital Standard Cell Libraries	IXC013 + Rad-Hard Library extension elements (~80 cells) (TMR-FF, DICE-FF)
CMOS Digital Standard Cell IO Cells	IO Pad Library (+2.5 V and +3.3 V)

III. Radiation Test Results

A. Total Ionizing Dose (TID) and Enhanced Low Dose Rate sensitivity (ELDRS)

1) HBT Devices:

Previous [5] [6] [7] TID and ELDRS measurements on SiGe HBTs were carried out at much higher dose rates and total doses, aiming at applications in high-energy physics. However for space-oriented applications, lower dose rates are required. MIL-STD-883 TM1019.8 calls out a dose rate of 50 to 300rad(Si)/s to ensure worst-case test conditions. Re-conducted tests on HBTs in SGB25RH show dependency of the Base-current and Forward Beta with respect to TID (Figure 1) to a tested dose level of 800krad(Si) while SG13RH HBTs do not show any substantial variation to TID (Figure 2) to a tested dose level of 1210krad(Si).

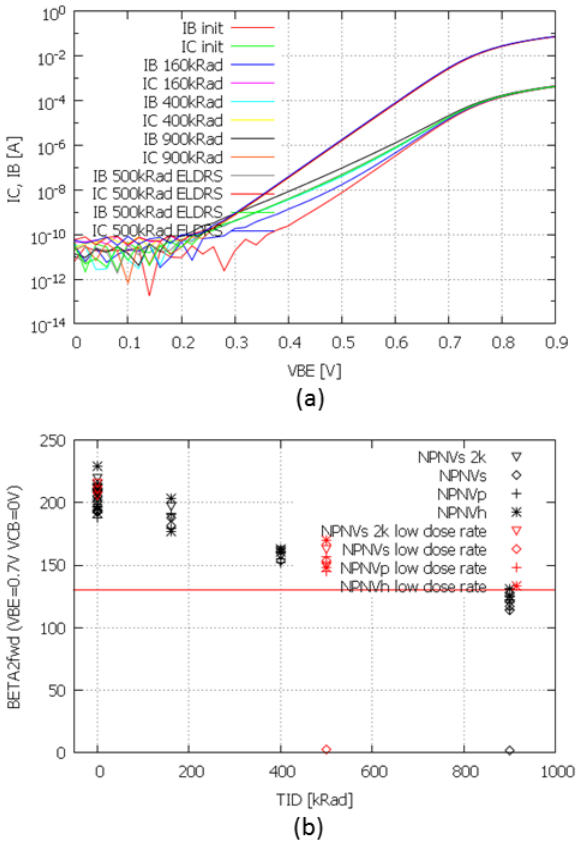


Figure 1: Forward Gummel plots (a) and forward current gain (b) for SGB25RH HBT devices (with emitter area of 1.06x1.48 µm^2) versus TID

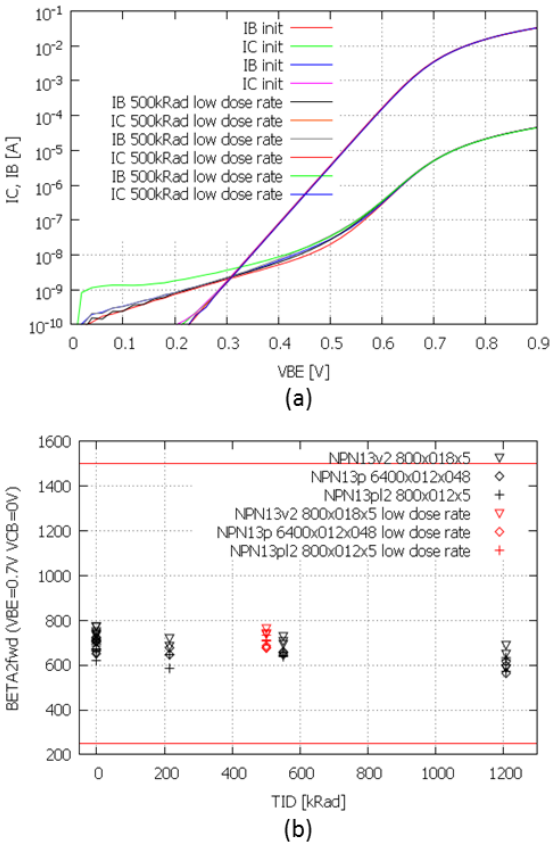


Figure 2: Forward Gummel plots (a) and forward current gain (b) for SG13RH HBT devices (with emitter area between 360 and 720 µm^2) versus TID.

2) CMOS Devices:

In modern CMOS technologies with gate oxide thicknesses <10nm the main TID effect is a strong subthreshold leakage current shift. TID-induced trapped charge accumulates in the trench oxide leading to inter- and intra-device leakage conduction paths. For the former case, accumulation of radiation induced positive charge in the shallow trench isolation oxide leads to parasitic corner devices with reduced (more negative) threshold voltage. For NMOS devices the parallel corner device leads to an increased leakage current.

PMOS devices in both technologies have been tested to a maximum total dose level of 500krad(Si) and exhibited no variations in their characteristics. For SGB25RH NMOS (Figure 3) and SG13RH LV-NMOS pass TID levels of up to 110krad(Si) for the devices used in the standard cell libraries. Leakage current remains within specification up to TID levels of 110kRad .

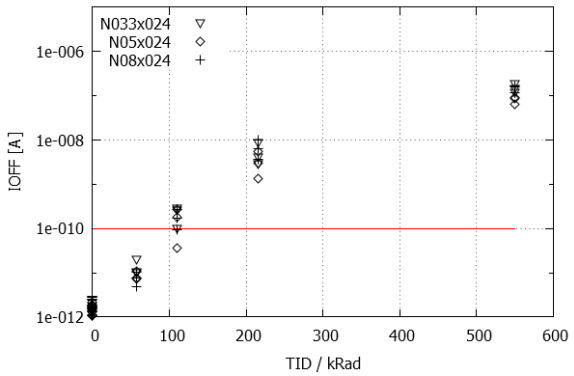


Figure 3: Leakage current IOFF versus total ionizing dose for SGB25V short channel NMOS DUTs with gate length L=0.24µm. Gate width is 0.33, 0.5 and 0.8µm. The red line is the pre- and/or post-irradiation maximum specification value as defined for the pass/fail parameter VTN024 in the SGB25V process specifications.

Annealing tests after irradiation showed a slight improvement after room temperature annealing (simulating low dose rate environments), accelerated annealing tests at 100°C showed no indication of Time Dependent Effects (TDE) (see Figure 4).

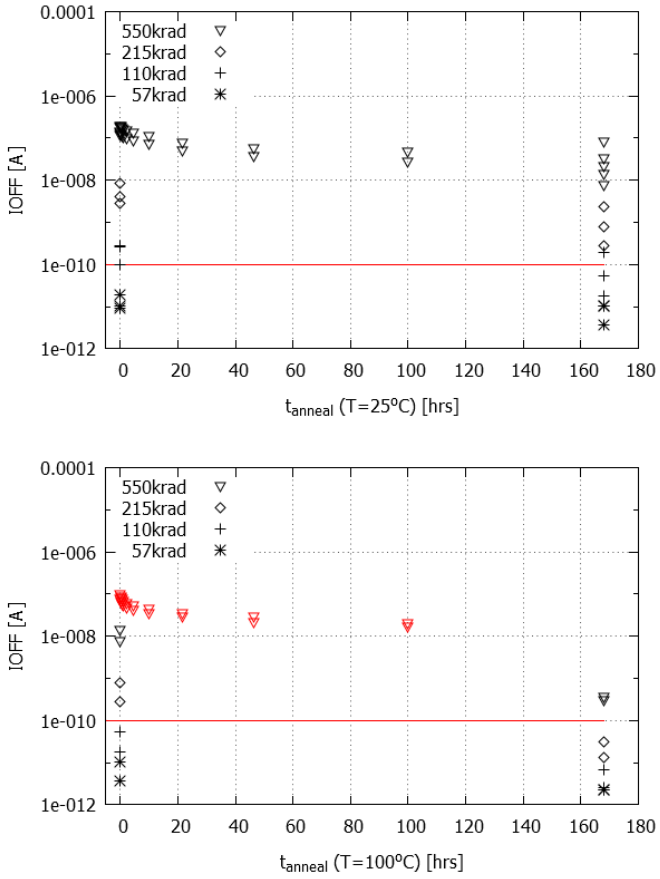


Figure 4: Leakage current IOFF for SGB25 NMOS versus annealing time for room temperature and high temperature accelerated anneal.

As expected the transfer characteristics for the Enclosed Layout (ELT) NMOS Transistor devices in SB25RH and SG13RH (Figure 5) exhibit very stable characteristics for TID well over 500krad(Si).

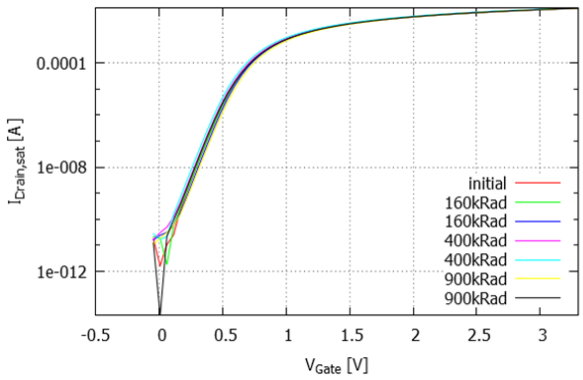


Figure 5: Transfer characteristic of the SG13RH ELT-NMOS (nELT033) high-voltage (HV) device in saturation (VDS=3.3V) before and after irradiation process for TID up to 900krad(Si).

B. SEL / SEU on CMOS Digital Standard Cell Libraries

Several Test Vehicles have been designed and tested under Heavy Ions (HI) for Single Event Latch-up (SEL) and Single Event Upsets (SEU) characterization. No SEL has been detected up to 65MeV/cm²/mg on the CMOS standard cell library elements. Achieved SEU LET thresholds and Cross-Sections on the different Flip-Flops (TMR, DICE, etc..) were measured on 1024-bit Shift Registers Test Vehicles and are shown in Figure 6 for SGB25RH. Similar curves are available for SG13RH.

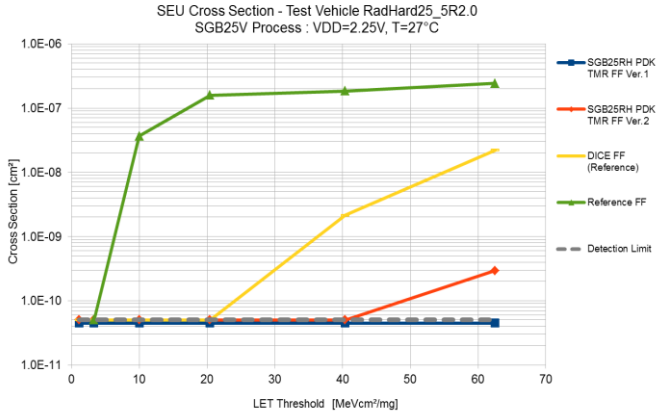


Figure 6: Heavy-Ion (HI) SEU test results on 1024-bit Shift Registers built around different Flip-Flops (TMR, DICE, etc..) for SGB25RH

IV. Status of ESCC Evaluations

A. SGB25RH

Rad-Hard PDK SGB25RH has been developed and has been evaluated in accordance to the ESCC-2269010 Basic Specification "Evaluation Test Programme (ETP) for MMICs" and will be requesting EPPL Listing in 2016 upon update completion of the Process Identification Document (PID) and Capability Domain (CD). Radiation tests (TID, ELDRS) have also been re-performed on the active devices to confirm the process and SEL/SEU characterization has been

completed on the digital standard cell libraries. Test Vehicles requested by ESCC-2269010 (TCV, DEC, RIC shown in Figure 7) have completed all Long Term Tests (LTT) as in Table 3.

Table 3: SGB25RH ESCC-2269010 ETP Test Summary

Test Vehicle	Long Term Test
TCV	4000h, 150°C – completed successfully with predicted degradations and expected failures during stress test
DECs	up to 3000h, 150°C and Room Temperature – completed with some failures due to EOS / ESD handling issues CMOS HCI degradation leading to lifetime estimation (~20 years / 300MHz / +2.7 V) HBT no degradation
RIC	4000h, 150°C – completed successfully with no failures

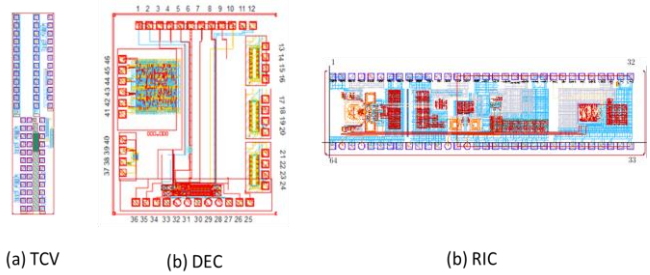


Figure 7: SGB25RH Test Vehicles (dies only) : Technology Characterization Vehicle (TCV) (a) consisting of standard technology test segments (HBTs, NMOS, PMOS, etc…), (b) Dynamic Evaluation Circuit (DEC) consisting of Shift-Registers, Ring-Oscillators, and VCO and (c) Representative Integrated Circuit (RIC) a 20 GHz VCO with integrated divider chain, 6 GHz RF Output and Serial to Parallel (SPI) Interface.

B. SG13RH

130nm Technology node, PDK SG13RH is under development and sensitivity to radiation (TID, DD, SEEs) is being completed on several Test Vehicles (including TCV and DEC) before continuing with the tests defined in ESCC-2269010 Evaluation Test Programme. Expected application for EPPL for SG13RH would be in the timeframe 2018/2020.

V. Conclusion

SGB25RH and SG13RH PDKs enable SiGe BiCMOS technologies for the development of MMIC/ASICs intended for space applications and harsh environments .

VI. Reference Publications

[1] A.Ç. Ulusoy, P. Song, W.T. Khan, M. Kaynak, B. Tillack, J. Papapolymerou, and J.D. Cressler, "A D-Band SiGe Low-Noise Amplifier Utilizing a Gain-Boosting Technique," IEEE Microwave and Wireless Components Letters, vol. 25, pp. 61-63, 2015.

[2] P.S. Chakraborty, A.S. Cardoso, B.R. Wier, A.P. Omprakash, J.D. Cressler, M. Kaynak, H. Rücker, and B. Tillack, "130 nm, 0.8 THz fmax, 1.6 V BVCEO SiGe HBTs Operating at 4.3 K," IEEE Electron Device Letters, vol. 35, pp. 151-153, 2014.

[3] N.E.Lourenco, Z.E.Fleetwood, S.Jung, A.S.Cardoso, P.S. Chakraborty, T.D.England, N.J.-H Roche, A.Khachatrian, D. McMorrow, et al., M.Kaynak, B.Tillack, D.Knoll, J.D.Cressler, „On the Transient Response of a Complementary (npn+pnp) SiGe HBT BiCMOS Technology", Vol. 61 n° 6 December 2014, IEEE Transactions on Nuclear Science.

[4] S.Díez, M.Ullán, M. Lonzano, G.Pellegrini, I. Mandic, D.Knoll, B. Heinemann, „IHP SiGe:C BiCMOS technologies as suitable solution for the ATLAS Upgrade Front-End Electronics",Vol. 54 n° 4 August 2007, IEEE Transactions on Nuclear Science.

[5] S.Díez, M.Ullán, M. Lonzano, G.Pellegrini , F.Campabadal, D. Knoll, B. Heinemann, „Gamma Radiation Effects on Different Varietes of SiGe:C HBT Technologies",Vol. 54 n° 4 August 2007, IEEE Transactions on Nuclear Science.

[6] S.Díez, M.Ullán, M.Lonzano, G.Pellegrini, F.Campabadal, D.Knoll, B.Heinemann, „Radiation hardness evaluation of SiGe HBT technologies for the Front-End electronics of the ATLAS Upgrade", A-579 (2007), Nuclear Instruments and Methods in Physics Research.

[7] S.Díez, M.Ullán, M.Lonzano, G.Pellegrini, F.Campabadal, I.Mandic, D.Knoll, B.Heinemann, „Proton Radiation Damage on SiGe:C HBTs and Additivity of Ionization and Displacement Effects",Vol. 56 n° 4 August 2009, IEEE Transactions on Nuclear Science.

Incorporating More In-Depth Radiation Knowledge in the DARE180U Analog Design Kit

S. Verhaegen[a], W. Sijbers[a], S. Zagrocki[a], L. Berti[a], J. Wouters[a], G. Franciscatto[a], G. Thys[a], S. Redant[a]
B. Glass[b], R. Jansen[b]

[a]imec, 3001 Leuven, Belgium
[b]ESA, 2200 AG Noordwijk, The Netherlands

staf.verhaegen@imec.be

Abstract

DARE180U is a radiation hardened system-on-a-chip (SoC) design platform including mixed-signal and full-custom analog circuits. It is built on the commercial UMC L180 MM/RF 1.8V/3.3V, Single Poly 6 Metal (1P6M), P-Sub/Twin-Well CMOS technology. DARE180U is a member of the DARE family of radiation hardened full-custom/mixed-signal design platforms with a portfolio that extends over several technologies. In order to facilitate mixed-signal/full-custom radiation aware analog design an analog design kit (ADK) is provided to the designer as an extension of the foundry provided PDK.
Over the years, radiation related knowledge has been extended and built up with design of and testing on test vehicles, prototypes and flight models. Based hereon, improvements have been made to the DARE180U ADK to reduce design effort in order to fulfill the radiation hardness specifications. In this paper an overview is given of these improvements together with the continuous learning on which they are based.

I. The DARE180U Mixed-Signal/Full-Custom Radiation Hardened ASIC Technology

DARE (Design Against Radiation Effects) is a family of radiation hardened full-custom/mixed-signal design platforms. With the focus on mixed-signal and full-custom ASIC development it allows the use of an IP-based SoC implementation flow where digital parts are combined with reusable mixed-signal IP-blocks and dedicated full custom designed blocks. It also supports full-custom analog-on-top ASICs. First work has already been done end of last century on UMC L180 MM/RF 1.8V/3.3V, Single Poly 6 Metal (1P6M), P-Sub/Twin-Well CMOS technology and is still continuing today under the DARE180U name. No end is in sight as the 0.18µm technology is a long running analog node. Due to the flexible set-up of the platform other technologies can be supported to fulfill specific requirements. So later-on also the companion UMC 0.18µm CMOS Image Sensor (CIS) technology (DARE180UC) was supported, the 0.18µm XH018 XFAB tech (DARE180X) with support for high-voltage BCD devices up to 40V and non-volatile memory and the 0.35µm On-Semi I3T80 with high-voltage BCD devices up to 80V. Currently DARE65T based on 65nm TSMC technology is started. This in order to be able to provide higher compute power at lower power consumption together with higher frequency analog performance. A more in-depth historical overview and discussion of the different technologies and an overview of the ASICs produced can be found on the latest DARE User Day Site[2].
To facilitate full custom design an ADK is provided. As longest running technology the DARE180U one has made an evolution together with the improved learning based on dedicated test-vehicles and lessons learned on completed projects. In the paper this evolution will be presented and the rest of the paper has the following structuring: in section II the first version of the DARE180U ADK will be described; in section III several results and continuous learning over the years will be described; section IV will discuss the improvements done based on this learning; section V presents some other topics that can be candidates for implementation in future ADK versions and section VI will then summarize the paper.

II. First DARE180U ADK

1) CERN W/L formula

Based on the original specs for TID level of 1Mrad and experimental transistor measurements it was decided to use enclosed-layout transistors (ELTs) for the NMOS transistors. Example layout can found in Figure 2. With this layout W does not correspond directly to the drawn dimension in the layout and the extracted W from the layout by the foundry provided deck does not match with the expected performance of the device. Therefor the W extraction was implemented with a formula based on a paper from CERN[1]. This formula computes the W/L as function of L and B & H, the width and height of the inner diffusion area of the ELT. Increasing L and keeping the B&H the same also increases W. This results in a leveling off of W/L reduction with increasing L. In the original ADK an excel sheet was provided where realizable W/L values can be looked up. Additionally this formula was implemented for schematic capture and in the parasitic extraction deck.

2) ELT p-cell and Verification Support

In the standard UMC technology library p-cell (parametric cells) for the devices are given. In order to allow the same design productivity in the DARE180U ADK p-cells are provided for ELTs.

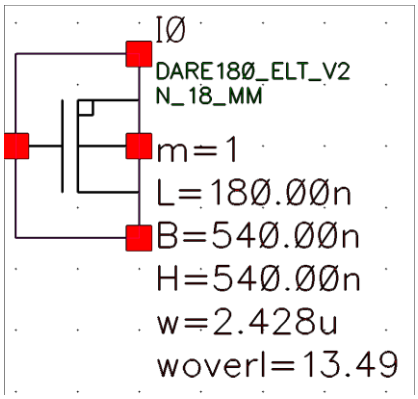


Figure 1: ELT p-cell symbol view instance

In Figure 1 an instance of the p-cell symbol view in a schematic is shown and in Figure 2 an instance of the layout view in another layout. When instantiating one of these p-cell views not the W is specified but B & H, the width and height of the inner diffusion area. Based on this, the W and W/L are computed with the formula as introduced earlier. The resulting values are shown in the schematic as reference. Additionally more correct estimates are done for the inner and outer diffusion perimeter and area so pre-layout simulation are closer to the post-layout simulation. For layout p-cell parameters are present that allow to choose on which side to put contacts in the outer area and at which side to put a P+ guardband.

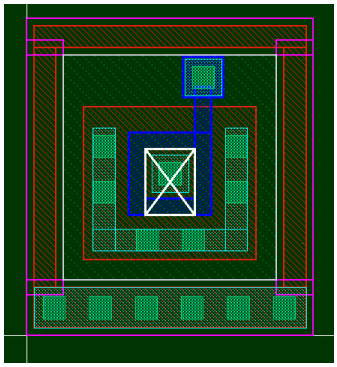
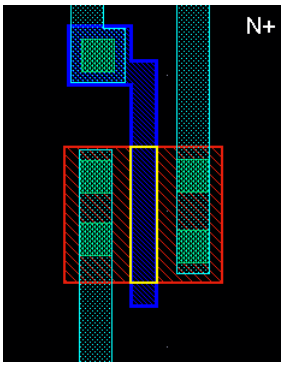


Figure 2: ELT p-cell layout view instance

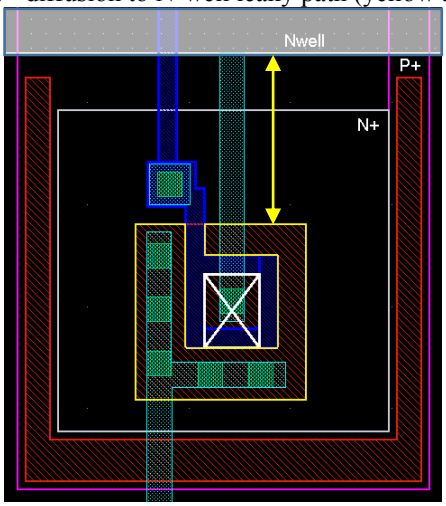
3) RAD check

In the first ADK an extra Calibre deck was provided to check for violations against agreed radiation mitigation rules. Following is a list with an example picture showing each of the rules:

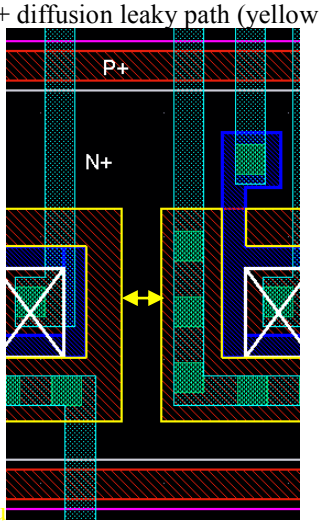
- Straight NMOS transsitor



- N+ diffusion to N-well leaky path (yellow arrow)



- N+ to N+ diffusion leaky path (yellow arrow)



III. Continuous Learning

Over the years several projects have been run using the DARE180U technology. Some of the projects included dedicated test-vehicles to increase knowledge on the radiation effects and mitigation, for other projects some ADK improvements were identified at the start and during the course of the project. The lessons learned in all the projects is also knowledge used as a guidance for ADK improvements. This section will summarize the learning for which improvements and extensions to the ADK have been implemented; section IV details the implementation in the ADK.

1) Latch-Up Mitigation

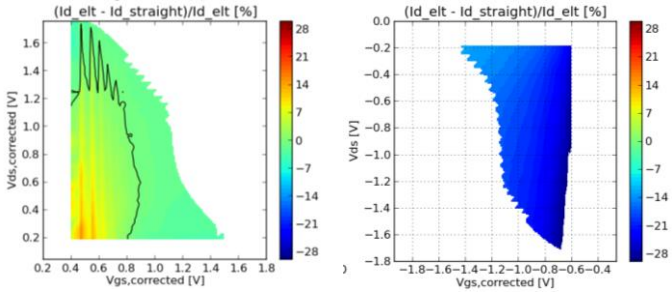
When using P+ guard bands in digital CORE and IO cells a good contact is made to the P-substrate. This prevents single-event latch-up (SEL); experimentally confirmed by never having seen a SEL on a DARE180U based ASIC. For analog designs, the use of big(ger) transistors, non-digital voltage levels and optionally triple-well devices could reduce the latch-up mitigation. For such cases extra rules may be wanted in addition to the default technology N-well and P-substrate contacting rules.

2) In-Depth Straight vs. ELT TID Experiments

In DARE+[3] - a follow-up project on the original DARE project - more in-depth measurements on unradiated and radiated test vehicles have been carried out. An overview of the ADK related results is discussed in this paragraph.

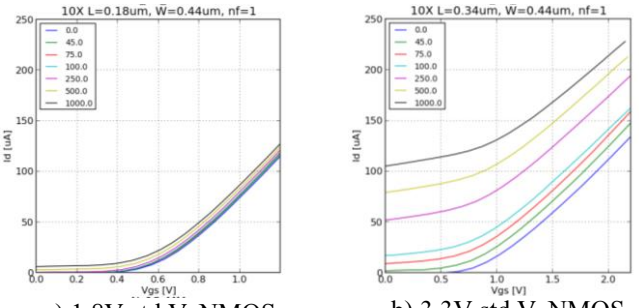
First the ELT W extraction as computed out of the W/L CERN formula is verified by comparing drain current between ELT and straight transistor with equivalent W. The measurements are done on the same die so process offsets are removed from the equation.

In Figure 3 the relative offset between the two is given, the equivalent W straight drain current is derived by interpolating results for a wider and narrower straight transistor. A black contour line is drawn where the drain current matches. For the given NMOS this is shown in the picture displaying reasonable agreement between the two, but for the PMOS the measured current on the ELT is always significantly lower than the equivalent straight transistor. The same trend is seen when looking at other device dimensions and the 1.8V, 3.3V, std. V_t & low V_t ones. The reason for this difference can have several causes and more work needs to be performed to fully understand this effect.



a) 1.8V std V_t NMOS b) 1.8V std V_t PMOS

Figure 3: Relative measured offset between straight and ELT with equivalent W



a) 1.8V std V_t NMOS b) 3.3V std V_t NMOS

Figure 4: measured TID induced leakage current for straight NMOS

Also measurements have been done at different TID levels for an extensive set of structures. In Figure 4 the I_d-V_{gs} curve for the straight NMOS transistor is shown; for a 1.8V device on the left and 3.3V device on the right. For the 1.8V device the curves are shifting in the Y direction as a function of the TID which corresponds with a leakage current that is only a function of TID. For the 3.3V device next to the much bigger shift in Y also a modulation by V_{gs} is seen in the sub-threshold area; meaning that this can't be represented with a leakage current being only a function of TID. In Figure 5 the extracted leakage current are given for 1.8V NMOS for different L & W values. Except for the narrowest device not much influence is seen of W on the leakage current; for L a maximum leakage current is seen around 0.7µm. Accurate measurement of the smaller currents can take quite a long time and due to the limited time window available for measurement during a TID measurement campaign the accuracy is capped. The I-V curves as presented in Figure 4 are measured over several dies and the extracted leakage currents with too much variation over the dies are filtered out. These results are left out in Figure 5 which occur for TID values equal and below 250krad.

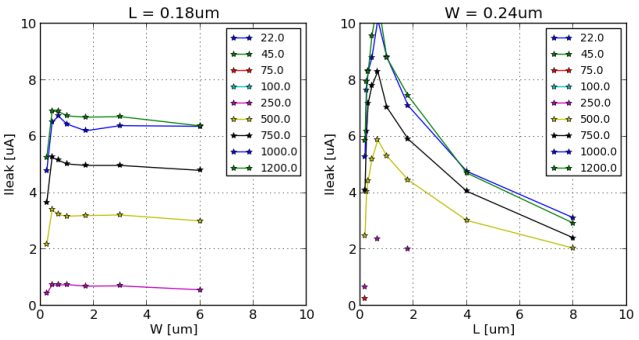
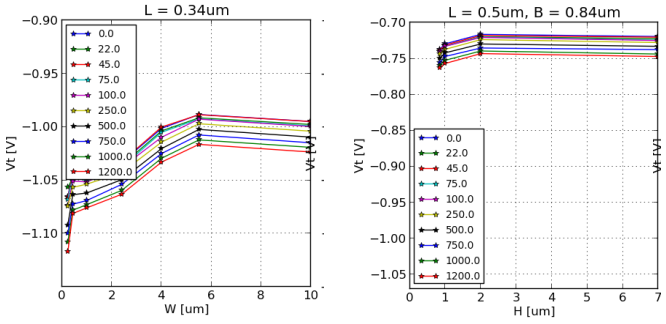


Figure 5: measured TID leakage current induced for straight std. Vt 1.8V NMOS as functions of W and L



a) straight std V_t 3.3V PMOS b) ELT low V_t 3.3V PMOS

Figure 6: Measure TID induced $V_{t,sat}$ shift on 3.3V PMOS

No TID induced leakage was measured on ELT NMOS transistors or on straight or ELT PMOS ones. For the 3.3V PMOS devices a small TID induced V_t shift was measured; results are shown in Figure 6. The V_t is in saturation and is extracted from the measurements by fitting a linear line to the I_d-V_{gs} curve; using a V_t fit method based on higher order derivatives of the I-V curves is difficult due to the measurement noise and repeatability. The absolute value will differ from V_t reported in other places using other fit methods. Next to the I-V results reported in this paragraph a much more extensive set of device parameters have been measured for TID sensitivity. A quick overview:

- Matching: no effect of TID observed
- C-V: no effect of TID observed
- Noise: no effect of TID observed
- Diodes: no effect of TID observed
- Bipolar: TID induced beta degradation measured
- Parasitic Field Devices leakage: TID induced leakage between n-type regions measured but the impact of poly and metal routing in between them is not understood. Measurements seem to indicate that the need of P+ guards can be relaxed in certain layout configurations but further investigation with an extended test set is needed to confirm that.

3) ELT Parasitics

In previous paragraph it was already shown that W/L formula of the ELT is a good approximation for the drive capability of the NMOS device and is also possible with some correction for the PMOS. Commonly, for analog designs not only the drive current of the device is important but also the parasitics; this includes for designs using high(er) frequencies, feedback loops,... . The layout for the ELT was already given in Figure 2 and in Figure 7 the well-known normal straight transistor is shown. The gate area used in BSIM3 SPICE models is assumed to be equal to (W+ΔW)*(L+ΔL); for the ELT the actual area is larger than the one computed with the equivalent W. The actual area increase starts from 30% for the minimal dimension device up to 90 % for a 10µm long transistor.

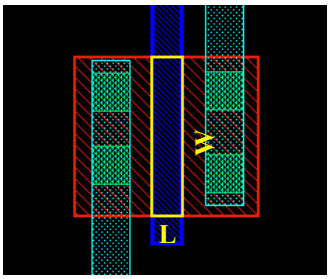


Figure 7: Regular Straight Transistor Layout

For the ELT as given in Figure 2 the gate to source or drain overlap is asymmetric between inner and outer diffusion area. BSIM3 model assumes that this overlap is symmetric and with the length equal to W. For this length and thus the gate to source/drain capacitance differences from 10% to 90% are seen; smaller for the inner diffusion area and larger for the outer diffusion area compared with straight transistor.

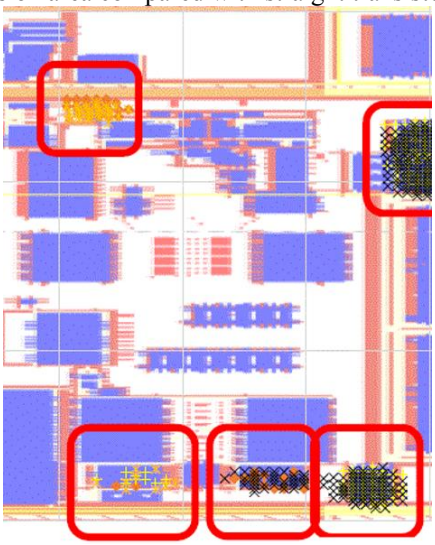


Figure 8: SET sensitivity laser testing report correlating with hot PMOS transistor locations

4) Hot-PMOS

As is shown in Figure 8, during SET laser testing of a chip it was found that some PMOS transistors with N-well not connected to the supply net were more sensitive to single-event effects than expected from charge injection based simulations. The physics are not fully understood yet although bipolar amplification is thought to have a play here. Without full understanding also no detailed design guide lines can be given. In the meantime as a precaution it is best to avoid using these devices or use MiM or MoM capacitances.

IV. DARE180U ADK IMPROVEMENTS

Based on the learning presented in the previous chapter, improvements have been made in different places in the ADK. The measured beta degradation of the bipolar transistor is not modeled but the measurement results are provided to the ADK users on request. For the P+ guard band checks the conservative approach of enforcing them in between all n-type regions on a different net is kept.
The next paragraphs will detail the improvements.

1) Schematic Capture Rad. Hard. Related Warnings

The RAD check from the first ADK is performed on the layout. Preferably already during design phase radiation hardness would be taken into account. For this purpose the "custom Virtuoso schematic checks" feature is used. In Figure 9 the list of checks as seen from the schematics rules checks setup window is given. Each of these checks can be put to be ignored, to give a warning or to give an error. The general default setting used when opening a schematic views can be configured for each of the rules in the setup of the ADK and thus be adapted to the designer's chosen radiation mitigation strategy.
When ADK setup is not changed the following checks are performed. The usage of straight 1.8V NMOS transistors will give a warning; the impact of the TID induced leakage can be verified by simulation as explained in the paragraph on improved modeling. The use of 3.3V NMOS devices gives an error and for these devices no TID induced sub-threshold current model is given. The modulation of the sub-threshold current by V_{gs} complicates the modeling and would need a more extensive data set than is currently available. Also by default a warning is given for the usage of the 3.3V PMOS to indicate the (small) TID induced V_t shift that is also modeled for simulation. And finally a warning is given for the use of hot-PMOS transistors that are possibly more sensitive for single events; for this check valid net names for the PMOS bulk connections have to be configured during setup of the ADK.

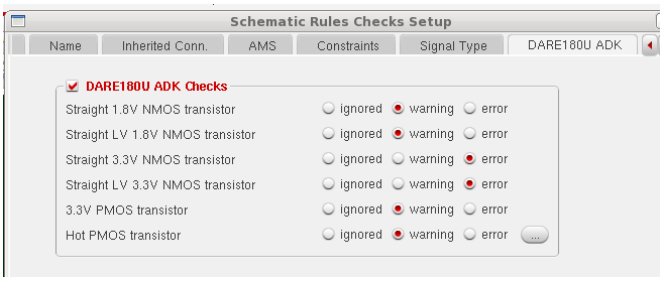


Figure 9: List and configuration of DARE180U ADK custom schematic checks

2) Optional LU Checks

The RAD check was extended with optional latch-up checks for more dense well contact placement and usage of guard rings at the edge of wells and in between wells. In Figure 10 an example is given. In the ADK manual the full list of the optional checks is explained.

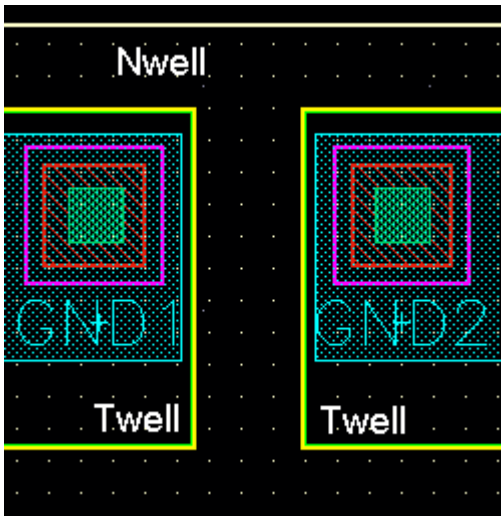


Figure 10: Optional latch-up check for Triple Wells inside same N-well connected to different nets and not isolated from each other

3) Modeling Improvements for Parasitics and TID

The transistor simulation models have been modified to include measured radiation effects as presented in previous chapter. UMC provided models are used as base to avoid a full calibration exercise and to minimize discrepancies with simulations performed using the original models. Below is an overview of the modeled effects.

- Correction of the computed equivalent W for the PMOS ELTs to account for the lower measured drive current
- Correction in computation of the gate area, gate-to-source/drain overlap capacitance and the inner and outer diffusion perimeter as explained in the paragraph 'III.3) ELT Parasitics'
- Modeling of the TID induced leakage current for straight 1.8V NMOS transistors. Simulation process corners at different TID levels are provided. Next to the tt (=typical-typical) corner also a tt_250k, tt_500k, tt_750k, tt_1000k corner is provided; this is repeated for all UMC provided process corners.
- Modeling the (small) TID induced V_t shift for the 3.3V PMOS transistor. This is also modeled by providing simulation process corners at the same TID levels as for the TID induced leakage.

4) Schematic Driven Layout Compliance

Over the years the Virtuoso full-custom/mixed signal design flow is extended to improve productivity of the designer. This includes tools like Virtuosos Layout (G)XL & EAD. For this to work well proper support in each of the views has to be implemented, including the ones provided in ADK by the ELT p-cell. In Figure 11 an example layout is shown; it includes a NMOS and PMOS ELT transistor and due to proper support in the p-cell the nets as defined in the schematic can be visualized.

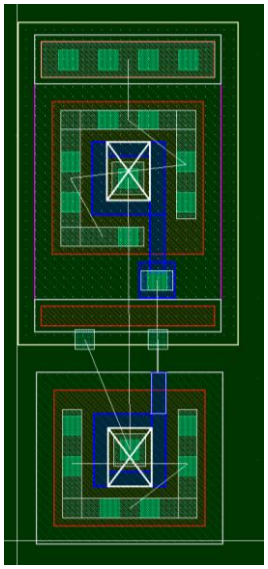


Figure 11: Layout showing connectivity compliant pcell layout view

V. Interesting Future Additions

Developing EDA tools and a mixed-signal/full-custom design flow is never finished. There will always be room for improvement or extension of the flow. Some candidates that came out of the discussions during all the designs and contacts with the community are presented in following paragraphs. For further discussion on one of the topics always DARE support [4] can be contacted.

1) Full physics based ELT device model

Currently the equivalent W and the parasitics computation of the ELT are based on geometrical based derivations. With the current availability of memory size, compute power and 3D process and device TCAD simulation tools it should be possible to simulate device performance based on device physics. This way it can also be validated if there is an asymmetric behavior in performance between current flowing through the ELT from inner diffusion to outer diffusion or in the other direction.

Setting up a 3D TCAD simulation for a non-conventional shape like the ELT is involved, especially if not only steady state effects are of interest but also transient effects like gate capacitance and the gate to source/drain overlap capacitance. For analog design already the transistor performance variation over the process corners is taken into account and in this light the effort to calibrate a full-physics based ELT model has to be weighed against the added value and reduced risk.

2) Modeling Parasitic Devices for SET Simulations

The foundry provided PDK provides support for digital and analog/mixed-signal design. In such a flow not all parasitic devices are important and not all of them may be modeled; for example for the UMC 0.18mm PDK the N-well to P-substrate diode is not modeled. When looking at single-event effects these devices may play an (important) role and models would be preferred for doing SPICE level simulations. Providing support for these parasitic devices not only the model has to be calibrated based on experimental results, likely well and substrate resistance has to be included in this exercise also.

Also the necessary views have to be provided and adapted so these devices can or have to be included in the schema and layout. The extraction deck has to be updated so the parasitic devices are recognized in a layout etc.
In the end, one may end up not with an ADK that is an extension of the foundry provided PDK for specific radiation hardness design requirements but a full revision of the whole PDK. PDK development is already considered a tough job by the foundries for their high-volume commercial processes so support is needed from the community if similar work needs to be performed for the low-volume space community.

3) SET simulation flow

The current ADK is now able to provide the necessary input to the designer to allow for easy investigation and mitigation of TID induced effects.
For single-event simulation currently manual or at best semi-automatic flows are used. Also at imec an internal flow is used for single-event simulation based on charge injection on selected nodes. It's a combination of semi-automated scripts and more manual work like node selection, ad-hoc simulation setup, etc. Another example of a flow is AFTU[5] working on Spectre netlist level and guided automation using Virtuoso Ocean simulation scripting.
Such flows are a perfect candidate to be much more automated by the proper use of scripting and the proper EDA tools and integrating in the ADK design flow. The work involved to go from an ad-hoc flow used in a specific setup to a more generalized and more automated one, should not be underestimated though. With cooperation with and support from the community it would be able to provide that as part of the ADK.

VI. SUMMARY

In this paper the improvement and the extension of the DARE180U ADK was presented based on continuous learning from IP development, ASIC tape-outs and test-vehicles. The combination of all added features in the DARE180U ADK allows designers to work in a flow that they are familiar with, benefiting from the productivity support provided by state-of-the-art EDA tools while including knowledge of radiation hardening-by-design of the technology. It allows the designers to focus on circuit performance and specific radiation requirements using a flow similar to the foundry-provided PDK flow enabling full custom/analog, digital standard cell and mixed-signal IP development.
Also some future improvements and extensions that can be implemented given the needed cooperation with and support from the European space community.

ACKNOWLEDGEMENTS

Due to the long history of the DARE180U a lot of parties have contributed to the advancement. First is the interaction and discussion with CMOSIS on the parasitic modeling of the ELT transistors. Conclusions on data can only be valid if hard work is put into the setup and dutiful execution of the measurement; in this case impossible without the dedicated work of microtest, Alter Technology and MASER Engineering. Discussions with and input from Thales Alenia Space Belgium and ICsense has been the seed for the latch-up checks. The other users of the ADK are always challenging us and thus help us to improve the tool to better fit their needs; this includes S.A.B.C.A, Cobham-Gaisler, Arquimea, RUAG, and IMSE-CNM.
Finally the expertise of the ESA officers is also invaluable as a guidance and help for getting projects successfully to completion and needs known to us.

REFERENCES

[1] G. Anelli & co (1999 December) "Radiation Tolerant VLSI Circuits in Standard Deep Submicion CMOS Technologies for the LHC Experiments: Practical Design Aspects", IEEE Transaction on Nuclear Sciense, Vol. 46, No. 6
[2] 2nd DARE User Day: https://indico.esa.int/indico/event/72/other-view?view=standard
[3] ESA Contract Nr 4000104087/11/NL/AF: "DARE PLUS ASICS for Extreme Radiation Hardness and Harsh Environments"
[4] DARE support: dare_support@imec.be
[5] F. Marquez & co. (June 2014), "AFTU, an Analog Single Event Effects Automatic Analysis Tool", AMICSA 2014.

Comparison Study of Bulk and SOI CMOS Technologies based Rad-hard ADCs in Space

Feitao Qi , Tao Liu , Hainan Liu , Chuanbin Zeng , Bo Li , Fazhan Zhao , Jiantou Gao , Gang Zhang , Jiajun Luo* , Zhengsheng Han , and Zhongli Liu

Institute of Microelectronics of Chinese Academy of Sciences, Beijing 100029, CHINA
Key Laboratory of Silicon Device Technology, Chinese Academy of Sciences, Beijing 100029, CHINA

*Corresponding Author's Email: luojj@ime.ac.cn

Abstract

The electrical and radiation characteristics of the bulk and silicon-on-insulator (SOI) CMOS based rad-hard analog-to-digital converters (ADC) in space are compared in this paper. A 10bits monolithic, high reliability pipelined ADC with 25Msps conversion rate is presented as a prototype to exhibit the benefits of radiation hardened by design (RHBD) and radiation hardened by process (RHBP) approaches. The ADC prototype hardened by RHBD is fabricated with 0.35um bulk CMOS technology and radiation hardened SOI CMOS technology with an identical technology node respectively. The experimental results show that the SOI-based ADC achieves the total ionizing dose (TID) tolerance of 300krad(Si), nearly one order of magnitude higher than the bulk ADC, and the single event upset (SEU) cross-section of 9.6E-6cm^2/device at 63MeV·cm^2/mg linear energy transfer (LET), lower than the bulk ADC by two orders of magnitude. The SOI-based ADC is also better than the bulk ADC in the electrical characteristics. It is more suitable for harsh radiation environment applications.

I. Introduction

In the harsh space environment, the integrated circuits within various electronic equipments often suffer from serious degradation due to the radiation effects, which lead to compromise spacecraft reliability [1,2] . As the interface between analog and digital circuits, analog-to-digital converters (ADC) are widely used in aerospace electronic equipments, and its reliability has received more attention. Radiation hardened silicon-on-insulator (SOI) CMOS technology has many advantages comparing with bulk CMOS technology, such as higher speed, lower parasitic capacitance, smaller short channel effects, etc. Especially due to its excellent capability of radiation hardness, the rad-hard SOI CMOS technology is more suitable for space applications.

Until now, intense interest has been paid in the radiation effects and hardened approaches of ADC [3-6], and the transistor level comparison between SOI CMOS technology and bulk technology is also studied extensively [7-10]. But there is seldom research on circuit level comparison between SOI CMOS technology and bulk technology for analog and mixed signal circuits, especially for ADC in space. In this paper, the electrical and radiation characteristics of the bulk and SOI CMOS based rad-hard ADCs in space are compared. A 10bits monolithic, high reliability pipelined ADC with 25Msps conversion rate is presented as a prototype to exhibit the benefits of radiation hardened by design (RHBD) and radiation hardened by process (RHBP) approaches. The ADC prototype hardened by RHBD is fabricated with 0.35um bulk CMOS technology and radiation hardened SOI CMOS technology with an identical technology node respectively. Both ADCs are tested under the same conditions and environment for comparison.

This paper is organized as follows: section II introduces the system architecture of the pipelined ADC prototype, section III describes the circuits design of the ADC prototype, the RHBD and RHBP approaches are provided in section IV, section V shows the experimental results and discussion on electrical and radiation characteristics, followed by a brief conclusion in section VI.

II. System Architecture

The block diagram of the pipelined ADC prototype is illustrated in Figure 1.

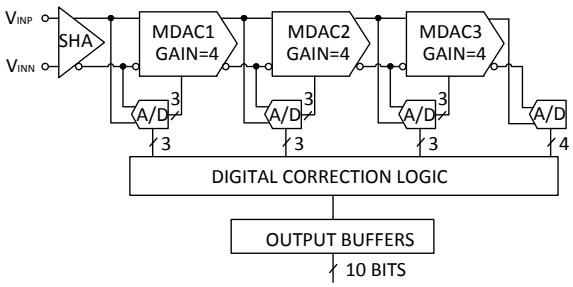


Figure 1: Block diagram of pipelined ADC prototype

In the front end of the converter, a sample and hold circuit is used to extend the input bandwidth of the ADC, followed by a cascade of three identical stages in which each stage performs a 2.5bits coarse quantization. The last stage is a 4bits flash ADC. Finally, the 13bits coarse quantization results are feed into digital correction logic to generate 10bits resolution at the output of the pipelined ADC.

III. Circuits Design

A. Sample and Hold Circuit

The sample and hold circuit (S/H) is based on a capacitor flip-around architecture [11], as shown in Figure 2.

Compared with a charge transfer S/H, the capacitor flip-around architecture S/H exhibits the advantages of lower power consumption, smaller die size and better radiation hardness capability due to its larger feedback factor and lower

load capacitor which can maximize the closed-loop gain and bandwidth of amplifier. In order to reduce the nonlinear effects of the switch caused by charge injection and clock feed through, the bottom plate sampling technique is adopted. To improve the input bandwidth of the S/H, the bootstrapped switch [12] is used on SW1, SW2, SW3 and SW4 in Figure 2.

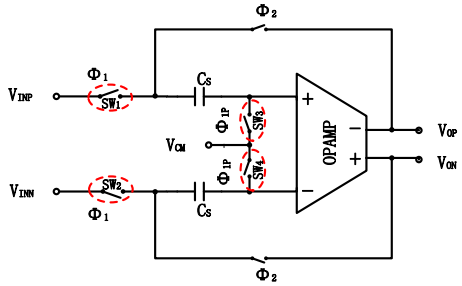


Figure 2: Sample and hold circuit

A high performance operational amplifier (opamp) is included in the S/H. Threshold voltage drift, migration rate and transconductance degradation caused by total ionizing dose will reduce the gain and the bandwidth of the opamp, increase DC offset, and finally affect the performance of the circuit, so the margin must be sufficient when designed [13]. A gain-boosted folded cascade amplifier is used in the S/H [14], as shown in Figure 3. This structure can efficiently improve the gain without reducing the bandwidth of the opamp.

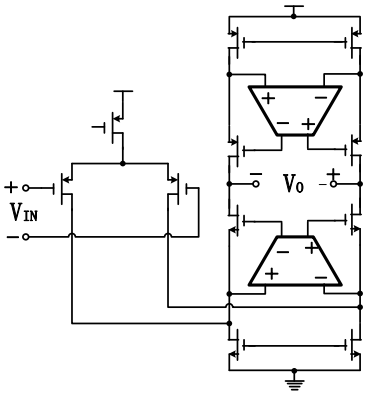


Figure 3: Gain-boosted folded cascade amplifier

B. Switched Capacitor Comparator

A switched capacitor comparator with a preamplifier is adopted, as shown in Figure 4.

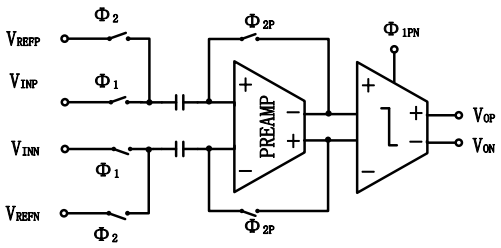


Figure 4: Switched capacitor comparator

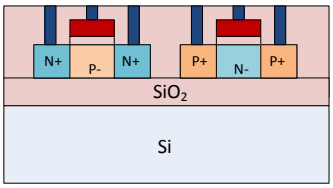
The switched capacitor structure can extend the input common mode range of the comparator, and the DC offset of the comparator can be reduced within a lower range due to the preamplifier. Thus the comparator allows larger tolerance for the error caused by radiation.

IV. Radiation Hardened Approaches

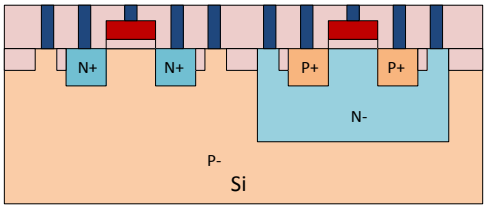
A. Hardened System and Circuits

In order to improve the radiation performance of the ADC prototype, the 2.5bits/stage system structure, the capacitor flip-around S/H, the gain-boosted folded cascade amplifier and the switched capacitor comparator with a preamplifier are all carefully determined and designed as described in section III. The values of the currents and capacitors in those sensitive parts are increased properly for the purpose of radiation hardness. By implementing the above RHBD approaches, the ADC prototype generates much smaller deviations when radiated. If the deviations from comparators are small enough to locate in the error correction range of the pipelined ADC, they will be corrected by the digital error correction logic.

B. Rad-Hard SOI CMOS Technology



(a)SOI CMOS



(b) Bulk CMOS

Figure 5: Cross-section views of SOI and bulk CMOS technologies

The SOI CMOS technology joins silicon dioxide as a buried insulator layer on silicon substrate as shown in Figure5 (a). The complete isolation between NMOS and PMOS eliminates any of the latch-up events [15]. Compared with bulk CMOS technology, the SOI CMOS technology could mitigate the sensitivity of single event upset (SEU) and single event functional interrupt (SEFI) due to its much smaller charge collection volume. As a result of the radiation hardened techniques, the total ionizing dose radiation tolerance of the rad-hard SOI CMOS technology has also reached a fairly high level. Figure5 (b) is the cross-section view of the bulk CMOS technology.

C. Hardened Layout

Contrasting with the immunity of single event latch-up (SEL) of the SOI CMOS ADC, the bulk CMOS ADC has to be implemented with reasonable and rigorous layout rules to mitigate the sensitivity of SEL. The substrate contact around the transistor should be sufficient to avoid the latch-up,

especially for the NMOS and PMOS which are close to each other [16], as shown in Figure 6.

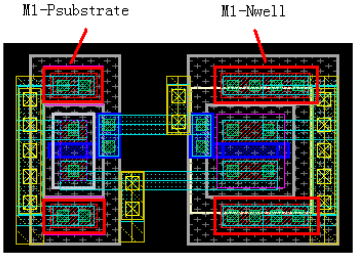
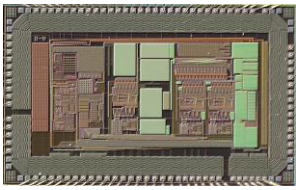


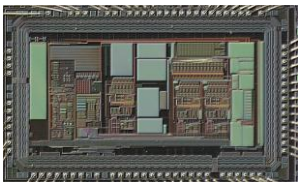
Figure 6: Hardened layout

V. EXPERIMENTAL RESULTS

The micrographs of ADC in different technologies are shown in Figure 7, respectively. The electrical and radiation characteristics of the two ADCs are tested for comparison.



(a) SOI CMOS ADC



(b) Bulk CMOS ADC

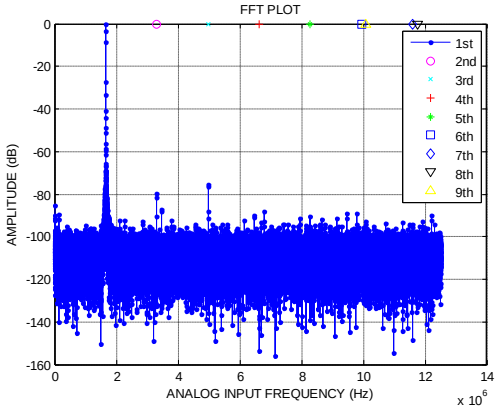
Figure 7: Micrographs of ADC in different technologies

A. Electrical Experiment

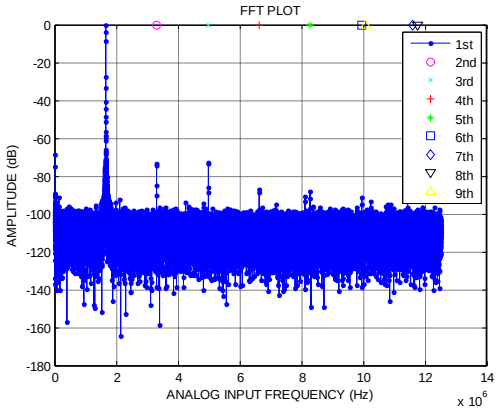
A high purity sine wave signal is feed to the ADCs with 25Msps sampling rate. The digital output data of the ADCs are captured and analyzed to obtain the electrical parameters such as SNR, ENOB, DNL, INL, etc. The electrical characteristics experiment indicates both of SOI ADC and bulk ADC could achieve effective number of bits (ENOB) of 9.5bits, spurious-noise-free dynamic range (SFDR) of 72dB, differential nonlinearity (DNL) of 0.4LSB, and integral nonlinearity (INL) of 0.5LSB. The detailed performance characteristics are listed in Table 1. Electrical Characteristics Comparison of SOI-based ADC and bulk CMOS ADC

	SOI ADC	Bulk ADC
F_S(Hz)	25M	
Freq_vin(Hz)	2M	
Supply（V）	5	
Consumption（mw）	240	
DNL(LSB)	±0.4	±0.4
INL(LSB)	±0.5	±0.5
SNR(dB)	60.5	59.6
SFDR(dB)	72.3	74.4
SINAD(dB)	60.2	59.2
ENOB(bits)	9.7	9.5

The spectrum analysis results of the SOI and bulk ADCs with 25Msps sampling rate are shown in Figure 8.



(a) SOI CMOS ADC



(b) Bulk CMOS ADC

Figure 8: Spectrums of SOI and bulk CMOS ADC with 25Msps sampling rate

By changing the sample rate, the frequency characteristics of the ADCs are obtained. Test results show that the SOI ADC still maintains the ENOB of 8.2bits up to the 40Msps. The ENOB of the bulk ADC is lower than 8bits from 31Msps and only 2.5bits to 40Msps. The SOI technology exhibits better frequency characteristic because the SOI MOSFET has smaller parasitic capacitance and better I-V characteristic. The comparison of the SOI and bulk based ADCs frequency characteristic is shown in Figure 9.

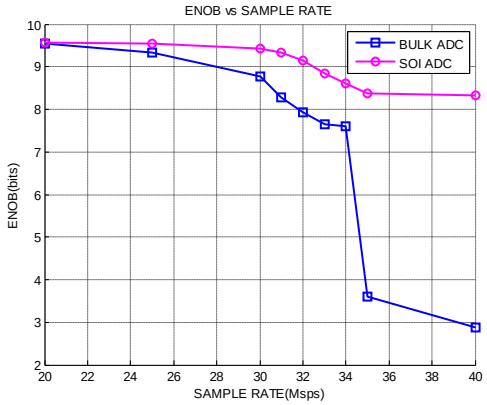


Figure 9: Comparison of the SOI and bulk based ADCs frequency characteristic

B. TID Experiment

The total ionizing dose (TID) experiment is performed by the Cobalt-60 gamma radiation source at Peking University.

The sample ADCs with different technologies are selected for the TID experiment. The samples are irradiated to 500krad(Si) with a dose rate of 50rad(Si)/s at the room temperature, and annealed 168 hours at 100℃ after last dosing [17]. During the experiment, samples are left static bias state, and measures are performed at pre-radiation, 50k, 100k, 150k, 300k, 500krad(Si) and after anneal.

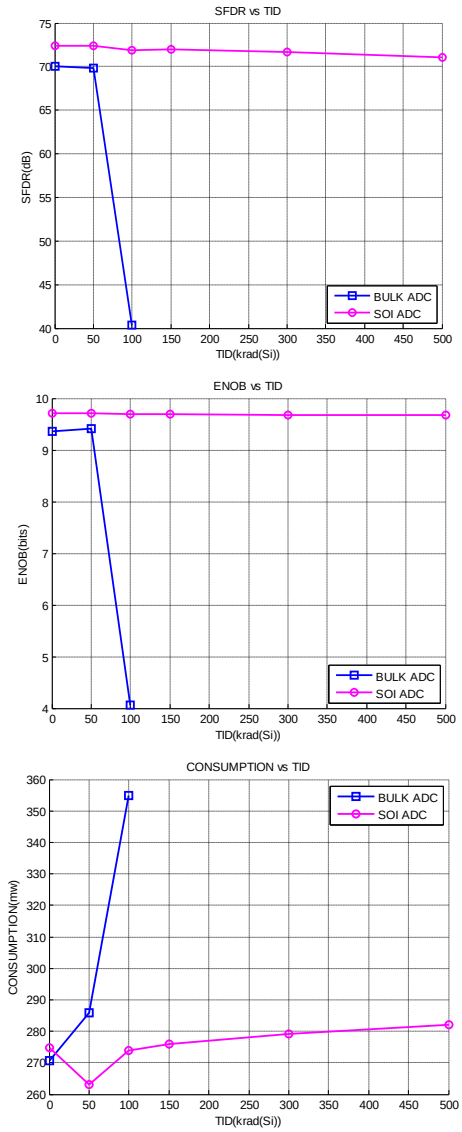


Figure 10: Comparison of TID responses between SOI and bulk CMOS ADC

The experimental results reveal that the SOI ADC maintains the consumption and spectral performances up to 500krad(Si), and the performances degradation are not observed after anneal. It achieves the TID tolerance of 300krad(Si) at least.

The bulk ADC performances with the identical circuit design and layout floor plan do not degrade until the radiation dose accumulation up to 50krad(Si). Drastic reductions are observed over 50krad(Si) , the ENOB of bulk ADC is only 4bits and the increasing of the consumption is over 25% at 100krad(Si). After annealing, the ENOB and the consumption of the bulk ADC both recover to meet all specifications.

Comparison of TID responses between the SOI and bulk CMOS ADCs is shown in Figure 10. It can be seen that the TID tolerance of SOI-based ADC is nearly one order of magnitude higher than bulk ADC. This is due to the radiation hardened techniques used in the SOI CMOS technology.

C. SEE Experiment

The single event effects (SEE) experiment is performed by the HI-13 tandem accelerator at the China Institute of Atomic Energy.

The sample ADCs with different technologies are selected for SEE test. At room temperature, all samples are irradiated by particles broad beams with stable DC analog input signals including -0.8V, 0V and 0.8V. The fluence is 1E7 /cm^2 with the 1E4 /cm^2• s flux. By monitoring the digital output and the consumption of the ADC, if the deviation of the digital output is more than ±4LSB from the expected value, or the consumption increases over 10% of the normal, the single event effect is confirmed [17].

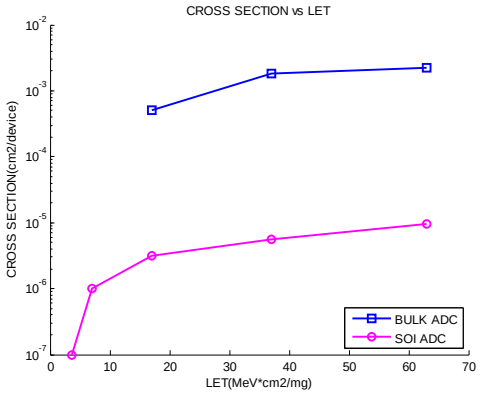


Figure 11: Comparison of SEU cross-section between SOI and bulk CMOS ADC

The experimental results indicate that neither ADC exhibits single event latch-up (SEL) and single event function interrupt (SEFI) sensitivity up to the maximum tested LET of 63MeV·cm^2/mg. This is due to the good nature of SEE insensitivity of SOI technology and the reasonable and rigorous layout rules of the bulk CMOS ADC.

The input voltage value does not have obviously effect on the device single event upset (SEU) sensitivity. At the LET of 17MeV·cm^2/mg, the SEU cross-section of the SOI-based ADC is about 3.1E-6cm^2/device, at the LET of 63MeV·cm^2/mg, the SEU cross-section of the SOI-based ADC is about 9.6E-6cm^2/device, both of the two points are lower than bulk ADC by two orders of magnitude. Due to implement the suitable RHBD approaches and take the inherent advantage of the rad-hard SOI technology, the SOI-based ADC generates much smaller deviations when radiated. Because most deviations could be corrected by the pipelined ADC's digital error correction logic with the system

redundancy, the SOI-based ADC acquires excellent rad-hard accomplishments. In contrast the bulk CMOS ADC with identical schematic design and layout floor plan could not be so efficient in SEE experiment. Figure 11 illustrates the differences of SEU cross-section between SOI and bulk CMOS ADCs.

VI. Conclusion

In conclusion, by implementing simple RHBD approaches and taking the inherent advantage of the rad-hard SOI technology, the SOI-based ADC achieves the TID tolerance of 300krad(Si) at least, nearly one order of magnitude higher than bulk ADC, and the SEU cross-section of 9.6E-6cm^2/device at 63MeV·cm^2/mg LET, lower than bulk ADC by two orders of magnitude, more suitable for harsh radiation environment applications.

VII. References

[1] D. Binder, E. C. Smith, A. B. Holman, "Satellite Anomalies from Galactic Cosmic Rays," IEEE Trans. Nucl. Sci., vol. 22, No. 6, pp. 2675-2680, Dec. 1975.

[2] R. L. Pease, "Total Ionizing Dose Effects in Bipolar Devices and Circuits," IEEE Trans. Nucl. Sci., vol. 50, No. 3, pp. 539-551, 2003.

[3] F. Baille, G. Borel,B. Commere, "A Multi MRad hardened 8 bit/20 MHz flash ADC," IEEE Trans. Nucl. Sci., vol. 39, no. 3, pp. 401-404, Jun. 1992.

[4] O. A. Kalashnikov, A. A. Demidov, "Integrating analog-to - digital converter radiation hardnesstest technique and results," IEEE Trans. Nucl. Sci., vol. 45, no. 6, pp. 2611-2615, Dec. 1998.

[5] A. L. Sternberg, L. W. Massengill, M. Hale, B. Blalock , "Single-Event Sensitivity and Hardening of a Pipelined Analog-to-Digital Converter", IEEE Trans. Nucl. Sci., vol. 53, no. 6, pp. 3532-3538, Dec. 2006.

[6] C. R. Grace, P. Denes, D. Gnani, H. von der Lippe, J. P. Walder, "Radiation-Tolerant Code-Density Calibration of Nyquist-Rate Analog-to-Digital Converters," IEEE Trans. Nucl. Sci., vol. 60, no. 2, pp. 1303-1310, Apr. 2013.

[7] G. Gasiot, V. Ferlet-Cavrois, P. Roche, " Comparison of the sensitivity to heavy ions of 0.25-µm bulk and SOI technologies," IEEE Trans. Nucl. Sci., vol. 49, No. 3, pp. 1450-1455, Jun. 2002.

[8] J. A. Babcock, P. Francis, C. Olgaard, J. A. Darmawan, "Comparison between Short Channel Bulk (Silicon) and Body-Tied Partially Depleted SOI nMOS for High Frequency Low Voltage Analog Circuit Design"IEEE Solid-State Device Research Conference, vol. 1, pp. 208-211, 1999.

[9] M. H. Han, C. Y. Chang, H. B. Chen, H. B. Chen, J. J. Wu, "Performance Comparison Between Bulk and SOI Junction less Transistors" IEEE Electron Device Letters, vol. 34, no. 2, pp. 169-171, Feb. 2013.

[10] A. V. Oliveira, P. G. D. Agopian, E. Simoen, "Comparison of analog performance between SOI and Bulk pFinFET," Microelectronics Technology and Devices (SBMicro), pp.1-4, 2014.

[11] Haitao Wang, Hui Hong, Lingling Sun, and Zhiping Yu, "A sample-and-hold circuit for 10-bit 100MS/s Pipelined ADC ," ASICON IEEE, pp. 480-483, Oct. 2011

[12] Andrew M. Abo and Paul R. Gray, "A 1.5-V, 10-bit,t14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," IEEE J. Solid-State Circuits, vol. 34, no. 5, pp. 599-606 May.1999

[13] Y. Yao, De sheng Ma, F. Dai, "A 12-bit interleaved opamp-sharing pipeline ADC for extreme environment application s," ICSICT IEEE, pp. 394-396 Nov. 2010

[14] K. Bult, G. J. G. M. Geelen, "A fast-settling CMOS opamp for SC circuits with 90-dB DCgain,"IEEE Journal of Solid-State Circuits, vol. 25, no. 6, pp. 1379-1384, Dec. 1990.

[15] Ru Huang, Guoyan Zhang, "Technologies and Applies of SOI CMOS," Beijing Science Press, Jan. 2005.

[16] Shicai Qin and Xiangluan Jia, "Electronics of Analog Integrated Circuits," Tianjin Science and Technology Press, Jan. 1996.

[17] "MIL-STD-883J_CHG-2", Mar. 2014.

DESIGN METHODOLOGY FOR MIXED SIGNAL ASIC WITH PREQUALIFIED ANALOG IPS

FOR SPACE APPLICATIONS

B.Bancelin

ATMEL Nantes
La Chantrerie, Route de Gachet
44300, Nantes, France

bernard.bancelin@atmel.com

Abstract

Mixed Analog / Digital System on Chip are increasing drastically in space equipment to reduce cost, power and dimensions and to improve performances.

The challenge for mixed SoC is to get a qualified product without heavy SEE or TID testing. As for a digital library, analogue cells and their combinations, High voltage LDMOS, regulators (to allow single supply) and latch-up protections must be "pre-qualified".

The qualification of IOs and digital is done by using a Standard Evaluation Circuit covering at least half of the maximum of transistor of an ASIC.

For the analog part all blocks must be validated. In addition, in order to check the "integrability" of the building blocks towards the elaboration of a complex space-adequate System-on_Chip, a complex function will be realized embedding all individual analog cells and a digital block embedded as an analog cell.

During the realization of this complex function emphasis is given to the observability and testability of the individual building blocks. For each new analog cell the same process must be conducted. The study will continue by determining the observability of the analog nodes and specifically the eventual propagation of Single Event Transient.
This study is conducted with support of ESA and CNES and with European industrial partners.

ATMEL ATMX150RHA offers a wide range of capabilities to enlarge the SoC integration: digital integration up to 20M gates, NVM, analogue, 3Gbit serial interface, N and P deep well, Deep Trench to isolate blocks, handle Wafer contact, 1.8V digital core, 3V, 5V, 15V and high voltage up to 60V. Mixing power, high voltage and high speed on a single chip needs adequate packaging technology, large die and small die must be handled by different packaging solutions: double pad ring, flipchip, Au bonding, Al bonding.

ATMEL can base the qualification for space requirements on standard process used in high volume. It ensures longer process lifetime and stability, as well as lower access cost. Same advantages applies to probe, assembly and final test. A mixed Standard Evaluation Circuit is under definition in order to check the "integrability" and "space testability and observability" of the building blocks.

The flow and the rules for integration of analogue cells coming from multiple suppliers will be clearly defined and qualified.

I. DESIGN FLOWS

I.1. DK description

The ATMX150RHA DK contains a complete set of tools, models, utilities and technology files for Place & Route environment and documentation.
It includes

- Libraries
  - Libraries for Design For Testability
  - Error Detection And Correction source code and testbenches
  - Topological libraries used by Synopsys tools
  - Compiled & Source libraries for Design Compiler Synthesis tool
  - Utilities for ATPG tool
  - Verilog & VHDL/VITAL models for cells, buffers and memories
- Tools
  - Atmel Tool Box & Freeware
  - Package Interface Management
  - Virage RAM / ROM compilers

I.2 PDK description

The ATMX150RHA PDK contains the hardening design rules. Transistors are characterized for the military temperature range (-55°C, +125°C).

It includes

- Analog cells
- Design rules
- Encrypted RHBD IOs netlists

Atmel plans to deliver Encrypted IP's with test files separately, through Atmel Design centers (see §4.2).

I.3. ASIC DEVELOPMENT FLOW

I.3.1. Standard Flow

Standard flow is when customer wants a full digital ASIC or uses Atmel analog IP's, he does not design any analog blocks. In such case, customer has to download the DK, encrypted IP netlist are provided separately. Customer designs its ASIC using ATMX150RHA RHBD library and analog IP blocks, providing Atmel with a synthetized netlist. Atmel is in charge of the Place & Route and verifications. *Figure 1* shows the design flow from DSR to DR with shared responsibilities.
This development phase is concluded by a Design Review (DR) meeting, involving Customer and Atmel. The objective of the Design Review is to validate the entire circuit database and the physical design. The main checked criteria are the simulation results with post-layout, back annotation timings, the layout organization with bonding diagrams and package features and the test program in compliance with Atmel tester rules.

At this step, customer has to provide Atmel with test vectors and burn-in program as well as ASIC marking.

A soon as the DR document is signed off, the manufacturing of the masks set and wafers lot start. 5 validation prototypes and 5 industrialization prototypes (*see appendix 1- prototypes definition*) are delivered to customer for ASIC validation on board.

I.3.2. Analog Flow

Customer wants a full analog ASIC, he designs its own analog blocks and potentially uses Atmel catalog IP's. In such case, customer has to download DK and PDK, encrypted IP netlist are provided separately. The development flow is as described in *figure 2*, Atmel will start from GDSII and run a DRC/ARC/LVS.
This development phase is concluded by a 'light' Design Review (DR) meeting, involving Customer and Atmel. The objective of the Design Review will depend on the Atmel services requested by customer.

- Foundry only: to confirm the DRC/ARC/LVS checks and freeze the schedule for wafer/dice delivery
- If Assembly service option: to freeze the package/pinout
- If Probe/test service option: to provide Atmel with test patterns.

A soon as the DR document is signed off, the manufacturing of the masks set and wafers lot start.

I.3.3. Digital or Analog on top

Customer wants a mixed-signal ASIC and will design its own analog blocks and potentially uses Atmel catalog IP's. In such case, customer has to download DK and PDK, , encrypted IP netlist are provided separately. The development flow will be as described in *figures 3 & 4*. Atmel manages the digital part (P&R, verifications, Cross-talk, IR drop, parasitics extractions…). If analog on top, Digital .LEF is provided to customer for top-layout and if digital on top, Analog .LEF is provided to Atmel for P&R.
This development phase is concluded by a Design Review (DR) meeting, involving Customer and Atmel. The objective of the Design Review is to validate the entire circuit database and the physical design. The main checked criteria are the simulation results with post-layout, back annotation timings, the layout organization with bonding diagrams and package features and the test program in compliance with Atmel tester rules. At this step, customer has to provide Atmel with specification to test analogue blocks and burn-in program as well as ASIC marking.
A soon as the DR document is signed off, the manufacturing of the masks set and wafers lot start. 5 validation prototypes and 5 industrialization prototypes (*see appendix 1- prototypes definition*) are delivered to customer for ASIC validation on board.

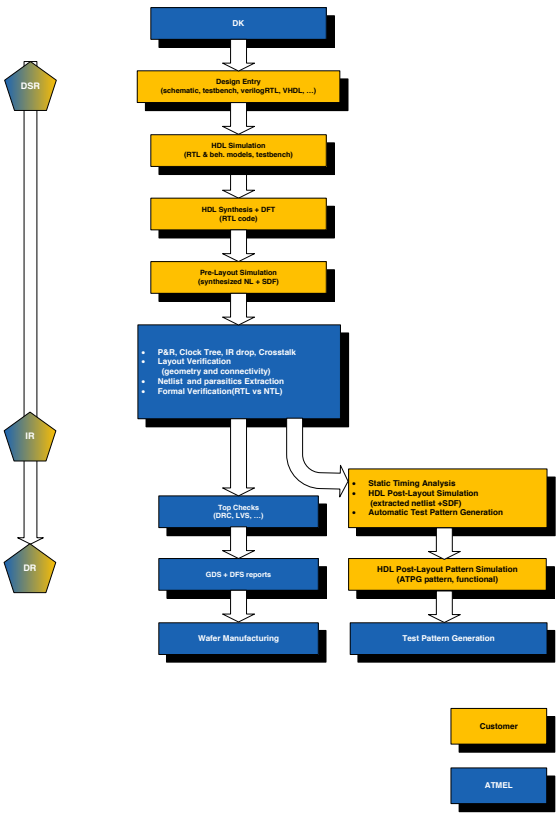


Figure 1: Development flow for digital ASIC or ASIC with Atmel pre-qualified analog IP's

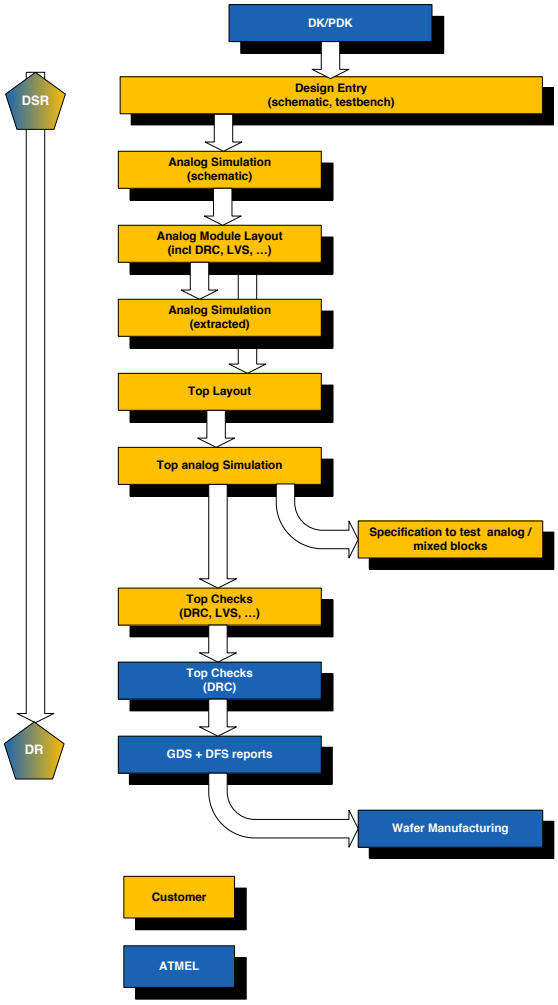


Figure 2: Development flow for analog ASIC

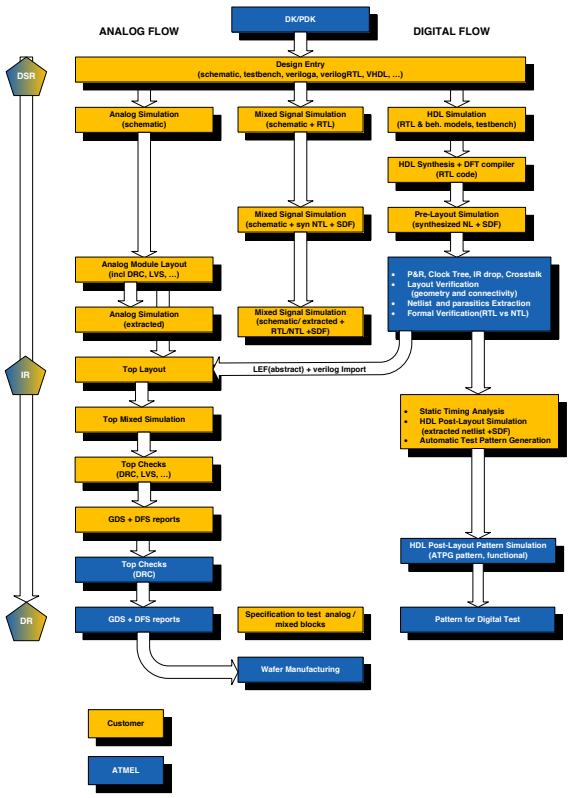


Figure 3: Development flow for analog-on-top ASIC

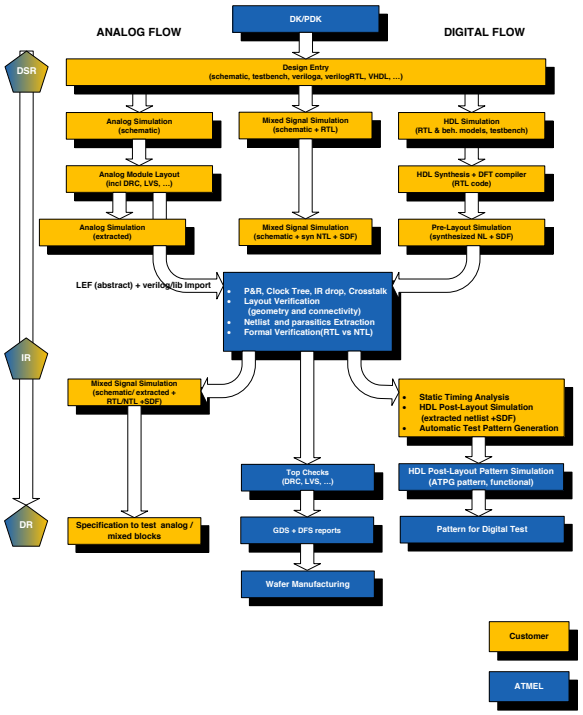


Figure 4: Development flow for digital-on-top ASIC

II. DIGITAL RADIATION STATUS

ATMX150, digital, has been tested against radiation TID, SEL and SEU. Radiation Report is available under NDA signature for users of thee technology. The overall results are on line or better than the previous technology ATC18RHA.

III. ANALOG RADIATION DESIGN

The analogue cells are tested as elementary cells in a test chip allowing individual test of each cell and the test of the combination of the cells. Electrical characterisation will be finished end of 2016. Radiation test results will be available in H2/2017. The analogue cells are listed below:

IP name	Functionality	Main characteristics/interest
	Linear Voltage regulator	Linear 5.5V/2.7V to 1.8V 50mA
	Oscillator	10MHz +/- 10%
	PLL	40-450MHz
	Bandgap	1.25V
IORHA	**IO library (Full digital + analog) up to 5,5 V**	Programmable digital buffer ESD protection enhanced Performance (frequency) enhanced Reduced cell number
MUX8RHA	**Analog Multiplexer**	8 channel 10MHz bandwidth
REG200RHA	**Linear Voltage regulator (including a POR)**	5.5V/2.3V to 1.8V @200mA
OSCRC10RHA	**Clock Generator / Oscillator**	Programmable 4/8/10/12 MHz RC oscillator
PLL400MRHA	**Clock Generator / PLL**	PLL 8/200MHz to 40/450MHz
BG1V2RHA	**Voltage reference / BandGap**	1.25V bandgap voltage reference
HERMES	**Clock Generator**	3GHz clock generator based on injection locked oscillator
	Clock Generator / Oscillator	32kHz xtal oscillator (ascosc138)
	Clock Generator / Oscillator	20MHz xtal oscillator (ascosc136)
	Clock Generator / Oscillator	32kHz RC oscillator (ascrc091)
	I2C filter	Filter for I2C high speed protocol (ascbuffilteterd2)
	Voltage Regulator DC/DC	DCDC 5V to 2.5V 300mA
	PLL	10-200MHz
	ADC	24 bits
	DAC	24 bits
	Voltage Comparator	
	Power On Reset **Low Power Band Gap**	5ms delay

IV. OTHER FEATURES

IV.1. NVM

A 32kBytes NVM is under electrical and radiation qualification.

IV.2. HIGH VOLTAGE LDMOS

The 15V IO is using standard CMOS transistor.

ATMEL has develop 25V, 45V and 65V LDMOS. Transistors. Radiation characterisation is ongoing. It is the plan to develop full IOs with ESD ELT production. Based on

V. ASIC & ASSP PLATFORM

Using this flow an example of the use of this development platform is started for an ASSP as described the below figure. Starting form a validated architecture of a processor core with its bus matrix (dark blue), ATMEL can derives new version adding digital IPs using the libraries (light Blue), custom IPs (middle blue) and NVM or analogue block. The blue to green system control block on the left includes voltage regulators, PLL, oscillators, power management …

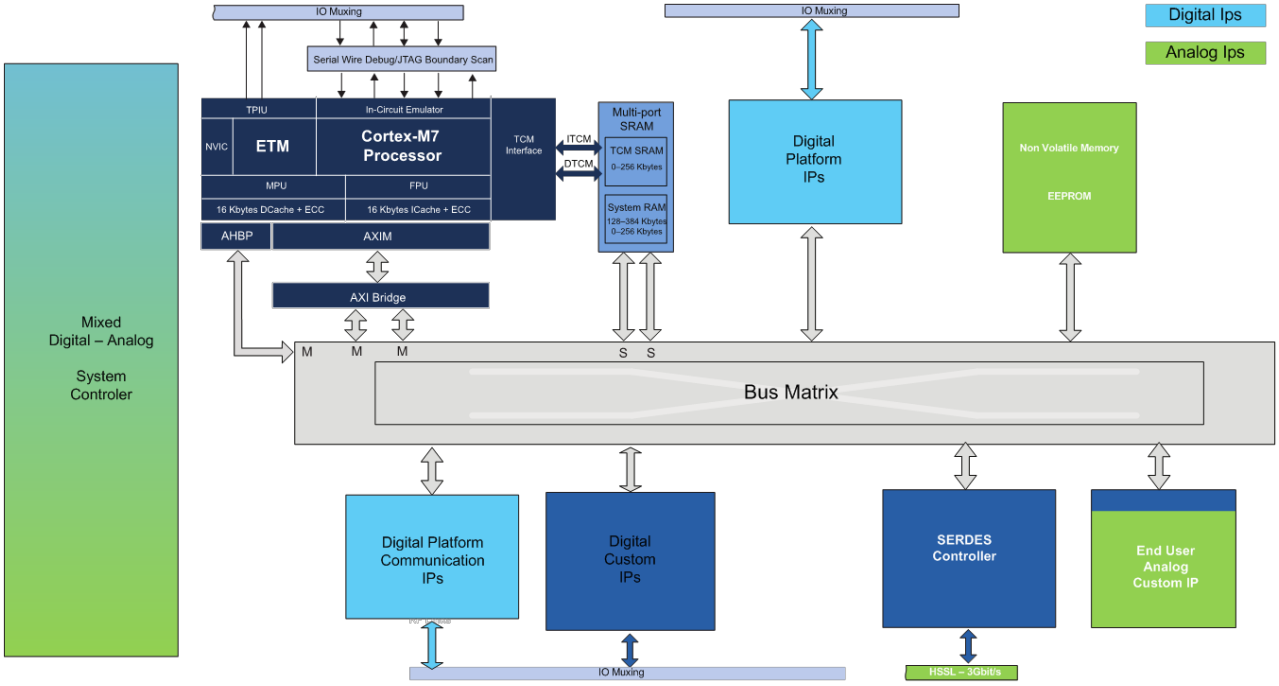
VI. CONCLUSION

ATMX150, digital, has been tested against radiation TID, SEL and SEU. Radiation Report is available under NDA signature for users of thee technology. The overall results are on line or better than the previous technology ATC18RHA.

The prequalified analogue IPs give a safer result and so limit the risk of re-spin. The integration of the analogue, NVM and HV with the digital improve drastically the overall cost.

An RF front end will be possible to add in the future.

The 150nm keeps an affordable access to the technology.



AMICSA: Radiation Effects on analogue and mixed-signal ICs

Single Event Simulation and Error Rate Prediction for Space Electronics in Advanced Semiconductor Technologies

K. Lilja[1], M. Bounasser[1], T. Assis[1]

[1]Robust Chip Inc. 7901 Stoneridge Drive #226, Pleasanton, CA, 94588 USA

Abstract: The effect of a single event in today's advanced semiconductor technology is no longer restricted to a single circuit node, and can depend strongly on layout details, on the angle of the ion, and on the response of the circuit during the charge collection. In order to catch weak spots in circuits and layouts, and to get reliable predictions for space error rates, it is important to have a possibility to model the circuit designs with a full (and correct) description of the layout, of direction of the ion, and of the time profile of the charge collection.

This paper discusses simulation techniques which makes this possible, while still being fast enough to be used to generate full cross-section maps and error rate predictions for different radiation environments. Application examples from advanced FinFET technologies (logic) and bulk technologies will be presented, along with comparisons to measured single event data. The application of the simulation techniques to remove or reduce the single event error rate will discussed.

***Index Terms*— Soft error, single event effect, radiation hardening, SET, SEU, layout optimization, LEAP, RHBD**

I. Introduction

In today's most advanced semiconductor manufacturing technologies the effect of a radiation generated single event extends over many individual devices in a circuit. This leads to new effects and requires more advanced analysis methods and new techniques for hardening against radiation. It also increases the rate of multiple errors, multi bit upsets (MBUs), in the circuits. The MBU increase, along with the sheer increase of size and complexity, cause the overall rates of radiation generated errors of chips and systems to go up, and increase the importance of estimating and controlling radiation effects, not only for space applications, but also for critical terrestrial applications.

The fact that a single event affects several devices, i.e., several nodes in a circuit, means that the relative placement of the devices and their contacts can have a very strong impact on the radiation sensitivity. To reliably capture these effects in simulation and prediction of single event effects it is essential to use methods with an a priori dependence on the layout.

Both the analysis and mitigation of single event errors also have to adhere to the stricter design rules and design hierarchy of modern chip design, which leaves little, or no, room, for customization. Qualified radiation hard building blocks (standard cells and other IP) which seamlessly can be inserted in the design flow alongside other (not hardened) circuitry, is required to enable cost and time effective radiation hardening.

II. Prediction Techniques: Simulation

In order for a simulation technique to capture the effects of the layout on a single event in a predictive manner, it is preferable to use a model which remains valid regardless of the particular layout used, i.e., a model based on the underlying physics of charge generation and transport, such as the semiconductor transport physics models used in traditional TCAD device simulation. Traditional device simulation, however, is too computationally intensive to generate sufficient information about the single event behavior of a circuit (cross-section, error rates, etc.), which requires a large number of individual single event simulations in a complex 3D structure with many devices. To alleviate this a hybrid device simulation method has been developed [l][2], which still includes a full representation of the 3D structure, of the simulation of the charge generation and transport therein, and of the contacts and the layout, but permits the simulation of the electrical device characteristics to be run using the circuit compact models (Figure 1).

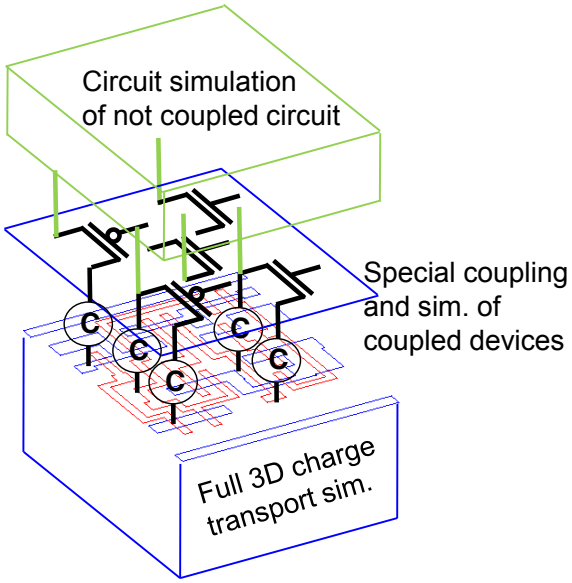


Fig. 1. Illustration of the specialized (hybrid-) single event devices simulation in the tool Accuro [2].

This single event device simulation method is capable of simulating a single event between 10-100X faster than regular

traditional device simulation, while maintaining the accuracy and predictive capability of full device simulation. This still makes it considerably slower than pure circuit simulation, but one simulation of a single event in a small to medium circuit can be done in minutes, and it can also handle much larger circuits (as much as several hundred devices can be included in the 3D structure). The method makes it possible to run the large number of individual simulations (1000-100,000) required to generate full cross-section and cross-section maps.

Since the simulation contains a full description of all doping regions, it fully captures latch-up and other bipolar effects as well.

Figure 2 shows an example of a simulation structure, used in this type of simulation, of a redundant flip-flop (FF) in an advanced FinFET technology. It captures the device placement, layout, and doping of the FF and its' surrounding. But, through the use of special models at the contacts, makes it possible to simplify the details of the individual devices and used the circuit compact models to model the electrical device behavior.

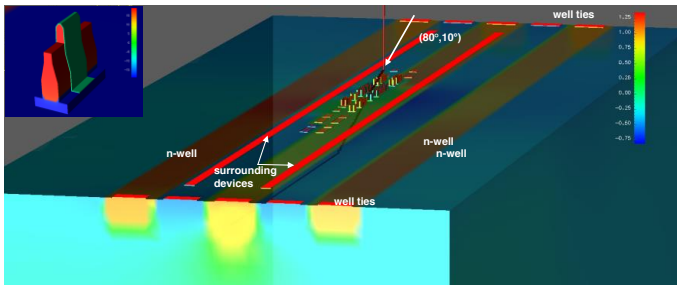


Fig. 2 Snap-shot from the modeling of a LEAPDICE flip-flop in 14nm FinFET technology. The figure shows the potential distribution (partially transparent) during the early phase of a single event at an incident angle of (80°,10°)..

III. Prediction Techniques: Error Rate Estimation

The simulation technique described in section II is capable providing the cross-section function, $\sigma(\theta,\varphi,LET,S)$, of a small to medium circuit as a function of the LET and the angles of incidence, θ and ϕ, (and of the circuit state S), and the simulation results can be verified directly to measured cross-sections at specific LET values and angles of incidence (section IV shows some selected examples).

If the cross-section is known, it can be applied to calculate the expected error-rate under a certain particle flux spectrum, $f_{flux}(\theta,\varphi,LET)$, measuring the differential flux per unit area and steradian as a function of LET and spherical angles;

$$ErrorRate = \int dLET \int_0^{\pi} \sin\theta d\theta \int_0^{2\pi} d\varphi \left\{\sigma(\theta,\varphi,LET,S) f_{flux}(\theta,\varphi,LET)\right\} \quad (1)$$

and it can of course be applied to compare the single event error rates of different circuit cells, and different layouts for the same circuit.

However, it also provides a lot of additional information, which is not accessible from measurements, such as the detailed current and voltage waveforms in the circuit during the single event and information about where in the layout the errors were generated. The latter information, the sensitive regions, make up the cross-section map of the circuit, $\sigma_{map}(\theta,\varphi,LET,S)$.

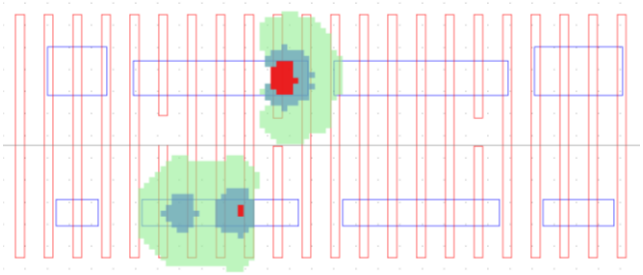


Fig. 3. Example of a cross-section map showing the sensitive regions for normal incidence (0°,0°) and LET values 2 (red), 20 (blue), and 100 (green) for a certain circuit state in a flip-flop cell.

A. Multi-bit upset prediction

The cross-section maps are helpful in understanding the single event behavior of a particular layout, but are strictly not required for the calculation of error-rates of the individual cell. They can, however, be used very efficiently to predict multibit error-rates. As illustrated in Figure 4, the cross-section for multibit upset (as a function of angle and LET), for two, or more cells, placed at certain positions can simply be evaluated by finding the overlap of the cross-section regions of the cells.

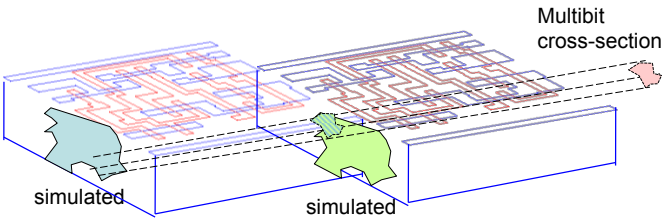


Fig. 4. Illustration of multiple-cell cross-section calculation. For every direction the overlap of the cross-section regions (for the specified criteria for each cell) is calculated to give the overall cross-section of the ensemble of cells (here for the criterion 'cell0 AND cell2').

Since the simulation generation of a cross-section map does require considerable computation resources, it is essential to have a way to interpolate the cross-sections between angles, i.e., not just an interpolation of the cross-section value, but of the actual sensitive regions. The tool Accuro [2] provides such a feature. It utilizes all information from all simulated angles in order to generate the maps (sensitive regions) for all other angles. Figure 5 illustrates this capability showing two

interpolated cross-section maps at (60°,30°) and (60°,60°) generated from simulated maps at (60°,0°) and (60°,90°) (shown in the figure) and (0°,0°), (90°,0°), and (90°,90°).

While this map interpolation is a quite complex process, it is, of course, very much faster than the generation of the simulation results for the original simulated angles. The generation of an interpolated cross-section map takes at most a few seconds per angle, and can easily generate a full cross-section map with a high angle resolution.

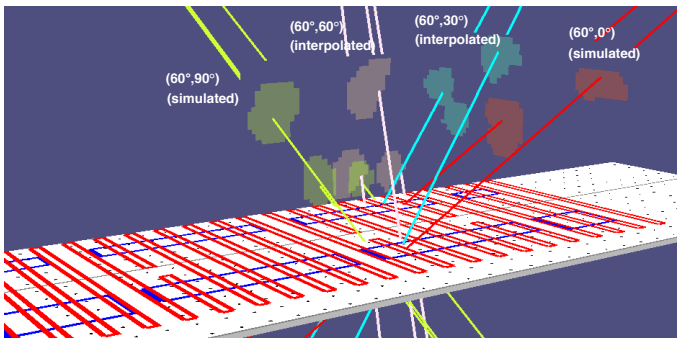


Fig. 5. Illustration of map interpolation including interpolated cross-section maps at (60°,30°) (cyan) and (60°,60°) (grey).

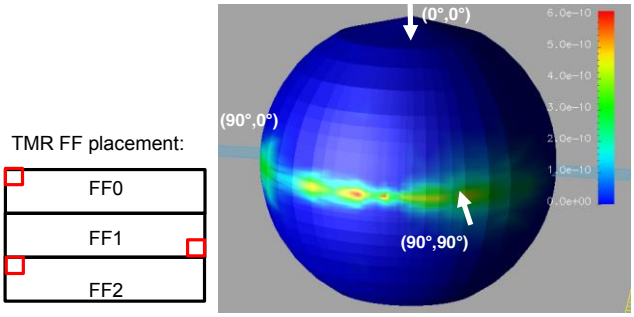


Fig. 6. Example of the cross-section (color-coded as a function of angle) of a TMR placement (left) of 3 flip-flops as a function of angle for a certain state (here state1) and LET (here 20 MeVcm^{2}mg^{-1}).

An application example of the cross-section interpolation and multibit prediction is shown in Figure 6. Here three flip-flops in a triple modular redundancy (TMR) configuration are placed in different positions relative to each other (one of which is shown in the figure), and the upset is determined by the condition that at least two of the flip-flop are upset (which would upset the TMR). As can be seen in the figures, the cross-section for the TMR configuration is zero (blue color) at normal incidence, and the only contribution comes from radiation with tilt angles close to 90°

IV. Selected Comparisons to Measurements

The accuracy of the simulation technique has been verified extensively against single event measurements in bulk technologies from 180-20nm, and SOI technologies from 45-28nm. Figures 7 shows an example from a 28nm bulk technology and Figure 8 show a comparison for unique measurement data taken at 91° tilt angle in a PDSOI technology.

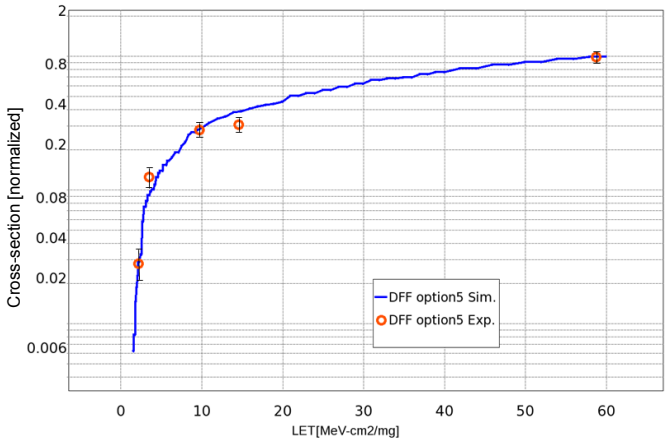


Fig. 7. Normalized experimental data (markers) and simulation (line) for a regular (not redundant) DFF in 28nm bulk technology [1].

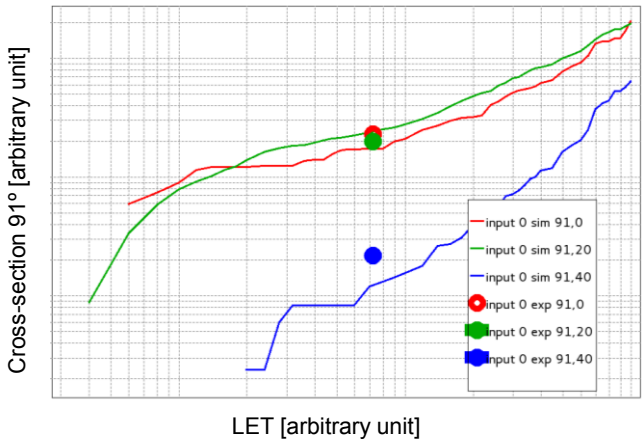


Fig. 8. Comparison of sim. and measured cross-sections for a DICE type flip-flop in 32SOI (91° tilt, 0° 20° 40° rotation, nominal supply voltage, blanket pattern 0). Data from [4].

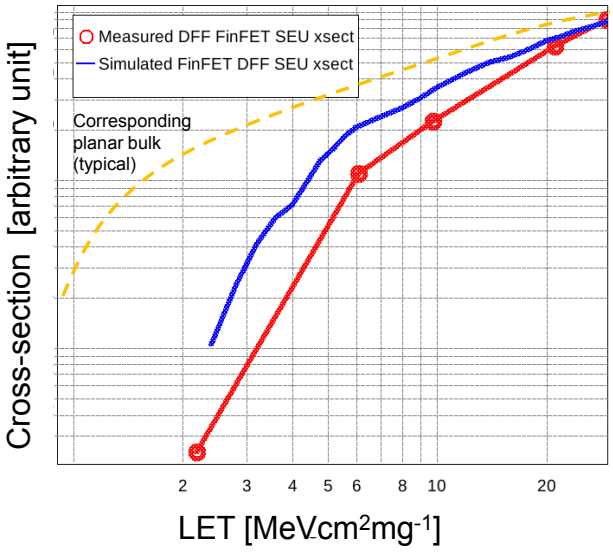


Fig. 9. Comparison of (un-calibrated) simulated and early measured results for the cross-section of a DFF in 16nm bulk FinFET technology [5].

At the 16nm and 14nm FinFET technology nodes comparisons to early measurement data indicate that the basic (un-calibrated) simulation model gives a decent agreement, but that there are deviations at low LET values (Figure 9).

V. RHBD TECHNIQUES: LEAP

Perhaps an even more important aspect than the error rate prediction is the support the advanced single event simulation provides for the design and optimization of efficient radiation hardened cells, and other basic building blocks. In the development and optimization of ultra-hard logic cells using the Layout design through Error Aware Positioning (LEAP) technique [1][6][7], discussed in this section, the advanced simulation has provided critical information and insight.

The fact that a single event, in an advanced technology, affects many devices and circuit nodes does not only create problems; it can actually be utilized as a hardening technique which can provide extraordinary error rate reductions. The LEAP method takes advantage of the charge sharing by rearranging the layout and the placement of the devices.

LEAP is applicable to sequential logic, combinational logic, as well as other applications (e.g., analog). The penalties in area, speed, or power can be kept very small. The technique is particularly effective for circuits and layouts that use redundancy where consistent error rate reductions of 100X or more (vs. a traditional layout implementation for the same redundant circuit), has been obtained in bulk, SOI, and FinFET technologies from 180nm to 16nm (resulting in three to four orders of magnitude error rate reductions vs. regular (not-hardened) logic).

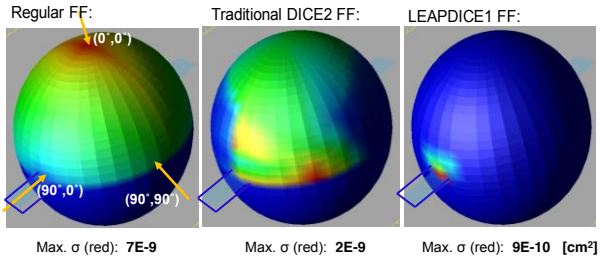


Fig. 10. Spherical plot of the cross-section as a function of incoming angle at an LET of 16 MeVcm^{2}mg^{-1} in 28nm technology.

Figure 10 illustrates how LEAP can reduce both the solid angle of incidence where the circuit is sensitive to radiation, and the value of the cross-section at the most sensitive direction. The left-most figure shows the cross-sections for the (non-redundant) DFF. This flip-flop can be upset at any angle of incidence, with a maximum cross-section at normal incidence and the smallest cross-section at a grazing angle along the long side of the layout (θ=90°, φ=0°/180°). The center figure shows the cross-sections for the traditional DICE flip-flop. At LET=16 MeVcm^{2}mg^{-1} the maximum cross-section for this FF is at θ=90°, φ=325°, but it has non-zero cross-section at normal incidence. The right figure shows the LEAPDICE, where the LEAP technique has reduced the non-zero cross-section to a small angle cone around θ=90°, φ=0°/180° for all LET values.

A. LEAP at low supply voltage conditions

Figure 11 shows recent SEU measurement results for redundant flip-flops implemented with and without the LEAP technique. These early measurement results have a very poor statistics (and further measurements are under way), but they indicate (along with initial results in other technologies) that the LEAP technique maintains its' efficiency down to very low supply voltages and makes it a good candidate for the generation of logic for Near Threshold Computing (NTC) applications.

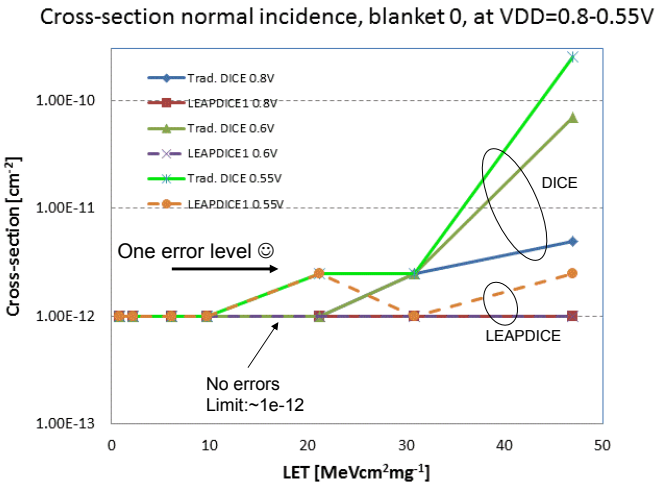


Fig. 11. Early measured SEU cross-section of a regular-layout, and LEAP-layout, DICE flip-flops at different supply voltages in an advanced FinFET technology [5].

B. LEAP flip-flops and logic

Custom LEAP flip-flops, and certain other logic, have been generated and applied in many different semiconductor technologies (and tested – confirming the extraordinary error rate reductions). Table I provides an overview.

Table 1. Overview of LEAP based logic cells.

	Implemented / Exp. Verified	SER reduction	Status / Availability
Technology	Type		
180nm bulk	LEAP FFs	10000X	Test chip & custom impl.
28nm bulk	LEAP FFs	5000X	Test chip & custom impl.
20nm bulk	LEAP FFs	5000X	Test chip verific.
32nm PDSOI	LEAP FFs, LOGIC	4000X	9T std. cells [1)]
28nm FDSOI	LEAP FFs, LOGIC		Test chip verific.
16nm FinFET	LEAP FFs	5000X	Test chip verific.
14nm FinFET	LEAP FFs, LOGIC	5000X[2)]	9T std. cells [3)]
[1)] FFs (Scan, P, C), clk-tree buffers			
[3)] FFs (Scan, P, C), buffers - testing and test chips in progress 2016			

For an efficient application in today's most advanced technologies, where, as discussed in the introduction, there is little room for customization, LEAP hardening is preferably introduced in form of basic pre-qualified building blocks (standard cells and certain other IP) which seamlessly can be inserted in the design flow alongside other (not hardened) circuitry. Such IP is now available in some advanced technologies (and in the process of being qualified).

VI. Application to Combinatorial Logic

The advanced simulation technique can be applied effectively to the analysis of single event transients (SET) in combinatorial logic. By changing the "event" criterion to monitor the SET pulse and recoding the pulse widths during the simulation, cross-sections and error (pulse-) rates which are functions of the SET pulse width are generated in the same manner as the SEU cross-sections and error rates.

Under most circumstances the combinatorial logic gives a much lower contribution to the overall single event error rates (than memory and sequential logic) and is not the primary target for hardening. However, the efficiency of the LEAP RHBD technique for the hardening of combinatorial logic has been experimentally verified for a number of different combinatorial logic circuits [8][9][10].

VII. Application to Analog and Oscillatory Circuits

The advanced simulation technique is directly applicable to analog and oscillatory circuits as well (with an appropriate modification of the "event" criterion, e.g., to monitor SET pulses or frequency and phase distortions). However, if the circuit response is complex, requires long simulation times, and introduces additional variables (e.g., the event time-point for oscillatory circuits), the generation of a complete cross-section function and map may become to time consuming.

Conclusion

Advanced simulation techniques can capture the complexity of a single event response in today's most advanced semiconductor technologies, and provide accurate predictions for single event cross-sections and error rats. The simulation provides critical support for design of hardened electronics in these technologies. The single event behavior in these technologies requires new or modified approaches to radiation hardening The LEAP RHBD technique is an example of such a technique and its' extraordinary efficiency has been verified experimentally down to the 16nm FinFET technology node.

Acknowledgment

Robust Chip Inc. gratefully acknowledges support from the Defense Threat Reduction Agency under contract HDTRA1-12-C-0093 and HDTRA1-13-C-0063 for this work.

References

[1] K. Lilja, M. Bounasser, S.-J. Wen, R. Wong, J. Holst, N. Gaspard, S. Jagannathan, D. Loveless, and B. Bhuva, "Single-Event Performance and Layout Optimization of Flip-Flops in a 28-nm Bulk Technology," *IEEE Trans. Nucl. Sci.*, Vol. 60, No. 4, pp. 2782-2788, August 2013.

[2] www.robustchip.com

[3] K. Lilja, M. Bounasser, S.-J. Wen, R. Wong, L. Chen, S. Baeg, N. Mahatme and B. Bhuva, "Logic Cells with Ultra Low SEU and SET rates in 20nm and 28nm Bulk Technologies Using Layout Optimization", NSREC 2014, to appear in *IEEE Trans. Nucl. Sci.*

[4] M. Cabanas-Holmen, E. H. Cannon, Salim Rabaa, T. Amort, J. Ballast, M. Carson, D. Lam, R. Brees, "Robust SEU Mitigation of 32 nm Dual Redundant Flip-Flops Through Interleaving and Sensitive Node-Pair Spacing", *IEEE Transactions on Nuclear Science*, Volume 60, No 6, 2013

[5] K. Lilja, et.al., "SER Prediction in Advanced FinFET and SOI FinFET Technologies; Challenges and Comparisons to Measurements", SEE MAPLD Symposium, La Jolla, CA, 2016

[6] Patent US 8,566,770 B2, US 8,468,484 B2, Robust Chip Inc.

[7] K. Lee, K. Lilja, M. Bounasser, P. Relangi, I. R. Linscott, U. Inan, S. Mitra, "LEAP: Layout Design through Error-Aware Transistor Positioning for Soft-Error Resilient Sequential Cell Design", *Proc. IEEE Intl. Rel. Phys. Symp.*, pp.203-412, 2010

[8] R. Quinn, et. al., "Heavy Ion SEU Test Data for 32nm SOI Flip-Flops", IEEE NSREC 2015 conference (to appear in *IEEE Trans. Nucl. Sci.*)

[9] R. Quinn, et. al., "Frequency Trends Observed in 32nm SOI Flip-Flops and Combinational Logic", IEEE NSREC 2015 conference (to appear in *IEEE Trans. Nucl. Sci.*)

[10] K. Lilja, et.al., "SEU and SET Measurements for Hardened Sequential and Combinatorial Logic in 32nm SOI Technology", SEE MAPLD Symposium, La Jolla, CA, 2015

AMICSA: Implementation of Radiation Hardening on analogue circuits at cell-, circuit-, and system design level

Using a Standard Commercial Process for Full Custom Rad Hard Mixed-Signal Design

S. Millner[a] , A. Zoller[a], V.Lueck[a]

[a]Tesat Spacecom, Gerberstraße 49, D-71522 Backnang, Germany

Sebastian.Millner@tesat.de

Abstract

A mixed signal design flow aiming at rad hard, qualifiable designs on a commercial unhardened process is presented[1] This is done by analyzing deficiencies of the process concerning radiation and mitigation on system, circuit and concept level. Methods of analyzing possible weak points already in the design or prototype phase without irradiation are presented.

I. Introduction

Mixed-signal design allows integration of further external discrete components and hence continues the dividend of integration. However, implementation of a mixed-signal flow into an operating digital or analog design flow is not a straight forward task. In space applications in addition, radiation is always an issue and ways need to be found to mitigate its effect on the circuit. Libraries using modified specialized layouts exist to create rad hard designs for digital and analog functions [1]. Companies offer complete flows from design to supply chain using pre-designed building blocks to qualified devices using proprietary libraries[2][3].

Indeed, these solutions can be very efficient and minimize the risk as used library components might be working in several other designs. However, if application constraints the design to other requirements than implemented within the library cells, full custom solutions might be required to obtain the full benefit of mixed-signal. In addition to the limited availability of analog library cells for space application at the beginning of design, this has been one of the main reasons for the necessity of full custom design in our applications.

We start with a short introduction into our design flow followed by radiation hardening / awareness approaches on system, module and process level. Afterwards we give a short sample of a design currently in development. The paper is closed by a short outlook into supply chain implementation.

II. Design Flow

Before going mixed-signal, our design flow has been focused on digital designs only and several digital ASICs and FPGAs have been successfully created. One of the main requirements was that the new analog functionality should integrate into the digital flow while preserving it. In addition, our mixed-signal designs usually have a huge amount of digital cells integrated. Consequently, the decision has been to work with a digital-on-top flow. The major design reference is a VHDL-netlist and the final layout is done using a place-and-route tool and not the full custom analog layout tool. This way, the timing information between digital sub-cells like IO-cells, a possible digital core and memory macros is in control of the digital tools and not a full custom designer only. SDF-based verification on top-level remains possible. Furthermore, the exact shape of the digital core can be adjusted easily to fit into the remaining area after placement of the analog macros. Long parallel digital interconnection buses do not have to be drawn manually with a large effort, but are drawn by the place-and-route tool.

A. Working with analog IP

The digital on top flow with instantiated analog macros offers to work with analog IPs on the long term. As a matter of principle, the operation of implementing a memory macro can be similar to the implementation of an ADC for instance. It is instantiated within the digital netlist as a black box, with possible interface description or model and no dedicated analog tool chain would be required anymore.

Indeed, modeling of these analog IP is a challenge here. The straight forward way of using the spice netlist in a mixed signal design is costly on the on hand concerning license costs and simulation time. On the other hand, the spice netlist might not be available at all – for instance because it has not been developed or because the actual circuit hat to be kept secret from the user of the library. Hence, an alternative has to be found. This could be done by using AMS-models for instance, which would at least close the availability issue and possibly improve simulation time. However, if more abstract modeling is sufficient, a way might be to work with real number modeling. Indeed, here compatibility to tools like synthesis and mixed signal simulation need to be retained. Routing of analog signals through digital modules in mixed signal simulations can be prevented by the use of resolved real signals for instance.

A simple way of modeling is to keep the interfaces of mixed modules digital while working with real signals internally. This way, an ADC could be modeled for instance. However, this approach can be too abstract.

[1] This work contains results from the "New LCAMP Technologies" project (ESTEC contract. no. 4000111633/14/NL/EM). Responsibility for the contents resides in the author or organization that prepared it

B. Space dedicated standards for analog/mixed signal ASIC development

The ECSS standard for ASIC and FPGA development [6] fits best for digital designs and seems to be evolved on digital design bases. Lots of effort had to be spend to develop a design approach allowing e.g. concurrent engineering with layout and circuit design while still being conform to [6]. Furthermore, the while there are lots of guidelines / best practices concerning digital rad hard ASIC design, guidelines for analog designs are still evolving. An ECSS handbook is currently under development [5].

III. Radiation Hardening

The next question is how to obtain a qualifiable rad hard design. Here the approach has been to work with an available commercial process which is tolerant enough for TID and do mitigation for SEE on system and design level rather than modifying the process or its devices. Furthermore, no dedicated rad hard digital standard cell lib should be designed and radiation tolerance should be given at netlist level. This way flexibility to adapt to other processes is retained in principle.

A. Process evaluation

However, not all insufficiencies of the process can be taken care of at system or netlist level. This is why radiation behavior of the process needs to be observed during process choice. Individually checked devices have been white listed concerning total dose and SEE behavior. Our result has been that we can work with our technology applying the netlist mitigation techniques on digital cells. Further devices or macros which might be required have to be observed, in addition.

In our evaluated process, 3.3 Volts transistors and lower voltage devices could be used basically without total dose concerns. Significant drifts will occur at higher voltage devices. Consequently, they should be avoided where possible and should not be used in analog macros where the exact parameters are important.

On device level, no latch-up issues arose during single event testing.

B. Digital design

On the digital side we work with triple mode redundancy of memory and logic elements. This procedure keeps the devices clean from single events up to a certain threshold. However, as IO-cells might be a bottleneck in this case, we had to develop an own redundant IO cell to keep the complete path redundant. Possibly necessary macro cells have be treated with special care dependent on the application and their radiation behavior.

1) Mitigation on standard cells

Usually the standard cell registers will be sensitive to single event upsets. As no errors are allowed to remain within the operating design, the original state of a register has to be recovered. This can be done by developing dedicated redundant self recovering full custom standard cell registers. This might be the most efficient way concerning area and power consumption. However, it is expensive concerning the development effort and a process change would require new full custom cells. A cheaper way is to build redundancy using already available commercial standard cells. As cost efficiency has been one of the key parameters during our design decisions, this has been our way to go.

There are several ways of adding triple mode redundancy on netlist level. A straight forward way would be to instantiate the top level digital module three times and compare the results of the three instances. This way, the effort would be little more than three times the cells necessary in the un hardened design. However, the mitigation is limited as the designs would need to be synchronized at least after a hit. This procedure might not be possible. A periodic hit independent synchronization would enlarge the cross-section drastically.

Another way of adding redundancy is to compare the results after each register. This way synchronization is done at each clock cycle which minimizes the cross-section. However, this way of redundancy is expensive as comparison elements are necessary for each of the registers of the circuit. It is the closest to a full custom self-redundant register.

Redundancy at register level is implemented in our design. As a manual modification of the netlist would be error prone, the synthesized netlist is modified automatically. Margin has to be included in the timing of the not redundant netlist to retain a valid timing after redundancy insertion. Indeed, normally optimizations are not possible any more after insertion. Redundancy could be removed in this case.

2) IO-Cells

Early radiation test showed SEE sensitivity of standard IO cells available for our process. In addition, the redundancy approach done on register level is not possible on IO-Cell level at least for outputs. There has to be a position, where the triple-mode redundant signal is converted into a single signal.

The straight forward way of implementing three input cells, for each input is hardly feasible, as the IO-cell count and the required pad ring area would increase drastically. However, in core limited designs with a small pin count, it might still be possible.

Our way to get out of this misery is to develop an own IO-cell consisting of 3 standard IO-cells from the library. The pad and its ESD-structure are implemented without redundancy. However, starting with the first input buffer, the signal is redundant. This way a hit in any buffer in the IO-cell will not influence the calculations done within the ASIC. Unfortunately, this implementation is not possible for the output paths. Here a voting circuit would be necessary at least upstream the final IO-driver.

3) Macrocells

Similar to IO-cells, digital memory macros implemented as IP cannot be implemented with triple mode redundancy on a

low level, as they are fixed. A procedure here could be to work with EDAC. However it cannot be assured a hit only changes one bit of a word, as close by bits might be affected, too. If multi-bit upsets are expected, an EDAC might not be sufficient. Consequently memory macros need to be implemented redundant as block and ways to maintain the data have to be applied.

One way of data maintaining is to regenerate the data periodically. If the probability of an upset at the same bits of two memory blocks is sufficiently small, within this period, upsets are mitigated. However, usually it is not possible to regenerate the complete data. Here, a periodic refresh has to be performed. All memory cells are read and rewritten again. Evaluation of the redundancy assures correction of single event upsets. Again, the probability of a hit on the same bit of two macros needs to be sufficiently small. A clear disadvantage of this procedure is the occupation of a memory port during refresh. If only one port is available, this will enlarge access time drastically depending on the refresh period and scheduling of the mechanism.

If latch-ups in IPs like memory macros occur, there are several different methods of treatment. If a destructive latch-up occurs during normal operation, the macro cannot be used in normal operation. However, it still might be used for a very short time during start-up for instance as latch-up probability of the system would hardly be affected this way. During normal operation, the macro would need to be disconnected from power.

If non-destructive latch-ups occur, it might be possible to power-down one instance of a redundant memory after latch-up detection. After powering-up the macro again, the data can be refreshed automatically by one of the mechanisms above. Indeed redundancy would not be given any more during a power cycle and the following refresh of one instance. Single bit upsets might be stored in all three instances during refresh. Again, this vulnerable time needs to be kept short enough to sustain a sufficiently low upset probability.

Unfortunately, the radiation performance of IP macros will usually not be available before first prototypes are irradiated as no data is available for commercial IP not dedicated for space application. Evaluation of the function applied, or the necessity additional mitigation methods will arise after first prototyping. The risk of not being able to use a macro at all will remain, too until measurements have been performed.

C. Analog design

For analog cells, treating SEEs is less straight forward. As we are doing full custom design, we do not know the SEE behavior of the circuits before. There are mitigation techniques like enlarging time constants or working with analog redundancy. For analog redundancy, the analog signals can be voted e. g. by resistive networks interconnecting the outputs of redundant circuits. However, the complete circuit would be basically n times as big as the initial circuit and enlarging a circuit and its current can lead to the same results. The most important thing is radiation aware design. The possible impact needs to be taken into account.

We used several approaches to analyze the circuit for radiation aware design. One is to inject charge onto all nodes of few critical circuits during simulations, which is very extensive indeed. Furthermore we apply techniques on system level to mitigate SEE effects or to include them in the design. A third method is to include laser test in early prototyping stage to get a figure of the expected radiation behavior.

1) Charge injection simulation

The actual shape of the current pulse injected at a node during a single event differs when going to modern technologies with shorter channel lengths. We implement a model sufficient for older technologies which is presented in [4] for instance:

$$i_{node} = \frac{q}{(\tau_\alpha - \tau_\beta)}\left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}\right)$$

The shape of the pulse for different amounts of charge can be found in the next figure:

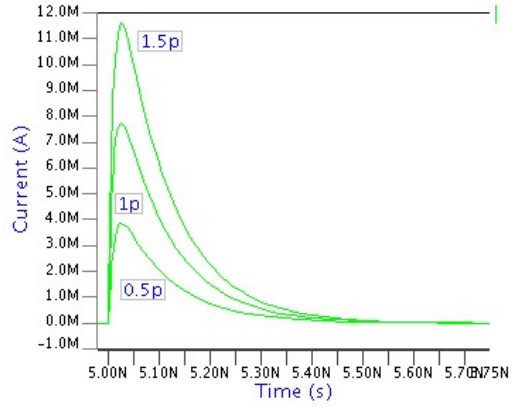


Figure 1: Current pulse for single event simulation

During our verification, we work with typical values of $\tau_\alpha = 100\,ps$ and $\tau_\beta = 10\,ps$. As charge, 1.5 pC have been taken which should correspondent to an LET of about 100 MeV/mg/cm³, however quantitative results are hard to rely on with this model. We use this method to get a rough view which nodes are vulnerable to get a starting point for mitigation. The parameters have been tuned to reproduce effects on inverter chains, which have been irradiated.

In practical simulation, a single transient simulation is done for each node of the circuit with a current source of i_{node} at the corresponding node. The insertion of the current sourced is done automatically after netlisting.

A sample simulation result, can be found in Figure 2:. Here a simple two stage OTA connected as buffer is simulated. Stimulation is done with the current pulse from Figure 1: at the high impedance output of the input stage, which is the most vulnerable node here.

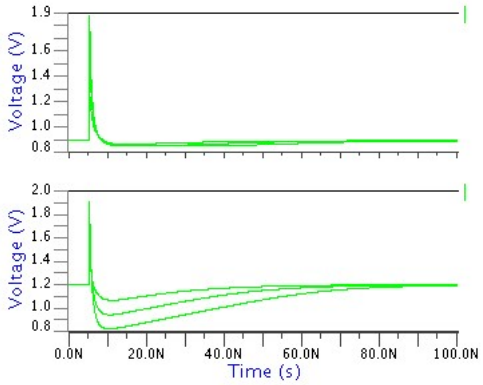


Figure 2: Single event simulation of a buffer connected two stage OTA at the high impedance node of the input stage (upper curve). The lower curve is the output of the OTA.

As the stimulated node is high impedance, the injected charge cannot be removed fast by the circuit, and the effect at the output is massive.

An issue occurring to this verification method is the simulation time. On the one side, the transient simulation has to be done for each node of the circuit. On the other hand, it has to be quite accurate as the time constants are small. The maximum time step of the simulation should be in the same order of magnitude. Else the current pulse might not have any effect on the circuit. Consequently, the simulation can only be performed for very critical circuits, like references, etc.

2) System level mitigation

Some level of mitigation of single event effects can already be done at system level. This is done by evaluation of allowed level of disruption caused by single event transients on analog signals for instance. Furthermore working with long time constants and large blocking capacitors at DAC outputs for instance will decrease the sensitivity against SETs. Measured values from ADCs on the other hand can be read several times to exclude incorrect measurements.

IV. Radiation tests

In addition to the necessary heavy ion tests and total dose tests, we are working with laser tests to get qualitative figures of possible weak spots of the ASIC. Indeed, the shape of the charge pulse created by a laser pulse might differ a lot from the pulse created by heavy ion irradiation. The length of the pulse might be different from Figure 1: for instance.

However, experiments have shown that it is possible to reproduce see effects on dedicated circuits using our laser test method. Consequently, our laser tests are a valid method to do SEE analysis before or after heavy ion irradiation. A great advantage here is the ability to do local stimulation. This way it is possible to locate the specific source of globally measures SEE-effects like latch-ups for instance.

V. Design example

A mixed signal ASIC has been designed were most of the discussed methods have already been applied. A first prototype of this ASIC exists and is currently in the lab for evaluation. Some key parameters of this ASIC can be found in Table 1:. A photo of the die is shown in Figure 3:.

Table 1: Key parameters of mixed-signal ASIC

Parameter	Qantity
Process	180 nn XFAB
Size	6 mm x 6 mm
Pins	132
Digital complexity	>150k Standard Cells
Third party macros	2
12 Bit DACs	24
12 Bit ADC	3
Analog regulator	10
Analog sensing	2
linear regulator	4
Power domains	>5

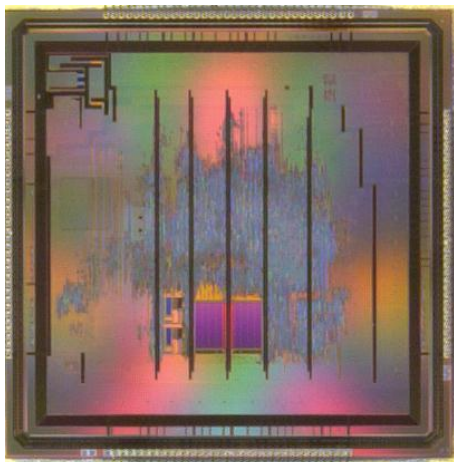


Figure 3: Die photograph of mixed signal ASIC

VI. Outlook: Supply Chain

Indeed, design life only starts with the finalization of the prototype into the production design. Finally, a complete supply chain has to be build. However, as this step is not part of the development it-self, it is not covered by the ECSS-Q-ST-60-02C [6].

Here we see at least two different ways of proceeding: Using the supply chain of external subcontractors who supply completely tested and packaged dies, or building up an own supply chain. The latter one might be more complex at the beginning, but this way all steps of e. g. qualification remain under control.

VII. Conclusion

We have presented our approach of developing mixed signal ASICS for space applications working on a commercial

process. Different ways of mitigating occurring radiation issues on system and circuit level have been shown.

Remaining challenges are efficient modeling of IP-like analog circuits within digital simulations and systematic hardening during analog design. Implementation of fixed Macros is a challenge, too, as radiation performance cannot be evaluated before testing and systematic approaches are limited as the IP cannot be changed.

The next step will be application of all concepts in a first prototype and finally qualification this device.

VIII. ACKNOWLEDGEMENTS

The authors would like to acknowledge the ESA/ESTEC ARTES 5.1 program for funding part of this work.

IX. REFERENCES

[1] Franciscatto G. et al., DARE180X:.A 0.18um mixed-signal radiation-hardened library for low-power applications, presented at AMICSA 2014

[2] Steinkamp J. et al., 180nm CMOS Mixed-Signal Radiation Hard Library as base for a full ASIC supply chain, presented at AMICSA 2014

[3] Briot V. (ATMEL), ATMEL mixed signal space offer: SOI 150nm radiation hardened process. Presented at AMICSA 2014.

[4] Garg,Rajesh et al., Analysis and Design of Resilient VLSI Circuits, Springer 2010

[5] Space product assurance Technique for radiation effects mitigation in ASICs and FPGAs handbook.

[6] Space product assurance ASIC and FPGA development - ECSS-ST-60-02C, July 31th 2008

Radiation Hardened by Design Pipeline Analog-to-Digital Converter Blocks in CMOS HV 0.18µm Technology

L. Perbet[a], O. Bernal[a], H. Tap[a]

[a]LAAS-CNRS, Université de Toulouse, CNRS, INP, 31000 Toulouse, FRANCE

bernal@enseeiht.fr

Abstract

In this paper, we present an approach to achieve radiation hardening by design (RHBD) for the main three blocks involved in pipelined Analog-to-Digital converters (ADCs): switches, comparators and residue amplifiers. A method to design bootstrapped switches has been devised to avoid voltage overshoots. Dual path with auto-zero techniques have been implemented for the comparators to be less prone to single effect upset (SEU). Finally, predictive switched capacitor techniques have been used for the residue amplifier in order to benefit from a simpler low-power amplifier architecture. To verify the proposed methodology, these blocks were implemented in an HV 0.18µm CMOS technology.

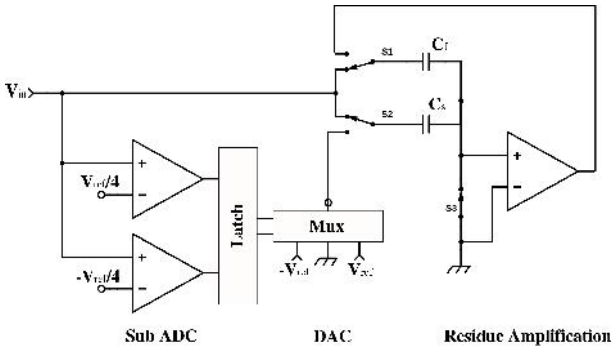


Figure 1: Pipeline stage with 1.5-bit resolution

I. INTRODUCTION

CCD sensors embedded in satellites need not only to convert analog signals into digital ones with high precision and speed (11-14 bits at 5-20 MS/s) but also to be radiation hardened due to the space environment. To achieve such performances, pipeline analog-to-digital converters (ADCs) are usually employed.

The pipeline ADC is an N-step converter consisting of M stages connected in series with a few bits being converted by each stage. Usually a 1.5-bit or 2.5-bits resolution is preferred for the most significant bit stages as it allows efficient digital calibration techniques to be performed. Fig. 1 shows a classical 1.5-bit stage architecture.

As shown in Fig. 1, ADC performance relies on switched-capacitor (SC) techniques. In such SC circuits, CMOS switches, comparators and amplifiers are critical components and their characteristics directly affect the linearity, the bandwidth and the power consumption.

Regarding CMOS switches. bootstrapped structures similar to [1] are often used. This technique allows not only to use the switch with low-voltage power supply but also lessen signal distortion by strongly reducing its signal-dependent On resistance. Such an improvement is obtained by keeping constant the switch overdrive voltage independently of the signal input voltage. Further, in order to eliminate the remaining non-linearity induced by the body effect on the MOS transistor threshold voltage, different methods were proposed such as by applying a controllable input signal factor to the gate of the main switch [4] or by biasing techniques of the body if the technology process allows it. In addition to the previously mentioned advantages of such bootstrapped architectures, charge injection effects due to the carrier release when the MOS transistor switch is turned off, are also significantly reduced since they are less dependent on the input signal voltage to be sampled. However, to maintain a proper overdrive voltage across the gate of the MOS transistor switch, voltage higher than the maximum power supply voltage are applied. Even if the previously mentioned bootstrapped techniques also aim at maintaining CMOS process stress as low as possible, it might not be sufficient to ensure that the switch can withstand a radiative environment. In particular, three main radiation effects should be taken into account carefully: total ionizing dose, latch-up and single event gate rupture SEGR [2]. In this paper, an approach to avoid voltage overshoot greater than the power supply will be presented.

As far as the comparators are concerned, an auto-zero dual path approach has been implemented so that the architecture could be less prone to SEU [3].

Finally, to achieve high linearity, class AB high-gain amplifiers are usually employed. To enhance the amplifier open-loop gain, more or less complex architecture based on cascoding techniques with two or more stages can be used. Such an inherent architecture complexity not only induces higher power consumption but also a lower reliability regarding radiation. It can thus be interesting to use SC gain-enhancement techniques to benefit from a simpler low-gain amplifier structure [4]-[6]. Here, to demonstrate such an approach in a radiative environment, a predictive technique based on correlated double sampling (CDS) has been used to reach a 66dB open-loop amplifier based on a 46dB open-loop gain amplifier.

II. Proposed RHBD Approaches for an ADC Pipeline Stage

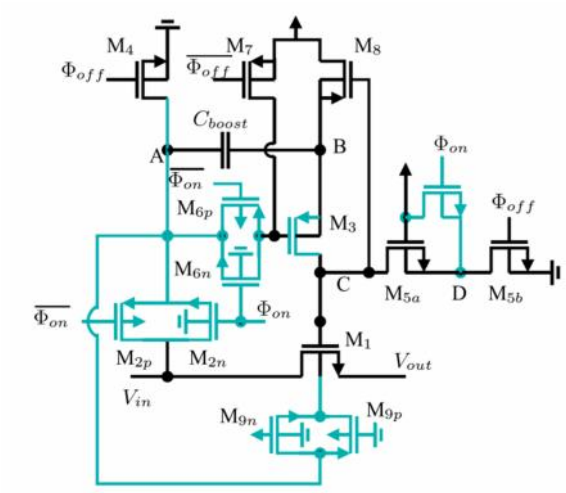


Figure 2: Proposed Bootstrapped Switch Schematic (proposed improvements in lighter tone)

A. Bootstrapped Switches

The proposed bootstrapped switch is shown in Fig. 2 where the modifications are highlighted to facilitate the comparison with a conventional bootstrapped switch. In order to use bootstrapped switches in a radiative environment, the following voltages should remain within the technology specifications (and for safety margin usually the maximum differential voltage is set to V_{dd}) at any time:

- the gate-body voltage V_{gb}^{M1} of M1. This implies that the body cannot be tied to ground but should depend on V_{in}.
- the gate-source voltage V_{gs}^{M1} of M1. A careful design should take into account the worst case with V_{out}=0 at the beginning.
- the V_D voltage is not accurately controlled and might be higher than V_{dd} (V_{gd}^{M5B}).
- the drain-body voltage V_{db}^{M5A} of M5A.

As in [7], the body of M1, M2 and M5 are thus tied to the source in order to alleviate voltage stress. However, those changes do not guarantee that all the voltages are lower than V_{dd} all the time. As explained in [8], the worst case corresponds to V_{in}=V_{dd} and V_{out}=0. To ensure that V_{CA} is always lower than V_{dd}, the change rate of V_C should match the one of V_{out}. It was shown that the maximum change rate of the gate voltage of M1 can be expressed as follows:

$$\left.\frac{dV_{GM1}}{dt}\right|_{\max} = \frac{V_{dd}}{\tau_{M1}}$$

where the time constant τ_{M1} is related to the charge of the gate of M1. The size of M3 should be subsequently well defined and a method to estimate its size has been devised in [8]. Further, when the switch is turned off, the voltage change rate of the body of M1 should match the gate voltage change rate. The simulation results (Fig.3-4) highlight the importance of the size of M3.

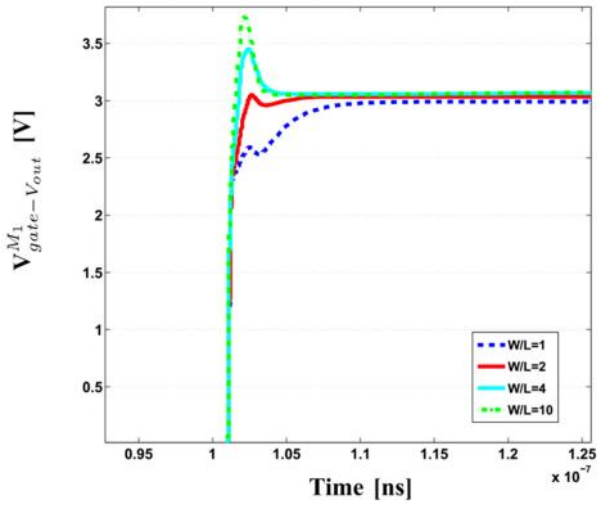


Figure 3: Simulated V_{M1} gate - V_{out} voltage for different size of M3

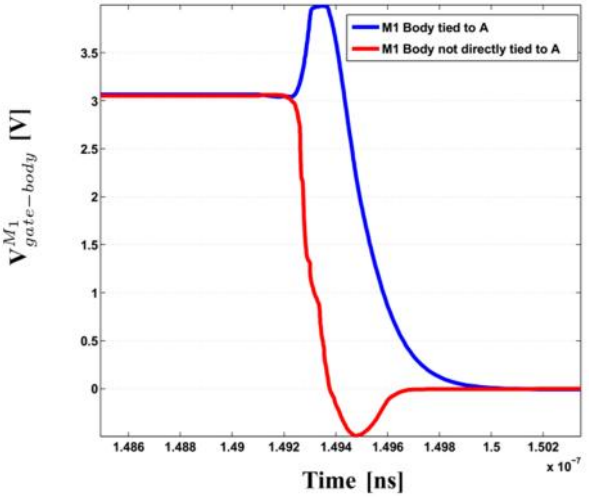


Figure 4: Simulated V_{M1} gate-body voltage with and without M9

B. Dual Path Comparator

To obtain a wider dynamic range, higher noise rejection, improved matching, and/or reduced power dissipation relative to their single-ended continuous-time counterparts, it is interesting to use differential switched-capacitor topologies [9]. A typical switched-capacitor CMOS comparator as commonly used in pipelined analog-to-digital converters consists of a capacitive input sampling/subtraction network, a pre-amplifier, and an output latch. These circuits compare an input voltage to a reference voltage and latch a logic '1' or '0' at the output depending on whether the input voltage is higher or lower than the reference voltage. Switched-Capacitor circuit topologies exhibit much greater single-event vulnerability than their continuous-time counterparts due to the presence of floating nodes in the signal path. Since floating nodes do not have any charge dissipation path, the charge deposited on a floating capacitor by a single-event strike remains until the next clock phase at least. We have implemented the radiation hardened approach proposed in [10] that aims to reduce the bit error rate of a comparator operating in a radiative environment (Fig.5). It relies on a dual

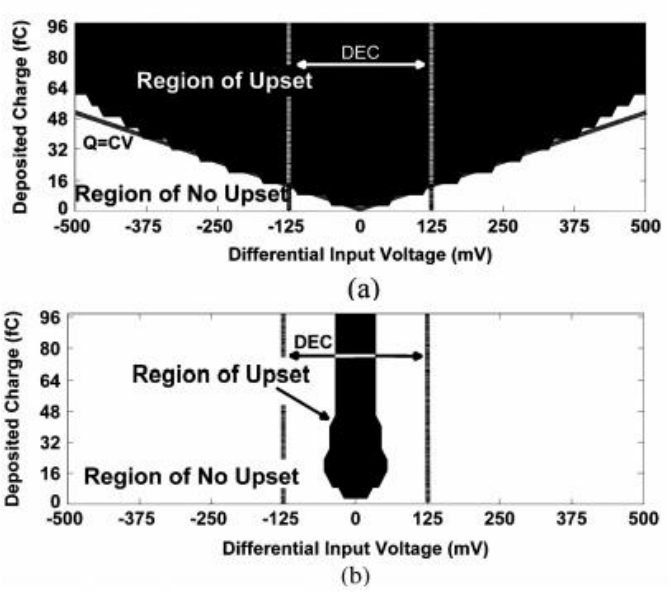


Figure 5: Simulated contour plots of differential pre-amp input voltage vs. deposited charge for (a) standard switched capacitor design and (b) dual path auto zero comparator [3].

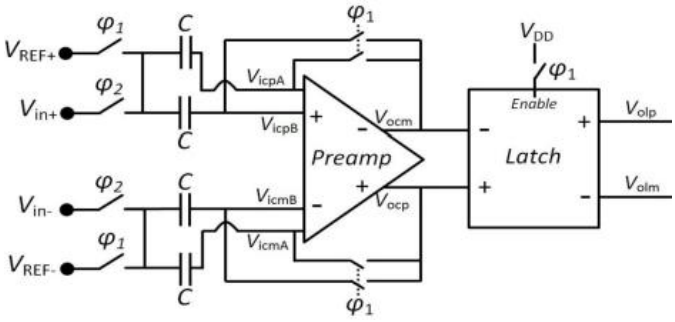


Figure 6: Auto-zero comparator with dual-path hardening around the preamplifier

path design technique to reduce the vulnerability of floating nodes in the switched-capacitor input network of the comparator. Furthermore, it has been shown that an auto-zeroing comparator design can limit the upset duration to a single clock cycle between reset phases [10]. An auto-zero approach has thus been added up to reduce both the upset duration and the comparator offset (Fig.6).

C. Predictive Residue Amplifier

In order to improve further the reliability of the main stage amplifier and reduce its power consumption, a predictive amplifier based on a fully differential class AB one-stage amplifier architecture was chosen and designed instead of a very high gain two/three stages amplifier. Fig. 7 shows the amplifier without the capacitive common mode feedback loop. Fig. 8 depicts the gain enhancement principle applied to the SC amplifier while Fig. 9 shows the required phases. During the first phase, the input voltage is sampled onto all the capacitor C_1-C_4. An estimation is then provided in the second phase. Finally, the last phase provides the residue amplification output.

The residue amplifier error ε can be significantly reduced and expressed as follows:

$$£ = \frac{-1}{A_{0^2}}\left(G_i^2 + \left(\frac{C_{tot}}{C_4}\right)^2 + \frac{C_{tot}}{C_4}G_i\right)$$

where A_0 is the open-loop gain of the amplifier, $C_{tot}= \Sigma C_i$ and $G_i=(C_1+C_2)/C_2=(C_3+C_4)/C_4$ the desired residue amplification value. Table 1 summarized the performance that can be achieved by this gain enhancement architecture for different amplifier open-loop gains and closed-loop gains.

Here, the native gain of the designed amplifier is 46dB and the overall gain enhancement is approximately 20dB, which improves the accuracy of the pipeline stage by 2-bits.

Table 1: Estimated Error with and without gain enhancement

Amplifier Gain	40 dB		60 dB	
	Without	With	Without	With
1.5-bits stage	ε=3%	ε =0.28%	ε =0.3%	ε =0.003%
2.5-bits stage	ε =5%	ε =1.1%	ε =0.5%	ε =0.011%

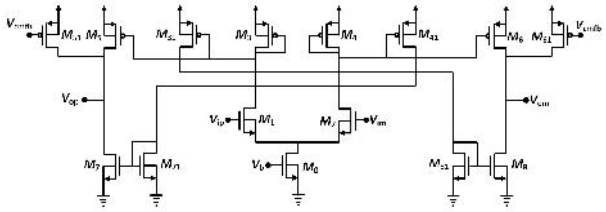


Figure 7: Class AB amplifier

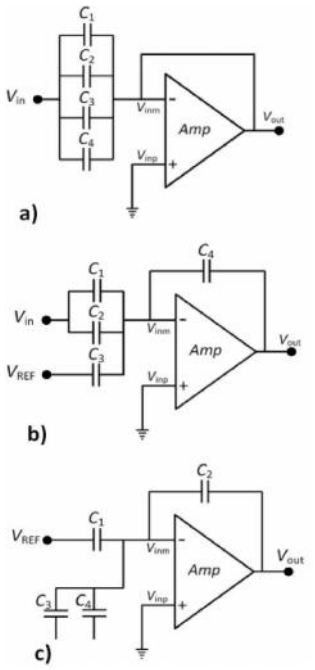


Figure 8: Predictive switched-capacitor residue amplifier: (a) Phase1: sampling, (b) Phase 2: predictive amplification and (c) Phase 3: residue amplification

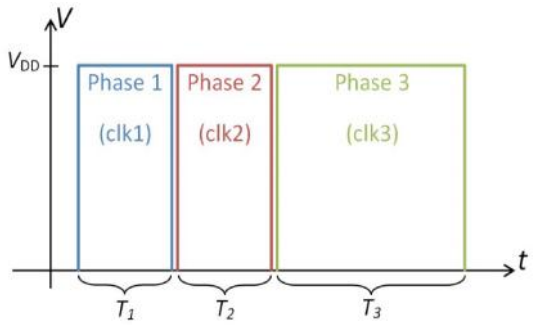


Figure 9: Phases for the gain enhancement: 1 sampling, 2 prediction (or estimated output) and 3 residue amplification.

III. Conclusion and Perspectives

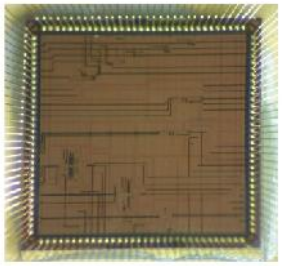


Figure 10:Die photograph of radiation Hardened pipeline ADC blocks in 0.18 µm HV CMOS technology

To validate the performances given by simulation results, a bootstrapped switch and a classical one, an auto-zero comparator with dual-path hardening and a classical one, a predictive rail-to-rail amplifier based on a CDS approach and a single rail to rail amplifier, have been implemented in a 3.3V 0.18µm HV CMOS process (Fig. 10). The test bench to measure the blocks performances is still under development.

Other gain enhancement techniques should be assessed in future implementations such as correlated level shifting and iterative gain enhancement approaches in order to achieve even higher amplifier open-loop gain, lower noise and lower power consumption and lower amplifier architecture complexity.

IV. References

[1] M. Dessouky and A. Kaiser (2001), Very low-voltage digital-audio Delta-Sigma modulator with 88-dB dynamic range using local switch bootstrapping, Solid-State Circuits, IEEE Journal of, vol. 36, n. 3, pp 349-355

[2] M. Silvestri and al, (2009 Aug.), Gate Rupture in Ultra-Thin Gate Oxides Irradiated With Heavy Ions, Nuclear Science, IEEE Transactions on , vol.56, no.4, pp.1964-1970

[3] Brian D. Olson and. al. (2008 Dec.) “Single-Event Effect Mitigation in Switched-Capacitor Comparator Designs,” IEEE Trans. Nucl. Sci., vol. 55, No. 6, pp. 3440–3446, Dec. 2008.

[4] K. Nagaraj and al., (1987 May) "Switched-capacitor circuits with reduced sensitivity to amplifier gain," in *IEEE Transactions on Circuits and Systems*, vol. 34, no. 5, pp. 571-574.

[5] B. R. Gregoire and U. K. Moon (2008 Dec), "An Over-60 dB True Rail-to-Rail Performance Using Correlated Level Shifting and an Opamp With Only 30 dB Loop Gain," in *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 2620-2630

[6] T. A. Monk, P. J. Hurst and S. H. Lewis (2016 April), "Iterative Gain Enhancement in an Algorithmic ADC," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 4, pp. 459-469.

[7] M. Waltari and K. Halonen (2002 Jun), Bootstrapped switch without bulk effect in standard CMOS technology, Electronics Letters , vol.38, no.12, pp.555,557

[8] O. D. Bernal, L. Perbet and H. Tap (2014), "Radiation hardened bootstrapped switch in 0.18µm CMOS process," *Electronics, Circuits and Systems (ICECS), 21st IEEE International Conference on*, Marseille, pp. 610-613.

[9] P. E. Allen and E. Sanchez-Sinencio. (1984) Switched-Capacitor Circuits, New York: Van Nostrand Reinhold.

[10] E. Mikkola, and al. (2004 Dec.) “SET tolerant CMOS comparator,” IEEE Trans. Nucl. Sci., vol. 51, no.6, pp. 3609–3614

RADIATION HARDENED HIGH-VOLTAGE AND MIXED-SIGNAL IP WITH DARE TECHNOLOGY

Bram De Muer[(1)], Jan Dielens[(1)], Eldert Geukens[(1)], Jonathan Van den Berk[(1)], Dries Liebens[(1)], Yves Geerts[(1)], Geert Thys[(2)], Steven Redant[(2)]

[(1)] ICsense NV, Gaston Geenslaan 14, 3001 Leuven, Belgium
Email: demuer@icsense.com
[(2)] Imec, Kapeldreef 75, 3001 Leuven, Belgium
Email: geert.thys@imec.be, steven.redant@imec.be

Abstract

Recent trends show the growing need for more analog, mixed-signal and high-voltage IP to enhance the intelligence and reduce the cost of satellites. This paper presents the set of radiation hard, mixed-signal and high-voltage IP that is part of the imec DARE solution and that is developed in UMC 0.18um, XFAB XH018 and On Semiconductor i3t80 technology. The IP is conceived to enable rad-hard SoC developments and consists of ADCs, PLLs, clocks, linear regulators, bandgap references with current reference and temperature sensors, high-voltage DCDC converters to convert the satellite main supply to analog and digital on-chip voltages and several high-power and high-voltage switches and drivers. The IP is versatile to be useful in a myriad of applications and is part of the DARE platform.

The IP in UMC 0.18um has been successfully silicon proven and radiation tested. First-time-right radiation hardness is achieved through a proprietary under-radiation simulation approach developed by ICsense and elaborated in this paper.

I. INTRODUCTION

Harsh radiation environments constitute an essential challenge for space applications. Pervasive particles from cosmic rays induce cumulative and transient effects that can cause soft errors or even permanent damage in electronics circuits. Mixed-signal integrated circuits implemented in deep submicron commercial technologies have already been qualified as a cost efficient solution for satellites and radiation applications [1]. Besides the low cost, these thin gate oxide technologies are inherently hardened against total ionizing dose (TID) and offer high speed, low power consumption and high yield.

Although commercial libraries and mixed-signal IP are available, they often present high single-event latch-up (SEL) and single-event transients (SET) sensitivity when used in mixed-signal ICs. On the other hand, radiation hardened mixed-signal IP and digital libraries are designed using special design and layout techniques to cope with such issues and still provide high density and low power consumption. These libraries can be used in traditional standard cell design flows.

The existing DARE180 library solution, implemented in UMC 0.18 µm technology, and including mixed-signal IPs such as ADC, PLL, DAC, linear regulators, clocks and current/voltage references with embedded temperature sensor, has already been validated in several space applications [2-4]. The mixed-signal IP in UMC 0.18um has been successfully silicon proven and radiation tested. This solution was designed to be useable in a broad range of systems and therefore offers a very high TID tolerance at the cost of higher power consumption and lower gate density than commercial libraries.

The DARE180X library platform is currently under development with a test chip being taped-out. It includes similar IP blocks, but also DCDC converters to convert the satellite secondary power supply to usable voltages for digital and mixed-signal ASIC use (3.3V and 1.8V). The library platform provides a solution tailored for space applications that require TID tolerance of at least 100 kRad while keeping power consumption and gate density closer to the commercial libraries and enabling high-voltages up to 18V in mixed-signal SoC developments for power management and drivers. Similarly to its UMC-based counterpart, DARE180X includes blocks specially designed to mitigate various single event effects (SEE). More information on the digital DARE180X library and a comparison with the DARE180 library can be found in [5].

Last but not least, the DARE solution has been extended with a ADK for On Semiconductor i3t80, which is a 0.35um BCD process with high-voltage devices up to 80V. It is created to allow radiation hardened, DARE methodology compatible, high-voltage ASIC developments in a standard Cadence design flow as is available for UMC and XFAB technologies. The commercially available PDK has been extended with ELT (Enclosed Layout Transistor) pcells for both nmos and pmos low-voltage devices and for NDMOS high-voltage devices and with octagonal devices for IO cells. The default physical verification decks (Mentor Calibre) have been updated for integration of the ELT pcells, guard rings and n-to-n type leakage. This ADK has been used to develop a high-voltage, radiation-hardened ASIC in i3t80 with maximal voltages up to 40V and currents of several amperes. Care has been taken to minimize SEGR and SEB.

II. RADIATION HARDENED MIXED-SIGNAL IP

All mixed-signal IP blocks - available in both the DARE180 in UMC 0.18um CMOS and the DARE180X in XFAB XH018 - have been developed in the framework of the digital programmable controller (DPC) of Thales Alenia Space [4]. Since the DPC is a highly versatile radiation hardened SOC for a myriad of applications in satellites, it comprises all important mixed-signal blocks needed to build a SoC:

- Reference voltage and current generation
- Built-in temperature sensor
- Power-management block with linear regulators for analog and digital power supply generation
- SET insensitive 120 MHz frequency reference system (PLL) to provide the clock to the digital part
- 100kHz reference oscillator
- 4 flexible 13 bit , 1MSps ADCs with extensive input muxing capabilities
- 3 12 bit, 3.75 MSps DAC current-mode outputs
- Power-on-reset circuit and under voltage detector
- Rail to rail comparators, PGA (0dB, 10dB, 20dB), level shifters, buffers, …

This paper only focuses on the test results of the analog blocks that are readily available in the DARE solution, being the PLL, ADC, bandgap with temperature sensor, DAC and linear regulators. Radiation test data is available and shows all blocks performing as specified under radiation. This excellent result can be attributed to the ICsense proprietary, automated SET hardening simulation environment to assess and decrease the SET sensitivity of the mixed-signal IP [3].

A. Linear regulators

Two linear regulators have been developed, both needing an external compensation capacitor.

For digital supply: Converts the 3.3V main supply to 1.8V with a current capability of 700mA. The area is 4.7mm2 which is needed to avoid temperature degradation. For analog supply: converts the 3.3V main supply to 1.9V with a current capability of 30mA.

Changing the package or the current capability of any of the regulators requires new simulations and possibly a redesign..

B. PLL

For a reliable operation of the digital part, it is essential the clock generation is without glitches (stable clock period and duty-cycle), even during SET events. 'Long-term' frequency spikes and phase shifts due to SET are minimized. The complete PLL, including divider, loop filter and VCO is integrated on-chip. The measured output frequency of the PLL is 120MHz and the bandwidth 7kHz. The input frequency to the PLL is a 100kHz input source selectable between an off-chip reference oscillator or an integrated relaxation oscillator.

The integrated 120MHz Voltage Controlled Oscillator (VCO) has been designed to ensure SET free operation. The VCO is less sensitive to power supply disturbances and provides lower jitter compared to a plain ring oscillator.

The measured specifications are shown in Table 1. All specifications have been validated under radiation and glitch free operation has been proven.

Spec	***Unit***	***Min***	***Typ***	***Max***
Area	mm^2	-	2.3	-
Supply PLL	V	1.8	1.9	1.98
PLL current consumption	mA	-	-	13.8
PLL frequency range when locked	MHz	-0.5%	120	+0.5%
PLL frequency range during SET when locked	MHz	-3%	120	+3%
Cycle to cycle jitter	Fs	-	-	400
Spurious free dynamic range	dB	100	-	-

Table 1: Measured specifications of the integrated PLL

C. ADC

The Analog-to-Digital converter has a cyclic topology with a sample-and-hold structure at the input. The block can operate both differentially and single-ended. It has an integrated reference buffer and requires no external components. The ADC requires a 120MHz clock signal that is internally divided to 30MHz to control the ADC. The block offers full flexibility over the timing of the mux and sample-and-hold. A sampling signal marks the start of the sampling operation of the sample-and-hold, while a start-of-conversion signal marks the end of the sampling operation and triggers the conversion of the sampled signal by the ADC. A block diagram is given in Figure 1. The behavior under SET is as follows:

- The ADC controllers are sensitive to SET, but they cannot enter a locked state.
- The analog part are sized such that an SET strike can only influence 3 ADC samples.
- The multiplexers are hardened for SET strikes to ensure that the analog inputs are never shorted.

The sample-and-hold/mux circuit operates with a 2.5Vptp differential input signal at a common-mode of typically 1.25V. The measured specification can be found in Table 2.

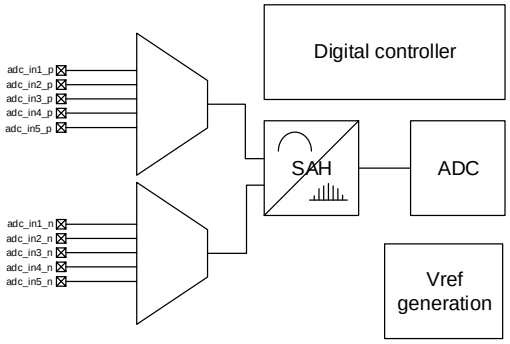


Figure 1: Block diagram of the ADC

Spec	*Unit*	*Min*	*Typ*	*Max*
Area	mm^2	-	0.42	-
Current consumption ADC	mA	-	-	6.0
Resolution	bits	-	13	-
LSB	mV	-	0.33	-
Sample rate	MS/s	-	-	1
INL (diff) / (se)	LSB	-	-	4.0 / 6.2
DNL	LSB	-	-	1.5
SNDR (differential) / (single ended)	dB	-	73 / 67.5	-
RMS noise	LSB	-	0.6	0.75

Table 2: Measured specifications of the ADC

D. DAC

The Digital-to-Analog Converter is a p-type current-steered 12-bit resolution DAC that can operate with/without Dynamic Element Matching (DEM). The DAC-current can be converted to a voltage with a resistor to ground or it can be fed into a buffer. The latter use case has superior linearity. The DAC supports two operation modes.

- Without DEM: Data can change at 3.75MHz data rate. An external filter at 1MHz should be employed.
- With DEM mode: Data can change at divisions of 58.6kHz (3.75MHz/64) data rate. Other data rates will show drop in performance. A first order filtering at 58.6kHz must be employed to suppress switching artefacts of the DEM.

Spec	*Unit*	*Min*	*Typ*	*Max*
Area	mm^2	-	0.39	-
Current consumption	mA	-	4.2	4.5
Resolution	bit	-	12	-
LSB	uA	0.93	0.98	1.03
Full scale	mA	3.8	4	4.2
Output range	V	0	-	2.5
Data rate no DEM/DEM	MS/s	-	3.75 / 0.058	-
DNL no DEM/DEM	LSB	-	-	2 / 0.75
INL no DEM/DEM	LSB	-	1.5 / 1.06	1.7 / 1.26

Table 3: The measured specifications of the DAC

E. Voltage and current reference with built-in temperature sensor

The voltage and current reference block provides an accurate radiation hard reference voltage and currents. It consists of a bandgap, bandgap buffer, current bias block and temperature sensor:

- The bandgap provides a high-impedance, unbuffered bandgap voltage of 1V. It requires an external decoupling cap of 4.7nF. The reference currents can be used to generate accurate voltages in other blocks by using matched unit resistances.
- The bias block uses an external resistor to generate accurate bias currents. It has 47 current outputs of 10uA and an additional source to be used together with the reference oscillator IP block.
- The temperature sensor, including output buffers, provides a PTAT (Proportional To Absolute Temperature) voltage and is compatible with the ADC IP block, so enabling digital temperature read-out.

The behavior under SET is as follows:

- SET cannot trigger an unwanted shutdown/restart sequence of the bandgap.
- SET can only generate minor disturbance on bandgap voltage (few mV) and on the currents.
- Temperature sensor and buffer outputs are not SET hardened.

Spec	*Unit*	*Min*	*Typ*	*Max*
Area	mm^2	-	1.67	-
Current consumption	mA	1.65	2.0	2.55
Nominal reference volt (Vbg)	V	0.987	1.0075	1.028
Integrated noise 1Hz – 1 GHz	μV_{RMS}	15.840	19.250	23.792
min. PSRR 1Hz - 120MHz	dB	34	-	-
Temp drift -20-110°C	ppm	-887	-	984
Error of temperature sensor in -20-110°C	°C	-0.81	-	1.01

Table 4: Measured specifications of the references

III. HIGH-VOLTAGE POWER MANAGEMENT IP IN XFAB XH018

As part of the DARE180X library, high-voltage power management blocks are developed and included in the test chip that is being processed. These blocks have been developed to handle input voltages between 4 and 16.5V. The XFAB XH018 high-voltage devices (45V) have been used in these blocks to have sufficient margin to avoid Single-Event-Gate-Rupture (SEGR). A previous test chip has been tested under radiation to assess the performance and robustness of these high-voltage devices.

The different high-voltage blocks that have been developed are:

- High-voltage regulator: converts the 4-16.5V to 3.3V for low power blocks (max 3.5mA) that have to start up fast;
- Shunt regulator that generates intermediate voltages for the DCDC converters;
- Hysteretic 1.8V DCDC converter that converts a 3V-16.5V input to a 1.8Voutput with a maximum load current of 600 mA and a maximum voltage ripple of 130mVptp; the efficiency is 70-86% for different load conditions;
- Hysteretic 3.3V DCDC converter that converts a 4V-16.5V input to a 3.3V output with a maximum load current of 350mA and a voltage ripple of 130mVptp; the efficiency is 86-94% for different load conditions;
- High-voltage driver that can drive up to 125mA with an output voltage of 16.5V.

Both DCDC converters use an external inductor and several external capacitors for their operation. The DCDC converts consists of a voltage loop with built-in soft start, with hysteresis that is controlled externally, type II compensation and a current loop that measures the coil current trough an external resistor. A SET hardened comparator compares the measured current to the wanted current in the voltage loop. The coil driver drives the coil controlled by the comparator. When the DCDC is disabled, the coil-driver is put into tri-state. The output supply is in this case pulled to ground. The DCDC is able to withstand a short at its output pin.

In Table 5, the total output variation is given for different parameters with and without trimming.

Parameter	**Unit**	**Variation**	
		Min.	**Max.**
SET event	%	-0.17	0.20
Load step drop	%	-7.87	6.35
Total	%	-2.97	2.57
Total, batch trimming	%	-1.65	1.34
Total, sample trimming	%	-1.01	0.7

Table 5: Output variation on the 1.8V DCDC converter

Several measures haven been taken to maximize the radiation hardness of the DCDC converter using the proprietary rad hard simulation methodology of ICsense [3]. As can be seen in Table 5, the effect of an SET is only +-0.2% due to these measures. For the digital controllers, rad hard cells are only used for controlling static signals to reduce spikes on the analog supply. For all critical bias nodes of the critical blocks (integrator gm cell, current sense gm cells), filtering techniques and higher currents have been used in bias branches to have faster settling and smaller voltage peaks. In the current sense block, low pass filters of 160 kHz have been added to the outputs of the comparators to deglitch the output, followed by a deglitched and hardened Schmitt trigger.

The soft start slope node has a high impedance, and is thus susceptible to SET strikes. It has been designed to limit the maximal current delta due to a SET event during startup to ±50 mA by choosing the right capacitor value. The soft start ensures that the current sensing has already started up before any current starts flowing in the coil.

IV. High-Voltage IP Development in i3t80

Using the radiation hardening ADK (Analog Design Kit) for the On Semiconductor i3t80 technology in de DARE solution of imec, a high-voltage, radiation-hardened ASIC in i3t80 has been developed.

The ASIC is a driver ASIC able to drive voltages up to 40V and currents up to several amperes in total. To limit the voltage drop and power dissipation very low-ohmic, high-voltage switches have to be used. To drive these switches a floating voltage domain for each high-voltage input is created, since the gate-source voltage of the high-voltage devices can be maximally 3.6V. Given the size of the DMOS devices care has to be taken of radiation effects, especially SEGR. In addition, the high-voltage power supply is protected with a 4kV HBM ESD clamp. The outputs are self-protecting up to 4kV. All low voltage pads are protected up to 4kV as well.

The ASIC only needs a minimal number of external component. All other blocks are integrated such as bandgap references, amplifiers, POR, regulators, level shifters, reference buffers, test infrastructure ... The layout is shown in Figure 2.

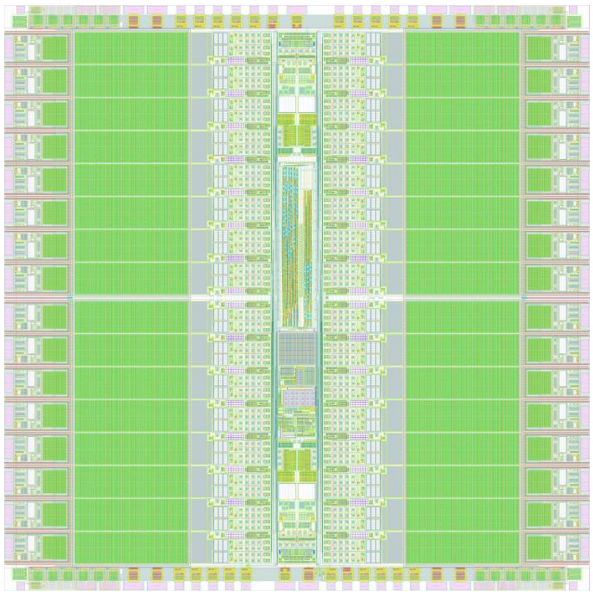


Figure 2: i3t80 ASIC layout

Several measures are taken to attain radiation hardness for a TID up to 100kRad and 60 MeV/mg/cm^3 LET. For TID effect minimization, ELT devices are used for both nmos and pmos devices and NDMOS devices. To prevent SEGR and SEB, DNMOS devices are stacked. Safe operating checks have been implemented to monitor the VDS of all high-voltage devices during simulation. To prevent SET effects, the proprietary SET simulation flow has been used to assess and minimize the impact of an SET pulse. The bandgap, level shifters and POR have been made SET proof through filters and increased currents to avoid state changes due to SET events.

The measurements of the ASIC are ongoing and show excellent results at the moment of writing this paper.

V. Conclusions

Thanks to the successful collaboration with its partners and customers, ICsense has been able to develop a set of radiation hard, mixed-signal and high-voltage IP blocks. The IP is commercially available as part of the imec DARE solution in UMC 0.18um, XFAB XH018 and On Semiconductor i3t80 technology. The IP enables rad-hard SoC developments and consists of ADCs, PLLs, DACs, linear regulators, bandgap references with current reference and temperature sensors, high-voltage DCDC converters to convert the satellite main supply to analog and digital on-chip voltages and several high-power and high-voltage switches and drivers.

The IP blocks in XFAB XH018 are being processed. The IP in UMC 0.18um has been successfully silicon proven and radiation tested. The high-voltage ASIC in i3t80 has been successfully proven in silicon and radiation testing is ongoing. First-time-right radiation hardness is achieved through a proprietary under-radiation simulation approach developed by ICsense.

VI. ACKNOWLEDGEMENTS

The authors would like to thank Thales Alenia Space Belgium (ETCA) for the successful collaboration on the DPC ASIC in UMC 0.18 and their contributions to this work for both the UMC 0.18 and XFAB XH018 IC developments. In addition the authors would like to thank RUAG Space Sweden for their contributions and fruitful cooperation. Last but not least, the authors would like to thank ESA for all the support.

VII. REFERENCES

[1] S. Redant, R. Marec, L. Baguena, E. Liegeon, J. Soucarre, B. Van Thielen, G. Beeckman, P. Ribeiro, A. Fernandez-Leon, B. Glass. (2004, September). The Design Against Radiation Effects (DARE) Library. Presented at 5th RADECS Workshop.

[2] G. Thys, S. Redant, L. Folens, J. Tsouhlarakis. (2010, September). Mixed Signal Tolerant Design with DARE Library: KNUT. Presented at 3rd International Workshop on Analog and Mixed-Signal Integrated Circuits for Space Applications (AMICSA 2010).

[3] G. Thys, S. Redant, E. Geukens, Y. Geerts. (2012, August). Radiation Hardened Mixed-Signal IP with DARE Technology. Presented at 4th International Workshop on Analog and Mixed-Signal Integrated Circuits for Space Applications (AMICSA 2012).

[4] M. Fossion, A. Van Esbeen,T. Van Humbeeck ,Y. Geerts, E. Geukens, S. Redant , R. Jansen , C. Monteleoned. A Mixed-Signal Radhard Microcontroller: the Digital Programmable Controller (DPC). Presented at 5rd International Workshop on Analog and Mixed-Signal Integrated Circuits for Space Applications (AMICSA 2014)

[5] Franciscatto, E. Geukens, G.Thys, S. Redant, Y. Geerts, M. Fossion, A. Van Esbeen. DARE 180X: A 0.18um mixed-signal radiation-hardened library for low-power applications. Presented at 5rd International Workshop on Analog and Mixed-Signal Integrated Circuits for Space Applications (AMICSA 2014)

[6] Bram de Muer ICsense “Rad-hard, high-performance analog and high-voltage IP in 0.18um CMOS (DARE)” ESA IP-cores day Sept 2013

A 2.56 Gbps Radiation Hardened LVDS/SLVS Receiver in 65 nm CMOS

B. Faes[a,c] , J.Christiansen[b], P.Moreira[b] , P.Reynaert[c] and P. Leroux[a,c]
[a] KU Leuven, Dept. of Electrical Engineering, ESAT-ADVISE, Kleinhoefstraat 4, 2240 Geel Belgium
[b] CERN, CH-1211 Geneva 23 Switzerland
[c] KU Leuven, Dept. of Electrical Engineering, ESAT-MICAS, Kasteelpark Arenberg 10, B-3001 Leuven Belgium
bram.faes@esat.kuleuven.be

Abstract

A novel radiation hardened by design LVDS/SLVS receiver is designed and simulated in 65 nm CMOS technology. The receiver is capable of receiving a 2.56 Gbps signal with less than 400 fs RMS jitter and 500 μW power consumption drawn from a 1.2 V power supply. A replica receiver with a compensation loop is used to measure and compensate for the total ionizing dose (TID) radiation effects. This loop will ensure an equal propagation delay of the rising and falling output edges, to allow the use in accurate time-domain signalling circuits.

.

I. Introduction

Many of today's applications require high precision time-domain signal processing circuits like particle detectors in high-energy physics experiments such as the CMS and ATLAS experiments at the Large Hadron Collider (LHC) in CERN [1] or laser-ranging sensors [2]. The key information of these applications is contained in the timing difference between multiple signals or events. This timing information is usually converted to binary data using time to digital converters (TDC) [3]. In large and/or complex systems however, the distance between the detector/event generator and the TDC can become rather large, calling for a highly time accurate, long distance, transfer of these signals.

Low Voltage Differential Signaling (LVDS) and Scalable Low Voltage Signaling (SLVS) are, because of their robustness to interferences, low power consumption and high speed [4][5], commonly used techniques for data transmission in today's applications. The SLVS standard is comparable to the LVDS standard, with the difference of a 200 mV common mode voltage instead of 1.2 V and a smaller voltage swing. For data transmission applications, the regenerative nature of the receiver allows some tolerance to jitter provided the bit error rate remains sufficiently low. However, in the envisaged sub-nanosecond timing applications, jitter is the major impairment to the performance of the system. When an LVDS/SLVS receiver is used in the signal path between the event generator circuit and the TDC, any time distortion introduced by the latter, will cause a time measurement error and consequently will lower the system resolution. To allow an accurate time measurement between several events, the propagation delay of all the edges, at the output of the LVDS/SLVS receiver, must be the same.

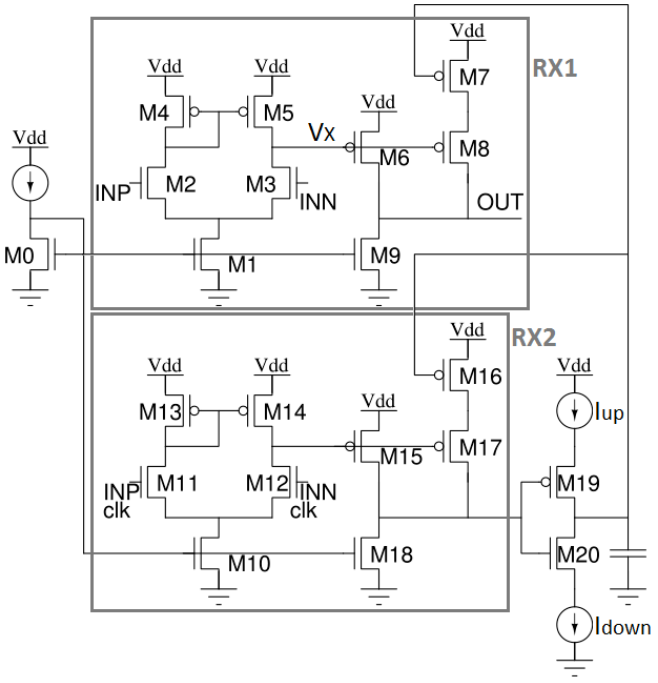


Figure 1: Schematic of the LVDS/SLVS receiver with feedback loop

This paper focuses on the design of a total ionizing dose (TID) radiation hardened by design LVDS/SLVS receiver which can be used in these long distance, high time resolution measurement applications. Radiation effects and/or process corners, will alter the propagation delay of the rising and falling edges at the output. In this design the time difference between these two propagation delays will be measured and compensated by a replica receiver with a charge pump based feedback loop [6].

This paper is organized as follows. Section II shows and discusses the schematic of the LVDS/SLVS receiver. The simulation results of the receiver and feedback loop are shown and discussed in section III.

II. Schematic

The schematic of the receiver is shown in Figure 1. Here RX1 (with input pair M2-M3) receives the accurate timing signal. From a design perspective it is possible to balance the propagation delays of the rising and falling output edges by choosing the ratio between M6 and M9 (ignoring for the time

being M7 and M8). However this cannot be done across all process corners and temperature variations.

Moreover, in radiation environments, the total ionizing dose radiation effects will cause shifts in the threshold voltage and degradation of the charge carrier mobility [7]. These effects will change the gain/propagation delay of the receiver's first stage and consequently will lower the current through M6 and so increases the propagation delay of the rising edge. In this case, transistor M9 can be set far into saturation region, so the threshold voltage shift does not, or minimally, effects the output current. Design for immunity to TID will also increase the circuit's robustness in term of PVT (Process-Voltage-Temperature).

To compensate the receiver's variations in speed and propagation delay, transistor M7 and M8 are added. The current through M7 can now be adjusted to compensate the increase or decrease in the current through M6 due to TID radiation effects and/or process variations. In this design, M8 is used as switch to turn off M7 together with M6 when the output voltage is low.

The mismatch between the propagation delays of the rising and falling output edges will be measured by a replica receiver (RX2 in Figure 1, input pair M11-M12) associated with a charge-pump (M19 and M20 and current sources I_{UP} and I_{DOWN}). When the propagation delays of the rising and falling edges are equal, an ideal clock at the input of this replica receiver will generate a clock signal at the output with a duty cycle of 50 %. In this case, when both charge pump currents are equal, the output voltage will settle to $V_{DD}/2$.

Any deviation from this 50 % duty cycle, caused by the TID effects, process corners or temperature, will cause the charge pump output voltage to shift. This voltage shift is used to compensate the current through M7 and M16 in order to equalize the propagation delays of the output rising and falling edges.

In this design, the clock input for the replica receiver will be generated by a second source. In practice, this can be done by a CDR (Clock Data Recovery) circuit. To save power, the feedback loop can also be implemented on the actual receiver (here RX1). But this requires a Manchester coding (which will halve the bit rate for the same bandwidth), or a scrambled signal with enough bit-flips, depending on bandwidth of the feedback loop and the frequency of the input signal, to ensure a stable voltage at the output of the charge pump.

III. Simulation Results

The proposed receiver is designed and simulated using a commercial 65 nm CMOS technology. This technology has a power supply of 1.2 V which is identical to the common mode voltage of an LVDS signal. In this design, for an optimal use of the receiver, the common mode voltage of the input signals must be between ± 0.5 V - 1 V. This is fine for ad-hoc systems, like the CMS and ALTAS detectors at CERN, which don't need to communicate with off-the-shelve LVDS modules, and so can freely choose the common mode level. Nevertheless, the proposed technique is easily scalable to I/O devices or other technologies with a larger power supply for full LVDS compatibility. Additionally, a PMOS input pair receiver is designed which is able to receive low common mode voltage and SLVS signals. All simulations shown in this section were done using the cadence spectre simulator.

All following simulation results will be executed using a 2.56 Gbps input signal with 200 mV single ended swing and 800 mV common mode voltage. The top receiver (RX1 in Figure 1) has a 2^7-1 sequence pseudo random bit stream input, while a separately generated clock is added at the input of the replica receiver (RX2 in Figure 1). The 800 mV common model level will give the worst case output signal. When the common mode level decreases, current source M1 will go into the linear region, consequently decreasing the current through the receiver and its performance. An increase in common mode voltage will make M1 more able to provide current through the receiver, thus increasing the speed and performance of the receiver.

A. Normal operation

Figure 2 shows the simulated eye diagram of the receiver's input (grey line) and output (black line) signal (output signal of RX1 in Figure 1). In an eye diagram, when the propagation delays of the rising and falling edges are equal, the crossing voltage of both edges should be at V_{DD}, in this case 0.6 V. In this paper, this crossing voltage is given to indicate the error in the propagation delay. Knowing the rise and fall times, and assuming that $t_{RISE} = t_{FALL}$, the error can then be calculated using:

$$Propagation\ delay\ error = \pm \frac{t_{rise}}{V_{DD}} \left(V_x - \frac{V_{DD}}{2} \right) \quad (1)$$

where V_x equals the crossing voltage.

In the eye diagram of Figure 2, the crossing is 580 mV, so indicating a small error between both propagation delays. This error is due to mismatch in the charge pump currents. The loop will, in this case, generate a 580 mV output voltage instead of 600 mV. The output signal has a rise and fall time of 100 ps and so a -1.5 ps propagation delay error between both edges. The output signal shown in this figure has a 400 fs RMS output jitter and consumes 500 μW drawn from a 1.2 V power supply.

The output signal of the charge pump during start up is shown in Figure 3. The feedback loop has a start up time of approximate 60 ns. This start up time can, depending on the application, be changed by changing the charge pump's current and/or capacitor. In regime, the output signal of the charge pump has a 10 mV variation.

B. Corners/Temperature/Voltage

This subsection give an overview of the variations of the crossing voltage and propagation delay error in terms of PVT.

These simulations were executed using the same input variables as in section III-A.

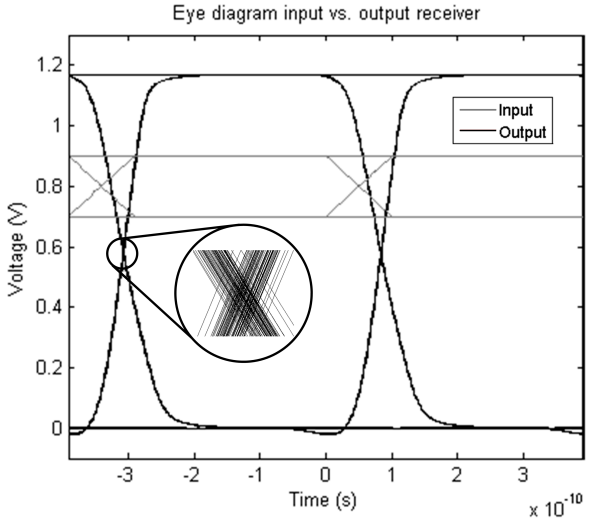


Figure 2: Eye diagram output LVDS/SLVS receiver with 200 mV amplitude, 800 mV common mode level and 2.56 Gbps, 2^7-1 sequence pseudo random bit stream input

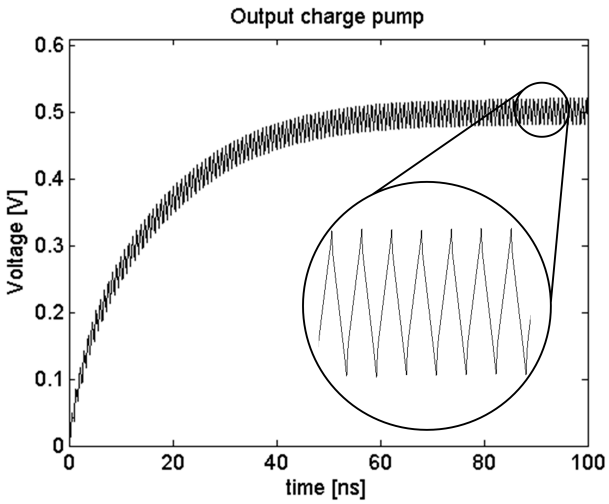


Figure 3: Output charge pump with 200 mV amplitude, 800 mV common mode level and Gbps, 2^7-1 sequence pseudo random bit stream input

The variations due to process corners are shown in Table 1. In all corners, the crossing voltage varies from 500 mV (SS corner) until 640 mV (SF corner) which is a total variation of 140 mV. The output signal has a rise and fall time of a 100 ps and so the crossing point variations will, using Eq. (1), introduce a total propagation delay variation of 10 ps, from 3 ps (SF corner) and -7 ps (SS corner).

Table 2 shows the variations of the crossing voltage and propagation delay due to changes in the operating temperature. Here, the crossing voltage varies from 550 mV (-25°C) until 640 mV (125°C) which is a total variation of 90 mV. The rise and fall times remain 100 ps, and so the crossing voltage variation can be related to a total propagation delay of 6.6 ps, going from -3.6 ps (-25°C) up to 3 ps (125°C).

Finally, the effects of 20 % power supply variations are shown in Table 3. Here, the crossing voltage varies from 460 mV (1.08 V) until 730 mV (1.32 V) which is a total variation of 270 mV. These variations relate, with a 100 ps rise and fall time and respecting the change in supply voltage in Eq. (1), to a total propagation delay error variation of 17.7 ps, from -10.3 ps (1.08 V) up to 7.4 ps (1.32 V).

Table 1: Variations crossing voltage and propagation delay error vs. corners

	TT	FF	FS	SF	SS
Crossing voltage [mV]	580	630	520	640	500
Propagation delay error [ps]	-1.5	2.2	-5.9	3	-7

Table 2: Variations crossing voltage and propagation delay error vs. temperature variations

	-25°C	25°C	85°C	125°C
Crossing voltage [mV]	550	580	620	640
Propagation delay error [ps]	-3.6	-1.5	1.5	3

Table 3: Variations crossing voltage and propagation delay error vs. power supply variations

	1.08 V	1.2 V	1.32 V
Crossing voltage [mV]	460	580	730
Propagation delay error [ps]	-10.3	-2.33	7.42

C. Influence of radiation

The TID radiation effects on the proposed circuit are simulated using transistor models with parameters after 500 Mrad radiation. Again, these simulations were executed using the same input variables as in section III-A.

The results of the radiation simulations (grey line) are shown together with the original output signal (black line) in Figure 4a. The simulated output signal after irradiation clearly has a larger propagation delay and a data dependency of the rising edge. These effects can be related to the internal node V_X (Figure 1). Due to the decrease of the transistor's gm, caused by the TID radiation effects, the charge and discharge speed of node V_X decreases, consequently increasing the slew rate of this node and the output propagation delay. Secondly, due to this drop, the internal node V_X can't be fully charged at the 2.56 Gbps speed. Now depending on the previous bit, node VX can be fully or partially charged, which will cause a variation in the propagation delay, resulting in the observed data dependent jitter.

The eye diagram (Fig. 4a) shows an output rise and fall time of 140 ps and a data dependent variation of the crossing voltage of 150 mV, which relates to a 16 ps data dependent jitter. The output signal has an average crossing voltage of 590 mV which gives a -1.2 ps propagation delay variation. This is only a 10 mV increase in crossing voltage and a 0.3 ps variation on the propagation delay error compared to the closed loop simulations without irradiation (section III-A). Figure 4b shows the output signal of the receiver when no feedback loop is implemented. The propagation delay error at

normal operation is equal to the one of the closed loop system. Like in the closed loop output signal, the open loop output signal has a rise and fall time of 140 ps. The crossing

Table 4: Summary table of required styles.

	Data rate [Gbps]	RMS jitter [ps]	Power [mW]	FOM [mW/Gbps]	FOM [ps/mW]	Measurements	Technology
This work	2.56	0.4	0.5	0.19	0.8	No	65 nm
[4]	11.2	58.8	1.602	0.14	36.7	Yes	0.18 μm
[8]	1.5	/	7	4.66	/	No	150 nm
[9]	3	/	2	0.67	/	No	0.18 μm
[10]	6.4	/	4.2	0.65	/	Yes	80 nm DRAM

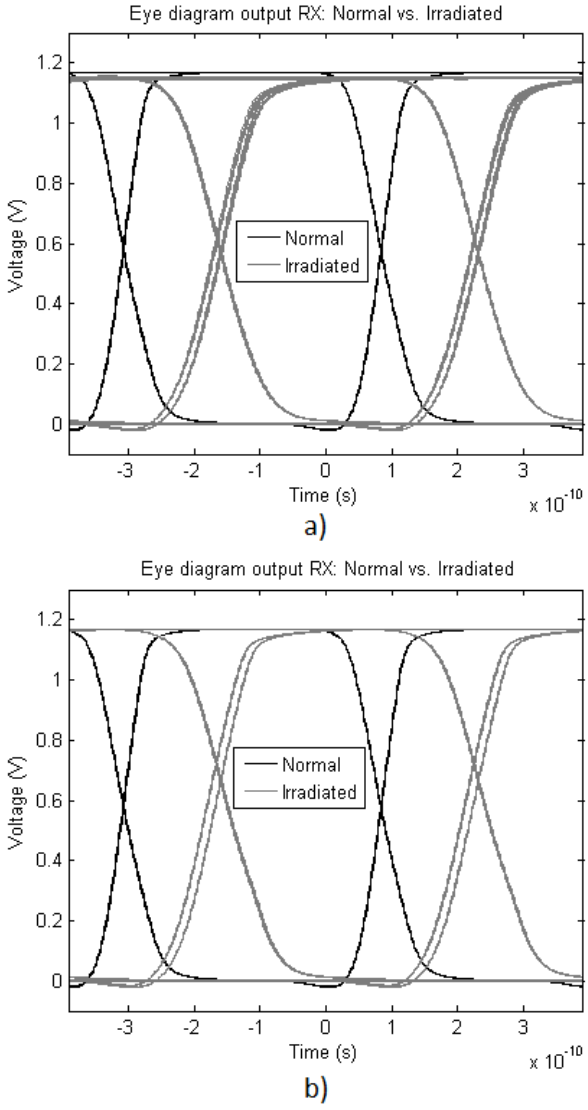


Figure 4: Eye diagram output LVDS/SLVS receiver with 200 mV amplitude, 800 mV common mode level and 2.56 Gbps, 2^7-1 sequence pseudo random bit stream input: a: Normal vs. irradiated output signal with compensation. b: Normal vs. irradiated output signal without

voltage has a data dependent variation of 300 mV, resulting in a 35 ps data dependent output jitter. The average crossing voltage equals 700 mV, which gives a 11.6 ps propagation delay error. This is a 120 mV crossing voltage increase and a 13.1 ps propagation delay variation compared to the open loop simulations without irradiation.

The simulations with irradiated transistor models and without compensation loop indicate a 19 ps decrease in data dependent output jitter and a 11 ps decrease in propagation delay error when the feedback loop is added.

D. Comparison SOTA

Table 4: gives a comparison of the proposed receiver with the current state of the art (SOTA). The data rate, jitter and power consumption are summarized in two figures of merit (FOM). The first FOM gives the power consumption of the receiver, relative to the data rate. The receiver designed in this paper has a FOM of 0.19 mW/Gbps which is slightly more than the 0.14 mW/Gbps of [4] but significantly less compared to the 4.66 mW/Gbps [10] and 0.65 mW/Gbps [9] of the other receivers. The second FOM gives the RMS jitter as a function of the power consumption. For the proposed receiver this is only 0.8 ps/mW, which is substantially lower than the measured 36.7 ps/mW achieved in [4].

IV. CONCLUSION

This paper proposes a novel 2.56 Gbps, radiation hardened by design, LVDS/SLVS receiver. Primary simulation results show a 500 μW power consumption and a 400 fs RMS output jitter. The propagation delay differences, due to radiation effects or PVT of the rising and falling edges at the output is compensated using a replica receiver with compensation loop. In normal operation, the receiver has a -1.5 ps propagation delay error. The process corners, temperature and power supply variations give a total propagation delay error variation of respectively 10 ps, 6.6 ps and 17.7 ps. The radiation effects were simulated using 500 Mrad TID irradiated transistor models. These simulations show a 13.1 ps propagation delay error at the output of the open loop receiver. The receiver with the proposed feedback loop shows only a 0.3 ps propagation delay error, which is an improvement of more than 43 times compared to the open loop system.

The main origin of variations in the propagation delay due to PVT originates in the mismatch between the charge pump currents. Consequently, the robustness to PVT can easily be increased by improving the robustness of the charge pump.

V. ACKNOWLEDGEMENTS

The radiation models have been made available by CPPM (Centre de Physique des Particules de Marseille) through the CERN RD53 collaboration.

VI. REFERENCES

[1] Ljuslin, C., Christiansen, J., Marchioro, A. and Klingsheim, O., ”An integrated 16-channel CMOS time to digital converter”, IEEE Trans. On Nuclear Science, vol.41, no.4, pp. 1104-1108, Aug. 1994.

[2] Gao P. and You Z., "Characters of Laser Ranging on Inter-satellite Position Measurement", Proc. International Conference on Recent Advances in Space Technologies RAST, pp. 614-617, Istanbul Turkey, 14-16 June 2007.

[3] Prinzie, J., Steyaert, M. and Leroux, P., "A self-calibrated bang-bang phase detector for low offset, time-signal processing", IEEE Trans. on Circuits and Systems II: Express Briefs, vol.PP, no.99, pp.1-1, Nov. 2015.

[4] Kyeong-Min K., Sewook H., Junyoung S. and Chulwoo K., "An 11.2-Gb/s LVDS Receiver With a Wide Input Range Comparator", IEEE Trans. on Very Large Scale Integration (VLSI) Systems, vol. 22, no 10, pp. 2156-2163, Dec. 2013.

[5] Burkhay, V., Rocke, A., Magistrati, G., Polo, C.B., Furano, G. and Guettache, F., "Radiation tested extended Common Mode LVDS Components", Proc. International SpaceWire Conference, pp. 1-4, Athens, Greece, 22-26 Sept. 2014.

[6] Leroux P., Lens S., Voorspoels R., Van Uffelen M., De Cock W., Steyaert M. and Berghmans H., "Design and Assessment of a Circuit and Layout Level Radiation Hardened CMOS VCSEL Driver", IEEE Trans. on Nuclear Science, vol. 54, no. 4, pp. 1055-1060, Aug. 2007.

[7] M. Menouni, M. Barbero, F. Bompard, S. Bonacini, D. Fougeron, R. Gaglione, A. Rozanov, P. Valerio, A. Wang ”1-Grad total dose evaluation of 65 nm CMOS technology for the HL-LHC upgrades”, Trans. on Journal of Instrumentation, vol. 10, no. 5 , May 2015.

[8] Alqarni, S. and Kamal, A., "LVDS receiver with 7mW consumption at 1.5 Gbps", Proc. International Conference on Microelectronics (ICM), pp.204-207, Doha, Qatar, 14-17 Dec. 2014

[9] Hui H., Jia L., Lingling S. and Keming C., "Design of 2Gb/s LVDS Transmitter and 3Gb/s LVDS Receiver for Optical Communication in 0.18nm CMOS Technology", Proc. China-Japan Joint Microwave Conference (CJMW), pp. 1-3, Hangzhou, China, 20-22 April 2011.

[10] Sua K., Bae-Sun K., Chil-gi L., Jin-Hyun K., Young-Hyun J. and Changhyun K., "A 6-Gbps/pin 4.2mW/pin Half-Deuplex Pseudo-LVDS Transceiver", Proc. European Solid-State Circuits Conference (ESSCIRC), pp.484-487, Montreux, suisse, 19-21 Sept. 2006.

AMICSA: Analogue intellectual property and re-usability of analogue circuits in space

AMICSA: Custom cell-, circuit-, and system design of ICs for space applications

SIPHRA 16-Channel Silicon Photomultiplier Readout ASIC

Dirk Meier, Jörg Ackermann, Alf Olsen, Hans Kristian Otnes Berge, Amir Hasanbegovic, Mehmet Akif Altan, Suleyman Azman, Bahram Najafiuchevler, Jahanzad Talebi, Philip Påhlsson, David Steenari, Arne Fredriksen, Petter Øya, Tor Magnus Johansen, Codin Gheorghe, Timo A. Stein, Gunnar Maehlum

All authors are with Integrated Detector Electronics AS (IDEAS), Gjerdrums vei 19, 0484 Oslo, Norway

dirk.meier@ideas.no

Abstract

SIPHRA is an integrated circuit (IC) for the readout of photon detectors, such as photomultiplier tubes (PMTs), silicon photomultipliers (SiPMs), and multi-pixel photon counters (MPPCs). The IC has 16 input channels and one summing channel. Each channel can be used for pulse height spectroscopy and timing. The summing channel is important for the readout of detector arrays with monolithic scintillators. The programmable shaping time of 200 ns, 400 ns, 800 ns, or 1600 ns allows for pulse-height spectroscopy using scintillators with different light emission properties. The current mode input stage (CMIS) is designed for large negative charge (-16 nC, -8 nC, -4 nC, and -0.4 nC), depending on the programmable attenuation, and it accommodates large capacitive load (several nF) and large leakage current (up to -100 µA from dark counts). Alternatively, the CMIS can be by-passed to allow for positive charge depending on programmable gain (+40 pC, +4 pC, +0.4 pC). The IC contains one 12-bit analog-to-digital converter (ADC) that allows for digitization of the pulse-heights from all channels, including the summing channel at a sampling rate of 50 ksps. Every channel output is available for external use and provides either the analog or a digital trigger/timing pulse with fixed width or time-over-threshold. The programmable channel output facilitates many applications, such as external waveform sampling and digitization, pulse height and time spectroscopy, pulse counting, and triggering. The IC operates at 3.3-V supply voltage and dissipates about 15 mW without CMIS and 30 mW with CMIS active. To save power, any channel or function can be powered down. The ASIC has a serial peripheral interface (SPI) for programming its register settings and for slow ADC data readout; faster readout with up to 1 Mbit/s is possible via a serial data transmission line.

I. Introduction

A. ASIC Requirements and Applications

The requirements for the application specific integrated circuit (ASIC) requirements were derived from needs in Gamma-Ray Imaging, Polarimetry and Spectroscopy (GRIPS, [1]), scintillating fibers for a gamma-ray telescope (PANGU, [2]) and astro-particle missions (HERD, [3]). The circuit covers a wide range of detector technologies and applications in space and terrestrial, for example, high-resolution gamma-ray spectroscopy, detector front-end readout for diagnostic imaging in nuclear medicine, fast photon counting, and timing. The ASIC can be used with SiPMs and MPPCs, for example ref. [4]. Operation in space requires radiation tolerance and low power dissipation. Therefore, special design effort has been on latch-up immunity, single event upset mitigation and error corrections, as well as low-power design and programmable power-down.

B. Design Heritage

The SIPHRA is a design without predecessor. The circuit inherits a few functions and circuit elements from other IDEAS ASICs: buffers from IDE3466 [5], analog-to-digital converter (ADC) from NIRCA [6], and implementation with the radiation tolerant IDEAS ASIC physical and digital design kit. The ASIC was designed with the goal to provide a reliable solution for pulse height spectroscopy with arrays of silicon photomultipliers (SiPMs, e.g., [4]) and multi-pixel photon counters (MPPCs) and multi-anode photomultiplier tubes (MA-PMTs), and to support individual channel analog and digital output for analog waveform sampling, timing, triggering and counting.

C. Readout of SiPMs, MPPCs and PMTs.

Figure 1 shows the block diagram of SIPHRA connected to an array of 16 SiPMs. SIPHRA has 16 channels and one summing channel. Each channel processes the analog signal from the PMT/SiPM/MPPC and allows one to measure the charge (pulse heights), trigger time, and time-over-threshold.

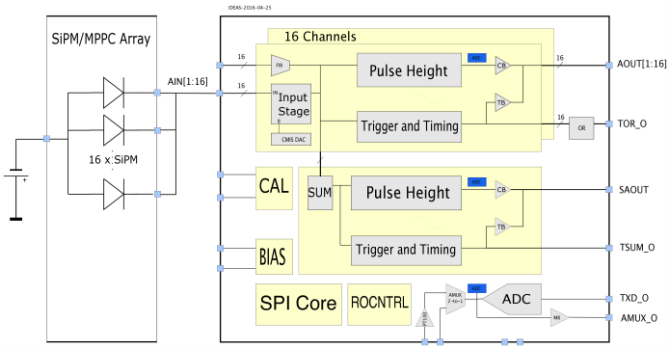


Figure 1: SiPM/MPPC array connected to SIPHRA IC.

II. ASIC Design Specifications

A. Overview

Table 1 summarizes the main features of the SIPHRA circuit, and Figure 3 gives the functional overview of the ASIC. SIPHRA has 16 input channels, one summing channel and one ADC. Every channel provides the functionality for analog pulse height spectroscopy and digital trigger timing pulse derived from pulse height discrimination. The trigger pulse initiates the digitization with the ADC and activates `TOR_O` and `TSUM_O`, to trigger the serial readout of digitized or analog pulse height (via `TXD_O`, and `AMUX_O`, respectively). The trigger pulse is programmable for fixed width or time-over-threshold. The outputs `AOUT[1:16]` can be programmed to provide the analog pulse height, the trigger timing pulses, or the time-over-threshold.

Table 1: SIPHRA features.

– 16 readout channels
16 current sensitive inputs (≤ 16 nC)
1 summing channel
– Programmable attenuation to handle charge up to
-16 nC, -8 nC, -4 nC, -400 pC at AIN inputs, or
+40 pC, +4 pC, +0.4 pC at FIN inputs
– Programmable shaping time
200 ns, 400 ns, 800 ns, 1600 ns
– 16 inputs (AIN) with programmable offset voltage
– Pulse height spectroscopy
16 shapers followed by track-and-hold
Programmable hold timing
12-bit analog and digital readout
3 ksps/channel max.
– Trigger generation
Internal from charge discriminator via
programmable threshold in every channel
External (trigger on input, trigger on sum)
– Power
15 mW without CMIS, 30 mW with CMIS active
Flexible power down scheme of channels or functions
– SEL/SEU radiation hardened
– SPI Interface

B. Analog Channel and Trigger Circuit

1) Current-Mode Input Stage (CMIS)

Each channel has a current mode input stage (CMIS) with inputs `AIN1` to `AIN16`. The CMIS can be connected to the detector either directly (DC coupled, Figure 2) or coupled via a capacitor (AC coupled, not shown), although the CMIS is ideally suited for DC coupling to the detector. The CMIS has two main purposes: to downscale the detector current and to provide a stable input voltage at `AIN`. The input offset is programmable and sets the SiPM bias voltage. This allows one to control the charge released from SiPM and to compensate for the variation in breakdown voltage among several SiPMs.

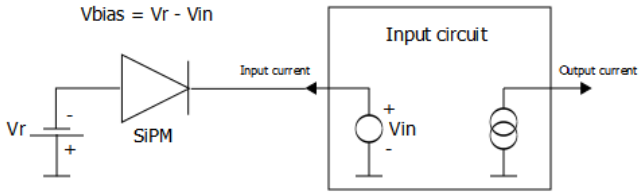


Figure 2: SiPM biasing principle.

Downscaling of the input current is required because the output current from PMTs, SiPMs and MPPCs is too large for on-chip current integration in a charge sensitive amplifier. The integrating capacitor would occupy an impractically large area on the chip. The CMIS is designed for large negative charge with programmable gain attenuation of 1/10, 1/100, 1/200, and 1/400, which causes charge saturation at -16 nC, -8 nC, -4 nC, and -0.4 nC, respectively. The inputs accommodate large capacitive load up to several nF, and large leakage current up to -100 µA from SiPM/MPPC dark counts. The input voltage is regulated to a stable bias voltage set via an 8-bit DAC over the range of 1 V. The CMIS also has a configurable bias current, 12 µA to 48 µA, which should be used if the SiPM has a very small dark current. The CMIS input impedance below 10 MHz is purely resistive between 5 Ohm and 30 Ohm depending on the bias current. Above 10 MHz, input impedance becomes reactive and peaks with a few 100 Ohm at 250 MHz. CMIS can be powered off and by-passed with the detectors connected to the inputs `FIN1` to `FIN16`. The `FIN` inputs allow for positive charge depending on programmable gain (+40 pC, +4 pC, +0.4 pC) in the current integrator.

2) Current Integrator (CI)

Each channel has one active current integrator (CI) with adjustable gain and an adjustable feedback device. The integrator input is fed from the output of the CMIS. If CMIS is powered down the input is taken directly from the `FIN` input pad. Figure 4 shows the block diagram of the CI. The CI integrates a current (positive charge) input, in first order to a voltage step of magnitude Q/C_{fb}, where C_{fb} is the feedback capacitor. The voltage step decays with a typically large time constant τ set to first order by $\tau = R_{fb} \times C_{fb}$, where R_{fb} is the feedback resistor. The CI has a programmable gain of 1V/30pC, 1V/27.75pC, 1V/3pC and 1V/0.75pC.

3) Shaper (SHA)

A pulse shaper (SHA) follows every current integrator. The shaper optimizes the signal to noise ratio (SNR). The shaper is programmable and can be by-passed. Each shaper has two analog inputs (one signal and one reference input) and one analog output. Figure 5 shows a block diagram of the shaper. The shaper has four different shaping times (nominally 200 ns, 400 ns, 800 ns and 1600 ns) that are programmable through a configuration register.

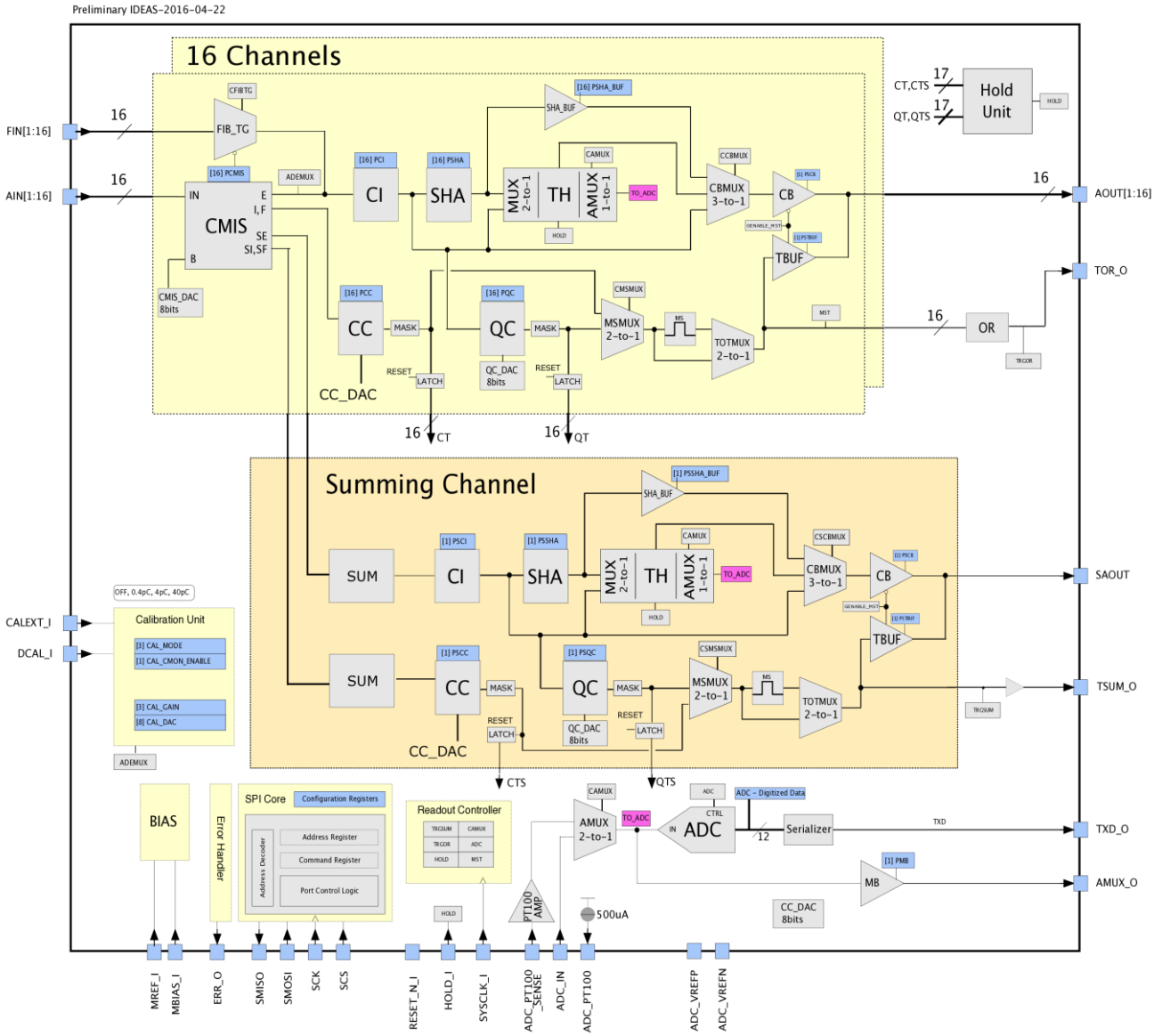


Figure 3: ASIC architectture overview.

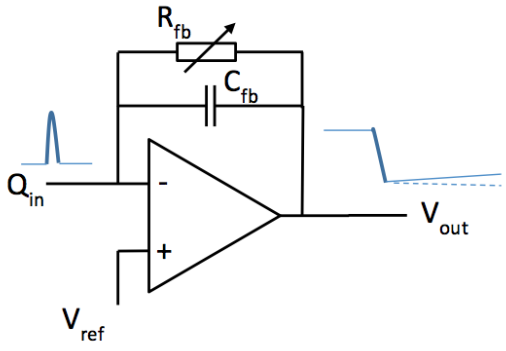


Figure 4: Current integrator block diagram.

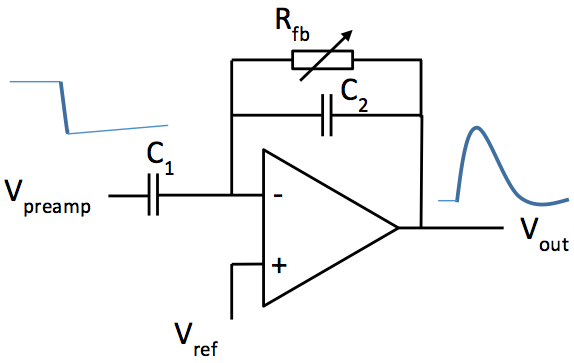


Figure 5: Shaper block diagram.

4) *Pulse Height Spectrometer*

The pulse height spectrometer consists of the current integrator (CI), the shaper (SHA), a track-and-hold unit (TH) and a channel output buffer (CB) capable of driving 10-pF external load. The TH circuit tracks the shaper output voltage waveform, and stops tracking and holds the signal when `HOLD` is asserted. The `HOLD` can be triggered from internal QC or CC or externally at `HOLD_I`. The held value remains constant with minimal distortion from voltage dependent charge injection and droop. The hold delay is programmable with respect to the trigger in the range typically from 69 ns to 4.7 µs. One can program the ASIC registers to provide the signals from the current integrators, or the shapers or the track-and-hold units at `AOUT[1:16]`. The output of the TH unit can be multiplexed (AMUX) to a 12-bit successive-approximation register (SAR) ADC. The ADC digitizes the signals from any or all 16 channels, as well as the summing channel and two externally applied input voltages (`ADC_PT100_SENSE` and `ADC_IN`), at a rate of 50 ksps. The digitized data is serialized and sent out at `TXD_O`. The multiplexed pulse heights are also available at `AMUX_O` for optional readout and digitization with an external ADC. This single-ended analog output is compatible with an external capacitive load of 40 pF.

5) *Trigger Timing and Trigger Readout and Time-over-Threshold*

The trigger timing pulse is generated in a charge comparator (QC) and in a faster current comparator (CC). The purpose of the comparator is: 1) to generate the internal `HOLD` signal for the track-and-hold and initiate the digitization in the ADC, 2) to generate a timing trigger pulse for the logic OR to indicate an event to the system, and 3) to provide a time-over-threshold (TOC) at `AOUT[1:16]` where TOC is related to the input charge. The QC compares the pulse height with an 8-bit programmable reference (charge threshold, individual for every channel) and triggers when the pulse height exceeds the charge threshold. The QC also incorporates programmable hysteresis to avoid retriggering from noise. The CC compares the current from the CMIS with a reference current which is generated by an 8-bit programmable current reference (global for all 16+1 channels). The purpose of the CC is to reduce time walk by providing an early trigger when a charge event occurs on the input of the channel. The programmable ASIC register allows one to enable or disable the triggering from individual channels. The mono-stable outputs of all 16 channels are connected to a trigger OR which outputs a logical OR from triggers in any of the channels (`TOR_O`).

6) *Summing Channel*

The summing channel consists of a differential summing integrator that integrates the sum of the currents of the CMIS outputs from all 16 channels and provides the same pulse height spectrometer and trigger/timing unit like any of the other channels. The summing channel allows one to trigger the readout based on the summed signals from all channels.

C. *Floor Plan, Pads and Signals*

Figure 6 shows the ASIC floor plan, with pad frame and signals.

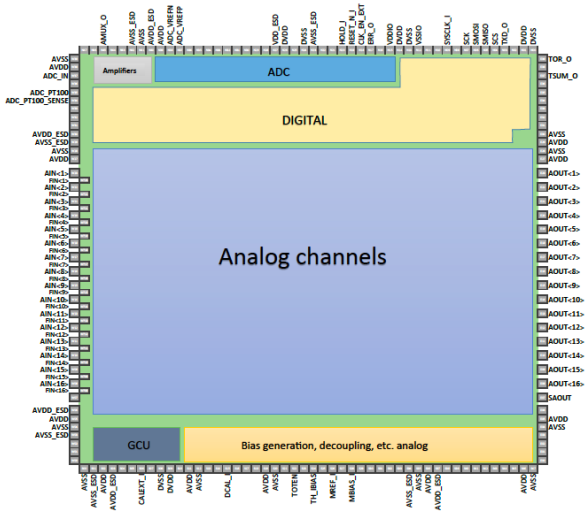


Figure 6: ASIC signals and chip pad frame.

At the center there are the analog channels with the input signals on the left side and output signals on the opposite side. The channels receive bias currents from the bias generation network, which generates all internal bias currents and voltages from one external reference bias current (`MBIAS_I`). The gain calibration unit (GCU) is near the inputs and allows one to inject calibrated charges up to 50 pC into any CI and measure the gain. The ASIC has a digital part with the serial peripheral interface (SPI), the readout controller, and the serial data interface. The readout controller generates the internal digital signals for the readout and digitization of the pulse heights.

III. ASIC Layout

Figure 7 shows the top-level layout of the chip. The active area is 7.6 mm × 6.8 mm. The SIPHRA has been designed in 0.35 µm CMOS and will be manufactured at AMS. All amplifier inputs are protected by diodes against over-voltage and electro-static discharge (ESD).

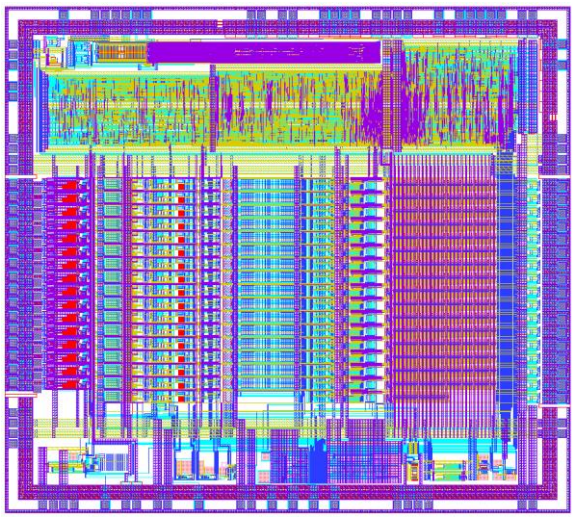


Figure 7: Top-level layout.

IV. ASIC Design Verification

We have performed ASIC design and verification using Spectre/HSPICE, Assura DRC and LVS, QRC for parasitic extraction, ModelSim for functional simulation and coverage, Encounter for digital implementation and RTL Compiler for synthesis and connectivity verification from digital to analog. We have verified the combined analog and digital circuit as follows:

1. Waveforms from the digital circuit simulation in ModelSim were used as input to analog simulations in Spectre/HSPICE.
2. We performed post-layout simulation on a fully extracted channel and analysis on the top-level analog part of the chip.
3. Top-level physical verification used the combined analog and digital circuit and performs layout versus schematics (LVS) and design rule checks (DRC) with Assura.

We have completed the design and verification and we have submitted the GDSII files to the foundry. The simulations were performed with SiPM directly coupled to the CMIS input. The SiPM model assumes 3.4-nF capacitance and 10-µA leakage current from pixel dark counts. The following are important outcomes of the design verification.

1) Power Dissipation

The total power dissipation is about 30 mW, corresponding to 1.87 mW/channel on average. The analog circuit power dominates, while power from the digital circuit is negligible. The CMIS contributes with about 15 mW, and, if the application permits, CMIS can be powered off, leaving a total power of about 15 mW.

2) Pulse Shaping

Figure 8 shows the simulated waveforms at the output of the CI and the shaper for different shaping time setting and the same negative charge injected into the CMIS input. The CI pulse rises when the negative charge is injected into the CMIS input (arbitrarily chosen at 5 µs). The shaped pulses peak after about 300 ns, 500 ns, 900 ns, and 1650 ns, which is only slightly longer than the nominal shaping time settings. The difference between shaping and peaking time is because of the 200-ns rise time of the CI output.

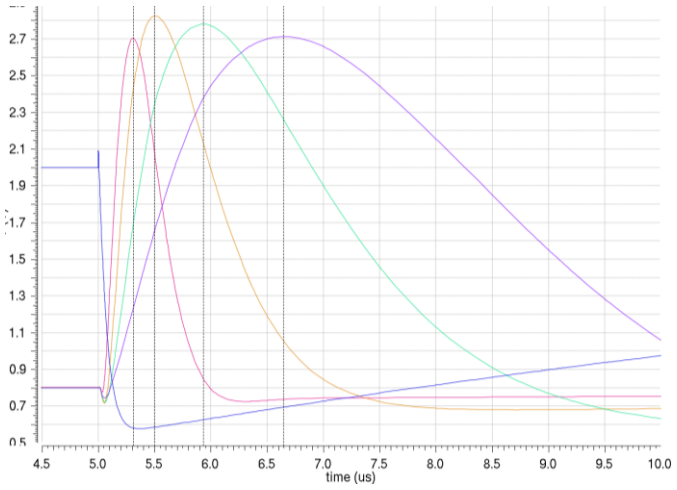


Figure 8: CI and shaper outputs at different shaper settings.

3) Input Charge Range, Noise and Dynamic Range

Figure 9 shows the simulated shaped signal at `AOUT` for different negative charges injected into CMIS. For the 6 charges shown (-3.9 nC, -7.75 nC, -11.6 nC, -15.5 nC, -19.4 nC, -23.3 nC), the semi-Gaussian pulses peak 500 ns after charge injection. The pulse shape for -23.3 nC distorts as the output voltage approaches the supply voltage of 3.3 V.

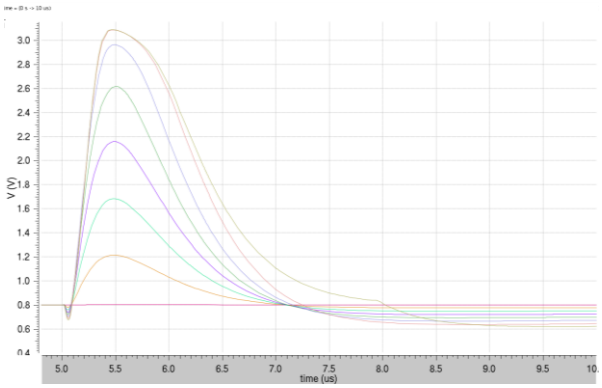


Figure 9: Shaped signal at AOUT for different negative charges at CMIS input.

Figure 10 shows the simulated peak values versus negative charge for the different attenuation settings and at 500-ns peaking time. The peak values increase linearly and saturate at different charges depending on the attenuation. We define the saturation charge as the charge where the pulse height reaches 90% of the supply voltage, i.e. 2.97 V. Table 2 summarizes the simulation results. One can see that the saturation charge increases, as expected, by factor 10 as the attenuation is changed from 1/10 to 1/100, and by factor 2 as the attenuation is changed from 1/100 to 1/200 and to 1/400.

Table 2 also lists the simulated equivalent noise charge (ENC). This simulation was done with the SiPM directly coupled to the CMIS input. The noise increases by factor 2 as the attenuation decreases by factor 2. However, the noise at attenuation 1/10 is larger than one would expect by scaling of the attenuation. The dynamic range, defined as the ratio of the absolute saturation charge and the equivalent noise charge, is between 6000 and 8228 for the 3 largest CMIS attenuation settings. The dynamic range corresponds to almost 13-bit resolution, and thereby exceeds the 12-bit on-chip ADC resolution.

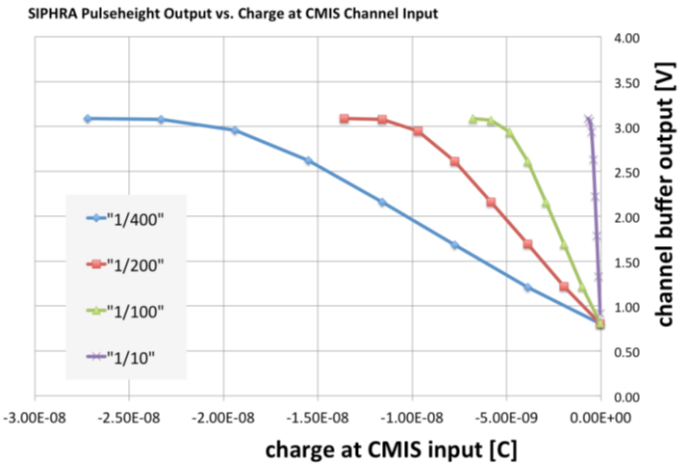


Figure 10: Charge range for different CMIS settings.

Table 2: Simulation results: saturation charge, equivalent noise charge (ENC) and dynamic range.

CMIS gain	Shaping time [ns]	Saturation charge [pC]	ENC [pC]	Dynamic range
1/10	200	-510	0.24	2125
	400		0.28	1821
	800		0.28	1821
	1600		0.28	1821
1/100	200	-4980	0.83	6000
	400		0.73	6822
	800		0.67	7433
	1600		0.63	7904
1/200	200	-9830	1.62	6068
	400		1.40	7021
	800		1.28	7680
	1600		1.18	8331
1/400	200	-19500	3.27	5963
	400		2.80	6964
	800		2.56	7617
	1600		2.37	8228

4) Readout Trigger Threshold Range

Table 3 shows the trigger threshold charge range from the absolute minimum to maximum value for the CMIS gain settings, simulated with the default SiPM at the CMIS input. One can see that the threshold range covers the entire charge range that can be read out for pulse height spectroscopy.

Table 3: Trigger threshold range.

CMIS gain attenuation	Trigger threshold charge range	
	Minimum [pC]	Maximum [pC]
1/10	-4	-560
1/100	-43	-5400
1/200	-87	-10800
1/400	-175	-20900

5) Readout Cycle

Figure 11 shows the signals that are important for the SiPM readout: the current pulse is injected at `AIN`[1], the current integrator output rises, and the shaped pulse appears at the shaper output. The hold signal is automatically generated, and the pulse height appears at `AOUT`[1]. The charge trigger, QT[1], activates and a trigger pulse appears at the trigger-OR output, TOR_O. The channel multiplexer, CAMUX, and the ADC clock are activated internally. The internal clock is synchronous with the externally applied clock (not shown). About 22 clock cycles after internal HOLD was activated, the ADC data becomes available at `TXD_O` (not shown). The readout ends with an internal reset.

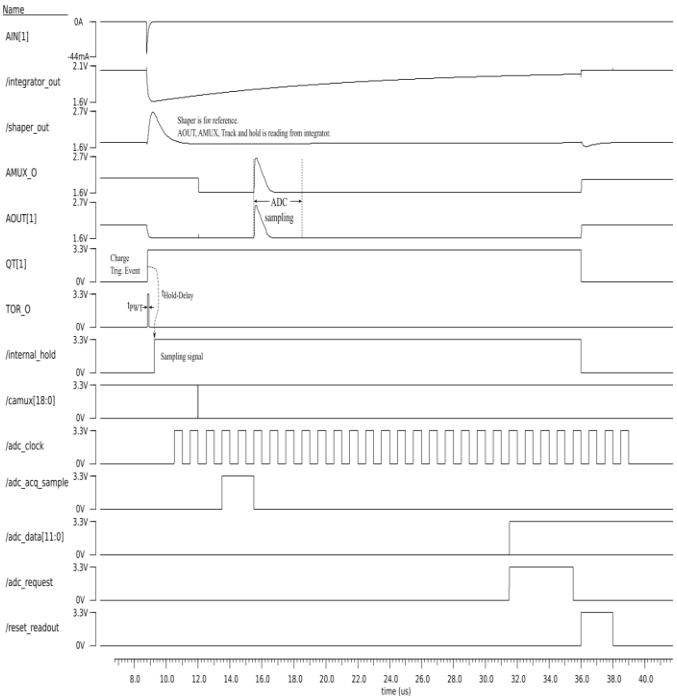


Figure 11: Simulation of signals in the channel.

V. ASIC Tests and Design Validation

Figure 12 shows the block diagram of the SIPHRA ASIC design validation system. The test system is based on the Xilinx Zync-7000 system-on-chip and custom-made firmware for the SIPHRA ASIC readout and control. The system is controlled via Ethernet from a standard computer. The SIPHRA ASIC is located on the ROIC test board, which allows one to connect to the detector array via standard SMA connectors or pin-rows. The test software is programmed in National Instruments LabView.

Preliminary design validation results are available from test devices: We have manufactured test devices with the ADC, SPI, registers and buffers, and have tested these design with respect to radiation. We measured a single-event-upset threshold of 50 MeVcm^2/mg and we do not observe any latch-up up to the maximum tested energy of 135 MeVcm^2/mg [7].

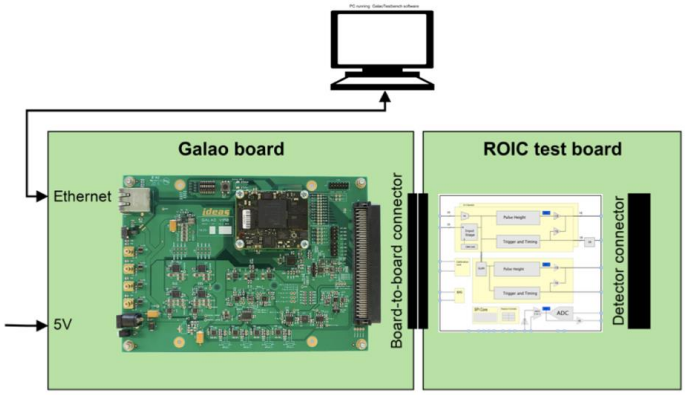


Figure 12: Block diagram of the ASIC design validation and test system.

VI. Summary

We have designed an integrated circuit (IC) for the readout of photomultiplier tubes (PMTs), silicon photomultipliers (SiPMs), and multi-pixel photon counters (MPPCs). The IC has 16 input channels and one summing channel. Each channel can be used for pulse height spectroscopy and timing. The current mode input stage is designed for large negative charge depending on the programmable attenuation and accommodates large capacitive load and large leakage current. Each channel has one output that can be programmed to provide either the analog signal from the current integrator, the shaper, or the digital trigger pulse, or time-over-threshold. The channel output allows one to test many features for further developments of the circuit. SIPHRA has a built-in ADC that automatically digitizes the pulse height and outputs serial digital data. The SIPHRA design will be manufactured in Q2 2016, and samples will be available in Q4 2016.

VII. Acknowledgements

We would like to acknowledge the support from the European Space Agency (ESA contract number 4000113026), the Norwegian Space Center (contract number BAS.05.14.1), and the University of Geneva.

VIII. References

[1] J. Greiner et al., “GRIPS Gamma-Ray Imaging, Polarimetry and Spectroscopy”, arXiv:1105.1265, see also http://www.grips-mission.eu

[2] Xin Wu et al., “PANGU: A High Resolution Gamma-ray Space Telescope”, arXiv:1407.0710v2, 17. Jul 2014.

[3] S. Zhang et al., "The High Energy cosmic-Radiation Detection (HERD) Facility onboard China's Future Space Station", arXiv:1407.4866 , 18. Jul 2014.

[4] SensL, SiPM Datasheet, “C-Series Datasheet, Low Noise, Blue-Sensitive Silicon Photomultipliers”, Rev. 2.1, Preliminary, December 2015.

[5] IDEAS IDE3466 ASIC for RADEM on JUICE, Datasheet, and Proc. SPIE Astro. 2016.

[6] IDEAS NIRCA, Near Infrared Readout and Controller ASIC, Datasheet, and accepted for Proc. SPIE DSS, 2016.

[7] P. Paahlsson et al., “Preliminary validation results of an ASIC for the readout and control of near-infrared large array detectors”, Proc. SPIE 9451, Infrared Technology and Applications XLI, 94512J (4 June 2015); doi: 10.1117/12.2180439

A New Mixed ASIC for Mars Surface Application

José F. Moreno Álvarez[1], Javier Alberola Perales[1]

[1]CRISA (an Airbus Defence and Space company)
Calle Torres Quevedo 9 (Parque Tecnológico de Madrid)
28760 Tres Cantos (Madrid) SPAIN

jose-francisco.moreno-alvarez@airbus.com, javier.alberola@airbus.com

Abstract

In this paper, a mixed-signal ASIC is presented, to be used in the rover of the Mars 2020 NASA mission. The ASIC is part of one of the rover's scientific instruments: the Mars Environmental Dynamics Analyzer (MEDA). The ASIC's main purpose is to digitize the information of the Wind Sensors and send it to the Instrument Control Unit (ICU) through a simple serial link (UART), so reducing the harness and saving a significant amount of mass. This forces the ASIC to be next to the wind sensors, and so exposed to the extreme Martian temperatures, between -128ºC to 50ºC. The operation within such extended temperature range without degrading the performances presents a big challenge to the ASIC design.

I. INTRODUCTION

The Mars 2020 mission includes a rover designed to investigate key questions about the habitability of Mars, and assess natural resources and hazards in preparation for future human expeditions. The mission is part of NASA's Mars Exploration Program, a long-term effort of robotic exploration of the Red Planet.

Mars Environmental Dynamics Analyzer (MEDA) is one of the Mars 2020 rover instruments being developed for the mission. MEDA will include a sensors suite to provide measurements of Mars near-surface atmosphere and ground temperatures, wind speed and direction, pressure and relative humidity. It includes also a sky pointing camera, and a set of photo-detectors for sky imaging and measurement of ultra-violet, visible and near-infrared irradiations at several bands, allowing characterizing the atmospheric dust profile.

MEDA wind sensor data acquisition will require the use of mixed-signal electronics to implement the front-end interface for the wind sensor transducers. Two of these sensors are accommodated mounted orthogonally to the Remote Sensing Mast (RSM) of the Rover. If the electronics is near to the transducers, and remotely connected to the rover's Instrument Control Unit (ICU) through a simple serial link, the harness is notably reduced, saving a significant amount of mass. However, if the mixed-signal electronics is near to the transducers, it will be exposed to the Martian extreme flight acceptance temperatures, between -128ºC to +50ºC. The problem is not only the temperature range per se, but the fact that for a given sol, the temperature excursion can be of more than 70 to 100 degrees Celsius, so, when accumulated during all the mission (1.5 Martian years equivalent to 3 Earth years) all materials suffers from extreme wear-out and fatigue. The application (the ASIC) must be also demonstrated to withstand three times the mission life, that is, 3015 thermal cycles.

This precludes the use of conventional space qualified semiconductors, which are typically down limited to -55ºC and not designed for withstanding those thermal cycles. To overcome this challenge, a mixed-signal ASIC with an operating temperature range of -128ºC to +110ºC has been defined, specified and developed. The ASIC need also to be packaged using specific materials and processes designed to counteract that fatigue. This was the case also of the previous ASIC developed for the REMS instrument on board Curiosity Rover. In this case, the REMS ASIC needed some warming up heating before reaching its performance operation temperatures, thus worsening the fatigue and wearing-out effects because extra thermal stress was happening on each measurement cycle. Therefore, the REMS ASIC needed to be tested to over 10.000 thermal cycles without showing any functional, electrical or mechanical degradation. The experience and heritage taken during the REMS ASIC development have been applied to the MEDA ASIC from the beginning to define the ASIC functionalities, the technologies and the verification program.

The design should counteract also the radiation effects, specially the single event effects (circuit latch up or single event upsets or functional interruptions that may be produced). And withstand a high neutron dose too, contributed from the Rover Thermo Electric Generator. Total dose required is low, less than 10 Krads(Si) typically, coming mainly from the exposition during the cruise to Mars mission phase, but needing to be taken into account.

The wind speed and direction are detected by the Wind Sensors using sigma-delta control loops. A wind sensor comprises four dice in a square (refer to Figure 1), each one with a temperature detector and a heater. The sigma-delta loops force the four dice to reach the same temperature, by applying the necessary power to each heater. Depending on the wind speed and direction, the loops will have to apply more power to one heater or another. Thus, by knowing each heater's applied power, is possible to calculate the wind speed and direction in one point (one die). Also, when the wind is flowing from a given direction, there is some thermal

exchange between the four dice; the leeward dice receive some heat extracted by the wind from the windward ones. Those heat exchanges are measurable (because affects to the power needed to maintain the temperature setpoint of the dice) and therefore permits MEDA to calculate the wind direction.

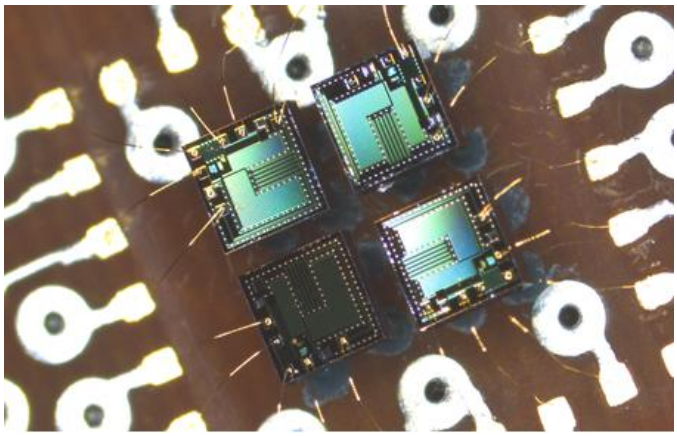


Figure 1: Wind Sensor Assembly dice (zoomed).

There are six of such assemblies (named Wind Sensor Transducers) per Wind Sensor equipment, each with four dice and each die requiring one control loop. For modularity reasons and backwards compatibility with the REMS ASIC, the MEDA ASIC implements twelve control loops to interface with just three Wind Sensors Transducers.

In addition to acquire the wind sensors information, the ASIC includes up to nine analog channels to interface other type of sensors, like thermocouples, thermopiles or resistance temperature detectors (RTDs). This enhances the ASIC front-end capabilities, expanding the applications range, and covering possible unexpected needs in MARS 2020 or in other future missions.

A digital state machine controls the wind sensor loops and analog acquisitions. It also communicates with the Instrument Control Computer accommodated inside the Rover equipment bay through an UART interface, receiving configuration data for the different acquisition modes, and transmitting the wind sensors and analog acquisitions digitized data. Also, if a SEU is detected, it is reported to the ICU through this serial channel.

MEDA-WS- FE ASIC key features:

- 12 sigma-delta control loops for three wind sensors. 14-bit resolution for 0.5Hz and 1Hz acquisitions, and 13-bit resolution for 2Hz acquisitions.
- 9 analog channels (switchable gain preamplifier + 15-bit ADC) with internal calibration, to acquire RTDs, thermocouples and/or thermopiles.
- Digital machine to configure and control the wind sensor and the analog channels, with SEU detection.
- 19200 baud UART with RS-422 interface.
- Over-temperature protection for the ASIC and the wind sensors.
- Internal housekeeping telemetries: Junction temperature and supply voltage.

The ASIC design have been developed by the Instituto de Microelectrónica de Sevilla (IMSE-CNM) and Crisa, with AMS 0.35 process, using radiation hardened by design technologies. Building blocks and libraries were previously characterized in temperature to -110ºC in the frame of other projects. First ASIC prototypes have been manufactured and started testing in February 2016. ASICs are completely operational and preliminary results are showing to be very promising confirming the expected performances. Once validated, we have the option to go for a second design to foundry iteration, to fine tune and improve functionalities if needed or to launch just the flight lot production.

The ASIC will be packaged by using a high reliability ceramic CQFP-100 package, the same that used for REMS, using a specific process (an adaptation of the standard QML process of the packager company) to make them more robust against the thermo-mechanical fatigue and wear-out effects as did for the REMS ASIC. The ASIC will be afterwards submitted to a full screening and lot qualification process according to EEE-INST-002 “Instruction for EEE parts selection, screening, qualification and derating”

II. Wind Sensors Operation

Each Wind sensor operates by heating its four dice to reach the same reference temperature. This is accomplished with four sigma-delta loops sharing a common temperature reference. The ASIC is capable to manage three wind sensors transducers, each with their’s own temperature reference.

The sigma-delta loop is shown in the block diagram of Figure 2. The temperature reference comes from a DAC (not shown), which is common to the three dice of each sensor. The die temperature is measured by its RTD element, and compared with the reference. If the die temperature is lower than the reference, the I_{delta} current (see Figure 2) will be applied to the die heater. Else, the I_{delta} current will be applied to an external resistor through the pin $I_{SINK}[n]$. In both cases the I_{delta} current source is active, thus achieving a constant current consumption fron the ASIC supply pins. This is necessary, because the ASIC is supplied by the ICU, which is at several meters (4.5m typically) from the ASIC due to MEDA accommodation and rover cabling constraints , so the supply inductance would cause an intolerable voltage ripple if the current consumption is pulsed. Some decoupling capacitors are placed next to the ASIC, but the total capacitance is relatively small due to space constraints, so a continuous current consumption is mandatory.

The I_{base} current source is always active, giving constant heating power. Both I_{base} and I_{delta} are configurable for each die, to optimize the operation of the wind sensor algorithm. This algorithm, which is performed by the ICU, sets the reference temperature and I_{base} - I_{delta} currents, depending on the Martian air temperature.

A 14-bit counter will accumulate the number of heating pulses (I_{delta} pulses) per cycle. From that number, the heating power needed to maintain the die at the reference temperature can be inferred. The integration period for the accumulator is configurable to 0.5s, 1s or 2s. For the first case, the resolution is limited to 13-bit.

Note that the voltage ripple at the die RTD is far below 1mV, so a regenerative microvolt-comparator with auto-zero feature is used.

The finite rise/fall time of the I_{delta} switch may introduce some error in the applied power. For example, if the rise time is faster than the fall time, the applied power will be higher when the I_{delta} pulses are separated than when they are adjacent. If the rise time is slower than the fall time, the opposite will happen. To overcome this, is possible to "cut" the I_{delta} pulses near it's end, guaranteeing that, if there are N I_{delta} pulses, there will be N rise times and N fall times, regardless if the pulses are adjacent or separated. This refinement is done with an internal "Duty" signal, which can be enabled or disabled, to cut or not cut the length of the I_{delta} pulses.

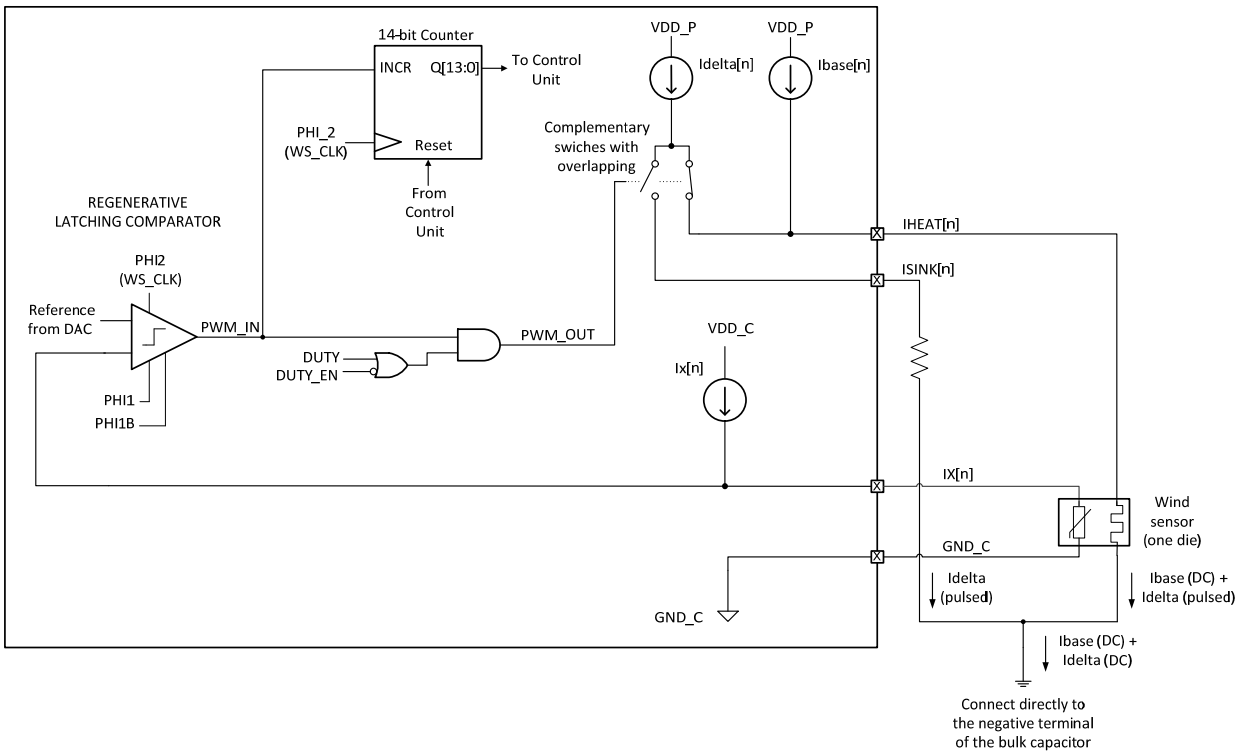


Figure 2: Wind sensors Sigma-Delta loops

III. Analog Acquisition Operation

For the analog acquisitions, a double ramp 15-bit ADC is included. It uses a voltage reference derived from the ASIC's bandgap reference. This voltage reference implements a curvature correction technique, to compensate the wide operating temperature range of the ASIC.

The ADC is driven by an input preamplifier with two switchable gains: 1V/V and 150V/V. The low gain is used to measure RTDs, and the high gain is used to measure thermocouples or thermopiles. For the RTD measurements, a current source is used. The current value is configurable to accommodate to different RTD types or values.

Both the preamplifier and the current source are multiplexed between nine differential input channels. Each channel can be configured with its own gain and current source value, if applicable. The multiplexing technique, apart from reducing silicon area, guarantees that the characteristics of all channels are equal. Furthermore, as the current source and the ADC are referenced to the same bandgap voltage, the RTD measurements are completely ratiometric, eliminating the error due to the reference. This also happens with the temperature measurements of the sigma-delta reference loop.

Figures 3, 4 and 5 show the ASIC equivalent input circuits when configured to measure two RTD types (Pt7200 and Pt1000), or a thermocouple. Note that for thermocouple measurements, the voltage could be either positive or negative, hence the offset applied to the amplifier. In this figure, there is no cold junction thermocouple. Instead, the connection between the ASIC and the thermocouple wires acts as a "cold" junction (which can be colder or hotter than the called "hot" junction). Actually, the ADC would measure the temperature difference between the ASIC and the thermocouple tip. But the ASIC temperature is always known, because the bandgap circuit gives also a PTAT (proportional to absolute temperature) voltage, which can be captured by the ADC.

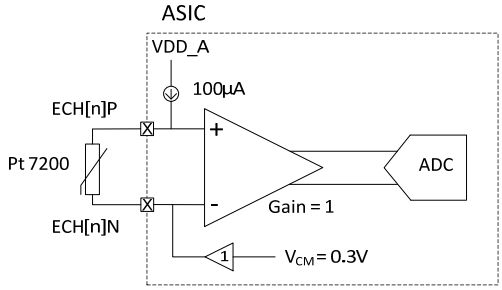


Figure 3: ASIC equivalent input circuit when configured to measure Pt7200 RTDs.

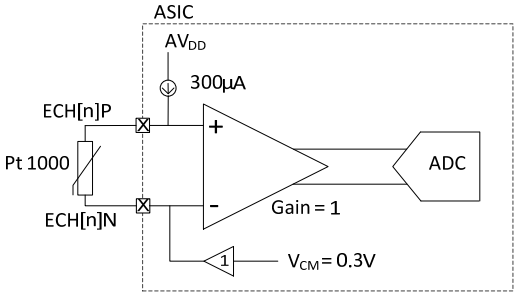


Figure 4: ASIC equivalent input circuit when configured to measure Pt1000 RTDs.

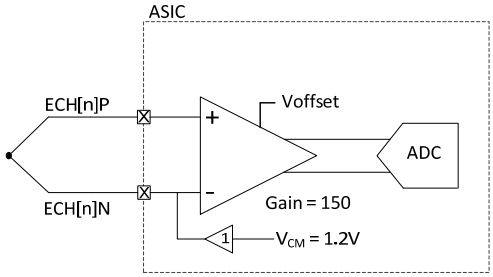


Figure 5: ASIC equivalent input circuit when configured to measure thermocouples or thermopiles

Apart from the 9 external channels, the ADC is multiplexed to 11 internal signals:

- The output of the three DACs, which set the reference temperatures for the sigma-delta loops.
- A fraction of V_{DD}, to monitor the supply voltage.
- The internal temperature measurement, derived from PTAT signal at the bandgap voltage reference.
- Six calibration voltages, three for the low gain and three for the high gain configuration.

IV. ASIC Specifications

The key ASIC specifications are detailed in the following list:

- Operating voltage: 3.3V ± 5%. Maximum rating: 3.6V.
- Operation temperature: -128ºC to +50ºC
- Wind sensor loops characteristics:
  - ✓ Current source mismatch: ±0.8%
  - ✓ I_{base}-I_{delta} compliance: 2.3V
  - ✓ Ratiometric measurements
- Analog channels characteristics:
  - ✓ RTD measurements accuracy: ±1.9ºC
  - ✓ Thermocouple measurements accuracy: ±3ºC for E-type
- Radiation characteristics:
  - ✓ TID = 9krad (Si).
  - ✓ No Latchup to a LET of 75MeV-cm2/mg.
  - ✓ No SEU to a LET of 37MeV-cm2/mg.

The ASIC block diagram is shown in figure 6.

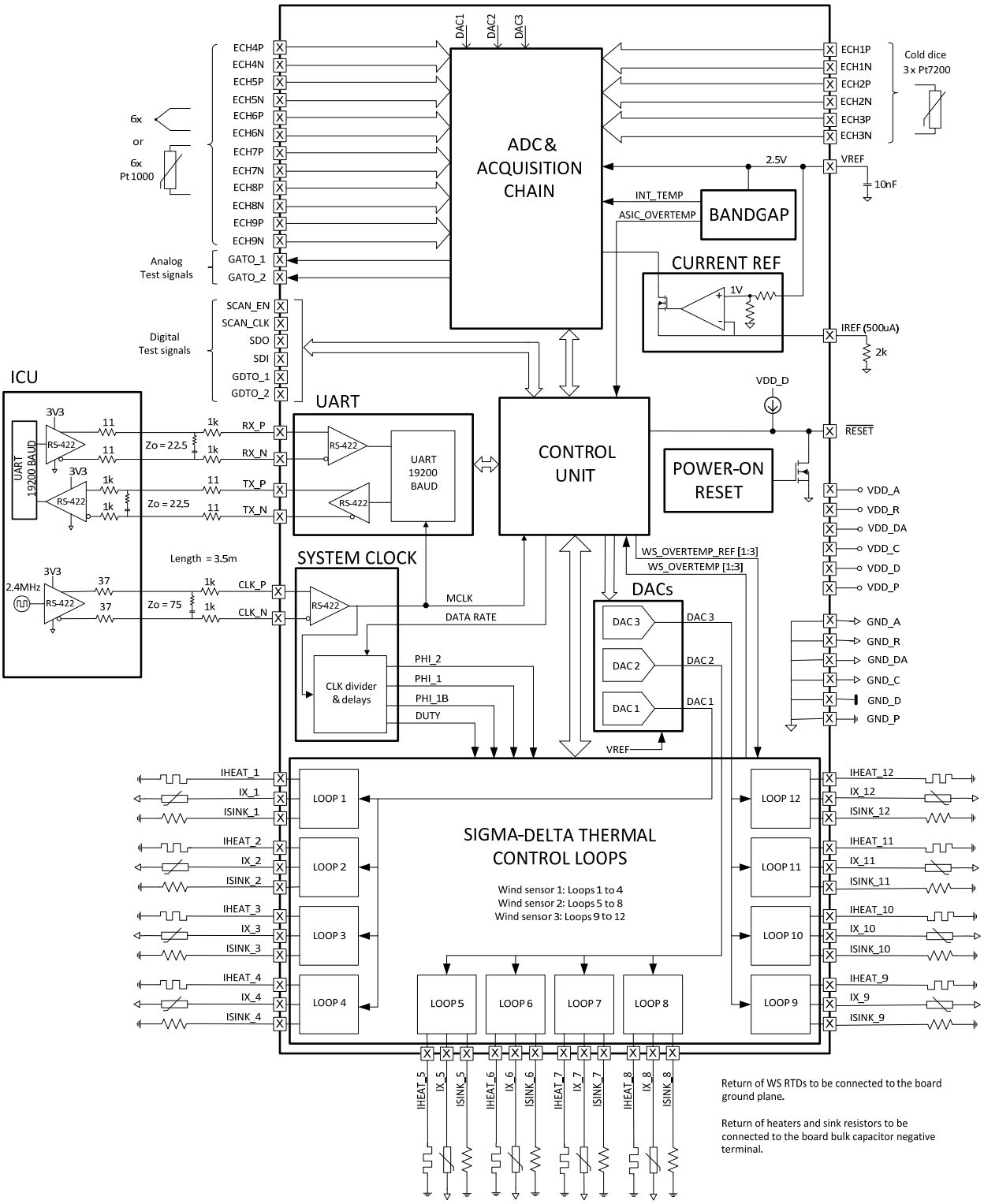


Figure 6: ASIC block diagram

V. Acquisition Board

Each acquisition board is a multi-segment flex-rigid PCB containing one ASIC and three Wind Sensors Transducers. There are two acquisition boards per boom. It also contains the minimum passive components needed by the ASIC: decoupling capacitors, bulk resistors to derive the I_{delta} currents when they are not heating the dice, and a reference resistor to obtain a current reference from the bandgap voltage reference. This current source acts as a master current source, and all the ASIC current sources, including I_{base}'s, I_{delta}'s, and RTD biasings, are mirrored from it.

The acquisition board is exposed to the severe Martian ambient conditions. The passive components have been selected based on their known behavior on extreme temperature ranges (REMS heritage) and are mounted using specific custom techniques allowing them to withstand the thermo-mechanical stresses. Similar approach is followed by the ASIC that is packaged using specific process and materials developed and validated for MSL-REMS and mounted in a very particular way to minimize the thermo-mechanical stresses in temperatures.

Once the ASIC are characterized they will be mounted into their acquisition boards and tested, also in temperature, at Wind Sensor and MEDA levels.

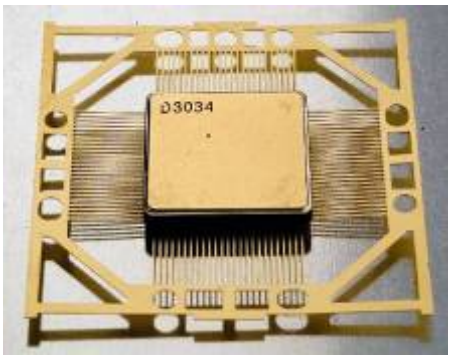


Figure 7: REMS ASIC package. Same package/same process will be used for MEDA.

VI. Conclusions and Acknowledge

A new custom mixed ASIC have been designed for withstanding the very harsh Martian environment. It is an enabler of the Mars Environmental Dynamic Analyser research instrument for the Mars-2020 new rover from NASA-JPL. The ASIC developed for MEDA, even being using a new process, is strongly based on the REMS ASIC heritage and technology. Electrical design have been also defined taking into account lesson learns, results and operation constraints from REMS.

The MEDA project is now close to the end of the detail design phase with the MEDA Engineering Model to be manufactured and tested at the beginning of 2017. First ASIC samples have been already manufactured and are presently being characterized electrically and in temperature. Successful results of testing to date allow us to look forward with confidence for the manufacturing and screening and qualification of the flight parts.

Authors want to express their gratitude to the whole MEDA team, composed of many people and many researching and engineering collaborating institutions who are contributing with their time, energy and expertise to make MEDA a reality.

MEDA is a Spanish contribution to NASA. MEDA works to date has been funded by the Spanish National Plan for Space (PNE) depending on the Spanish Ministry of Economy.

VII. References

[1] José F. Moreno, Javier Gómez-Elvira, Antonio Peña and Jaime Serrano (May 2009). Data Systems on Aerospace (DASIA) 2009 Conference. The meteorological station for NASA's 2011 Mars Science Laboratory rover.

[2] Jose-F. Moreno-Alvarez (September 2010). Analog and Mixed-Signal Integrated Circuits for Space Applications (AMICSA) 2010 conference. The Strategy for qualification and mission validation of a mixed ASIC developed for next NASA Mars mission.

[3] Jose F. Moreno-Alvarez, Antonio Peña-Godino, Jose Antonio Rodriguez-Manfredi, Elizabeth Cordoba. Data System in Aerospace (DASIA) 2016 conference (Pending publication). MEDA, the new instrument for Mars environment analysis for the Mars 2020 mission.

MEDA Wind Sensor Front End ASIC

S. Espejo, J. Ceballos-Cáceres, A. Ragel-Morales, S. Sordo-Ibáñez, L. Carranza-González, J.M. Mora-Gutiérrez, M.A. Lagos-Florido, J. Ramos-Martos

IMSE-CNM (CSIC/Universidad de Sevilla)
Parque Científico y Tecnológico Cartuja, Calle Américo Vespucio s/n, 41092, Sevilla, SPAIN

mailto:espejo@imse-cnm.csic.es

Abstract

This paper describes a rad-hard, mixed-signal ASIC designed in a standard 0.35 μm CMOS technology. It has been designed using Radiation Hardening By Design (RHBD) techniques aimed to reduce Single Events Effects (SEE) and to mitigate the effects of ionizing radiation. The ASIC function is that of an analogue front-end for a wind sensor that will become part of the Mars Environmental Dynamics Analyzer (MEDA) instruments set, for NASA's Mars2020 mission. The ASIC functionality, circuit approaches, and the RHBD techniques used in the analogue and digital sections are described briefly, and present test results are reported.

I. The MEDA Wind Sensor Concept

The MEDA instruments set [1] is being developed by a consortium led by Centro de Astrobiología (CAB) [2]. The wind sensor in particular is based on a concept developed at the Polytechnic University of Catalonia (UPC) [3],[4]. Essentially, a set of four heated silicon dies, which are spatially placed in a convenient configuration, are kept at a constant temperature over the environmental atmosphere temperature. The heat power required by each of the dies to maintain its temperature is measured, and from there, the wind speed in a direction related to the space distribution of the four dies, is computed.

Each of the four silicon dies includes two platinum resistors. One, R_x, biased with a constant current, is used to monitor the die temperature, while the other, R_{heat}, is used to heat up the die when required. An additional, unheated, identical, fifth silicon die (the cold die) is used to monitor the ambient temperature. Expected values of R_x and R_{heat} (at 0ºC) are in the range of 7.2KΩ and 80Ω respectively.

With a known R_x value at a reference temperature, a known constant current, and the well known, precise, platinum resistivity variation with temperature, there is a precise and stable correspondence between the voltage at R_x and temperature. In what follows, temperature measurements will be implicitly understood as voltage measurements.

Three of these wind speed sensors are used to obtain a complete three-dimensional wind speed vector measurement. This includes some level of redundancy to cope with some crossed effects, as well as with the wind disturbances produced by booms and other solid elements located within the rover vehicle in the vicinity of the sensors.

II. The MEDA Wind Sensor Front End ASIC

From the previous description, measuring the wind-speed vector requires monitoring the temperature of 15 silicon dies (3 x (4 +1)), and heating 12 of them, as needed, depending on their measured temperatures, so as to maintain their temperatures constant. The heating power (average current) delivered to each of the 12 hot dies must also be measured.

Temperature measurements are based on current-biased platinum resistors. The biasing currents must also be provided by the ASIC. The temperature of the 12 hot dies must be monitored continuously, within feedback loops, so as to maintain their temperatures constant. The measurements of the temperatures of the 3 cold-dies may be time multiplexed.

In fact, the hot dies temperature just need to be compared to a reference goal-temperature, in order to act on the heating current, in feedback loops. The actual values of the hot dies temperatures are not required. Therefore, simple voltage comparators (as opposed to analogue-to-digital converters) can perform that function.

On the other hand, the ambient atmosphere temperature, meaning the temperatures of the cold (unheated) dies, is actually needed, with their real values, because this information is required to establish the correspondence between the power delivered to the hot dies to maintain their temperature constant, and the wind speed. This means that precise voltage values must be measured. For signal integrity reasons, ease of communication, etc, ADC conversions are convenient and are done within the ASIC, close to the hot and cold dies. The ADC is then used to measure other magnitudes in the ASIC, like its own internal temperature (from a PTAT circuit), the power supply voltage, some internally-generated calibration levels for the ADC, etc, as well as other external magnitudes, essentially temperatures, used for instrument house-keeping functions.

Implicitly, it is clear that temperature stability of the ASIC is very important for precise measurements. In particular, concerning the bias currents and the voltage reference of the ADC. The ambient temperature operation range is quite large, as usual in space applications: -128 to 50 ºC. The operating die temperatures range will certainly be above those limits, due to self-heating. Precise analysis is still underway, depending on the final package thermal properties and the final heat flow from the package to the PCB and to the low density Mars atmosphere. The power dissipated within the

ASIC has significant variations as well, depending on the programmed values for the heating current sources.

In summary, the ASIC must contain an ADC, with a multiplexer for measuring several internal and external voltages, must provide current biasing for external platinum resistors, and must include 12 thermal control loops (each comprising current biasing, voltage comparison, and conditional heating currents). Three voltage-output DACs, one per wind sensor, are also included in order to set the reference goal-temperatures of the four hot dies. Here, again, the correspondence between voltage and temperature is based on the platinum resistivity variation with temperature, a known resistance value at a reference temperature, and a constant-current bias.

Finally, the ASIC contains a digital finite state machine (FSM) for functions control and data communications with the external instrument control unit (ICU).

The ASIC specification and design-process quality control have been done by CRISA [5]. CRISA has also been in charge of the high-level digital code of the control and communications FSM. IMSE-CNM-CSIC has been responsible for the design of the ASIC, including its analogue architecture and blocks, and the synthesis and back-end of the digital part.

The ASIC has been developed in a standard 0.35μm CMOS technology from AMS [6]. This technology, which is specially well suited for medium frequency, medium complexity, analogue and mixed-signal designs, allows the use of 3.3V and 5.0V transistors, among other several options. Only 3.3V transistors are used along the chip, simplifying the design and avoiding the larger ionizing radiation effects on thick gate-oxide transistors.

Along the past years, the authors have done previous efforts in the characterization of radiation and low-temperature effects on devices in this technology, in the development and validation of a rad-hard library of digital cells, and have developed several other mixed-signal space ASICs. [7],[11].

Figure 1: at the end of the paper shows a layout of the MEDA WS FE ASIC.

III. Functionality

Figure 2:, also at the end of the paper, contains a symbolic block diagram of the ASIC. There are three major functional blocks:

- Digital Control Block
- AD Conversion Channel
- Thermal Control Loops

and a number of auxiliary circuit blocks:

- RS-422 Transmitter and Receivers
- Power-On Reset (POR)
- Voltage and Current References Block
- Band-Gap
- Input-Signals Multiplexer
- Signal Conditioning Block
- ASIC Temperature Indicator
- VDD level indicator
- ASIC Temperature Alarm
- Wind-Sensors Temperature Alarm
- Signals Observation Multiplexers

Figure 2: shows the external connections of the ASIC as well, using dashed lines. There are three major pin sets:

- ICU connections
- External sensors (channels) connections
- External hot dies connections (including power sinks)

In addition, we have a number of power domains:

- VDD and GND connections

and a number of auxiliary/miscellaneous connections

- External biasing resistor (Iref) and Vref connections
- External reset and Power-On-Reset observation
- Scan Path
- Global observation nodes, analog and digital

The following paragraphs describe the circuit blocks and their functionality, and the external connections of the ASIC.

IV. External Interface

From an upper system perspective, the MEDA-WS-FE ASIC communicates with the so called Instrument Control Unit (ICU). The communication is performed through a serial, bidirectional, asynchronous link (UART) that uses an RS-422 differential physical interface. This interface serves both for control (commands) and data transmission purposes. Four pins are used for the differential, bidirectional data transmissions. A master 2.4MHz clock, used to govern the digital control block, is sent by the ICU to the MEDA-WS-FE ASIC using the same RS-422 physical layer. Two more pins are used for this purpose. The ICU connections require therefore a total of **6 pins**.

The ADC conversion channel is used to digitalize external and internal signals. Nine differential input ports are available on the ASIC, making a total of **18 pins**.

Concerning the 12 thermal control loops, for the 12 hot dies, each of them requires a pin for the current biasing of R_x, the platinum resistor used for temperature monitoring. This same pin (its voltage) is used as input to the comparators in the temperature-control feedback loops. Each die requires an additional pin for its heating current. The heating current, which can be quite large (up to 30mA for each die), is partially switched on and off from the heating resistor of each hot die during the operation of the feedback loop. The ASIC specs require the total current consumption of the ASIC to be constant, in order to avoid excessive ripples in the power supply. For this reason, the heating currents are maintained invariant in time, and (partially) switched to alternative, "power-sink" external resistors. One power-sink external resistor is used for each hot die, requiring a total of 12 pins. The power-sink resistors need to be external, as opposed to being built within the ASIC, because of the limits to the maximum power dissipation within the ASIC, imposed by the maximum junction temperature of the ASIC. In summary, each thermal control loop requires three pins, making a total of **36 pins**.

Some alternatives aimed to reduce the number of pins dedicated to power sinking were considered but discarded. One of them was the use of just one external sinking resistor for the 12 loops. This was discarded because the large range of the total current to be sunk, together with the voltage limits imposed by the technology, forced the use of a low resistor value, which in turn resulted in excessive power dissipation within the ASIC under some circumstances. The alternative of using a nonlinear external resistive load (e.g. several series connected diodes) was also discarded due to expected difficulties in finding the proper space-qualified components.

A total of **29 pins** are dedicated to power and ground connections. Six different power domains are used, in an attempt to prevent power and substrate noise generated by noisy environments (digital sections, heating currents, etc) from reaching sensitive nodes (ADC section, and thermal loops comparators). Because of the large heating current sources, which drive external resistors connected to ground, more VDD pads are used than GND pads.

Some additional pins are used for miscellaneous purposes. One pin is used to monitor the global reference voltage V_{REF}, generated internally, from which all other internal voltage levels are derived. Measuring its value for each individual ASIC sample, as well as its variation with temperature, allows a much higher accuracy in the final, calibrated system. An external capacitor can also be connected at this pin in order to reduce the noise bandwidth of the reference voltage. Another pin is used to generate a precise reference current using an external resistor with very low temperature coefficient. The current is derived from the internal reference voltage and the external resistor, using a continuous-time feedback loop. One more pin is used for FSM reset-related functions. It allows the observation of the internally generated reset pulse from the power-on-reset block, as well as forcing an external reset if needed. Four pins are dedicated to a scan-path testability function that was added for the digital control block, and another four pins are dedicated to the observation of many internal analog and digital signals, which can be multiplexed to these four nodes. This makes a total of **11 pins** for miscellaneous purposes.

The ASIC has a **total of 100 pins**. The package used for initial measurements and characterization is a CQFP-100. The final package to be used in the flying modules will also be a CQFP-100 but from a different manufacturer, due to qualification concerns.

V. Signal Conditioning and ADC

The signal conditioning and analogue-to-digital channel is designed to measure external and internal voltages. The principal external voltages to be measured are representative of temperatures, i.e., they are voltage drops generated across external platinum resistors, which must be current-biased. The input to the conversion channel is differential. The ASIC must provide the biasing current, and the voltage at the other end of the resistor. A secondary type of signal to be measured is the voltage across thermopiles. In this second case, some signal amplification is required. The internal signals to be measured include the three DACs outputs (which represent the target hot-dies operating temperatures), one signal representing the ASIC internal temperature, a down-scaled version of the power supply voltage, and six internal reference signals used for conversion channel calibration.

A. The input channels multiplexer

A multiplexer, built using CMOS switches, is used to convey one of the 9 external channels, or one of the 11 internal signals, to the preamplifier input. The on-resistance of the switches does not affect the measured voltages, thanks to the capacitive input impedance of the preamplifier at the input of the ADC. A four wires interface is used for the resistors to be measured, again avoiding the effect of the on-resistance of the switches connecting the bias current and the DC voltage at the other end of the resistor. The complete multiplexer for the differential signals with the four wires interface can be understood as a set of four multiplexers under the same control word. The multiplexer, and the whole conversion process, is controlled by the digital control block.

B. The bias current for the ADC Channel

As mentioned above, the ASIC provides a bias current for measuring resistor values by measuring their voltage under a known current value. Since there is only one conversion channel, the 20 signals (9 external, 11 internal) are converted sequentially, multiplexed in time. This allows the use of one single, programmable current source for all channels. The current source uses a cascode topology for improved output impedance, and can be programmed with four bits from 0 to 750μA in steps of 50μA. The bias current can take different values (including zero) for each of the signals, under the control of the digital control block.

In a similar form, the connection at the other node of the resistor, this is, at the negative node of the differential input signal, can be connected to different reference voltages for each of the channels, also under the control of the digital control block.

C. The ADC channel

Figure 3: shows a simplified block diagram of the conversion channel. It is composed of a preamplifier with two stages, and a dual-slope ADC. The dual-slope ADC is composed in turn of an analogue integrator, a comparator, a finite state machine (the ADC-FSM) for the control of the AD conversion process, and an oscillator used to generate a higher frequency clock for this ADC-FSM.

The ADC is designed to have 16bits (15 + sign) resolution, with conversion times below 1ms. Integral non-linearity and r.m.s. noise have been taken into account in the design, keeping them within the range of a few least significant bits equivalent voltage (V_{LSB}).

1) Preamplifier

A conventional instrumentation amplifier, with a differential architecture, is used at the input of the ADC channel. It provides capacitive input impedance, important to avoid the effect of the on-resistance of the switches in the signal multiplexer. The gain of the amplifier is 1 in general, for all signals to be measured, but can be optionally set to 150

for some external signals, when external thermopile voltages are to be measured. Special care has been taken in minimizing the amplifier offset so as to avoid saturation, in particular with the high gain configuration. Fully differential dual-slope converters often suffer from a zero-crossing discontinuity (or sign-dependent offset). This is not a problem for input signals given by voltage drops at current-biased resistors, or other signals whose polarity is well known a priori. However, this is not the case for thermopile voltages. For that reason, a level-shifting equal to 1/4 the differential input signal range can be optionally added to the input signal, mapping the central 1/2 of the bipolar input range into one side of the amplifier output range. This is done in the second stage of the amplifier, after the signal has been amplified, for accuracy reasons.

2) ADC-FSM

Dual-slope converters perform two time integration processes. The first one begins with a reset integrator (zero initial value) and integrates the input signal, while the second starts with the accumulated result of the first, and integrates the reference signal with sign opposite to the input signal.

The time required, during the second integration period, for the integrator output to cross zero is proportional to the ratio of the input signal to the reference signal. This time is measured using a digital counter, driven by a digital clock. The counter is set to zero at the beginning of the second integration period and stops (or its content is sampled in an auxiliary register) at the zero crossing of the integrator output. The zero-crossing is detected by a comparator, often a clocked, fast, regenerative comparator. The comparator is first used, at the beginning of the second integration, to select the proper polarity of the reference signal.

The ADC-FSM controls the sequence of operations and signal switching required to perform whole process, the clocked comparator, and the digital counter. The clock of this FSM must have a high frequency, because the conversion time is at least 2^N clock cycles, with N being the number of (magnitude) bits, 15 in our case. For that reason, the external 2.4MHz clock was not appropriate, and a higher clock had to be generated on chip.

3) Oscillator

A 50MHz (nominally) oscillator has been included in the ASIC, in order to drive the ADC-FSM. It is a relaxation type, with an RC time constant defined by the same components used in the integrator (same resistor and capacitor options among those available in the CMOS process). This ensures that, even under severe process and temperature variations, the integrator output will not saturate, because the integration time, measured in clock periods, and the integrator time constant become proportional. The oscillator frequency, or its stability with process and temperature, has no effect on the conversion process. Extreme frequency variations are in the range of ±25%, and have to be accounted only for worst-case conversion time. Clock jitter is not a dominant source of noise in this type of converters.

4) Analogue integrator

The analogue loss-less integrator is based on a typical, capacitive fed-back operational amplifier. It is fully differential, with the same common mode level than the preamplifier output. Some switches are required for integrator reset, and to connect the input of the integrator to the input signal or to the reference signal with one or the other sign. Special concerns in the design of the operational amplifier were offset and noise. The integrating capacitance, at each rail, is 90pF. During the first (signal) integration period, which lasts 2^{12} clock cycles, the input resistor is 1MΩ. During the second (reference) integration, which lasts a maximum of 2^{15} clock cycles, the resistor is 8MΩ.

5) Comparator

The comparator operates with the high-frequency ADC clock, in two phases. It is composed of a high-gain, open loop differential preamplifier, followed by a clocked sampling/regenerative stage, in turn followed by a latch. Note that hysteresis, which could be expected from the use of a high-gain preamplifier as a first stage, is not a big concern because the input to the comparator is always a well-behaved, slow ramp. Note also that the preamplifier offset, as well as the delay time of the comparator, with its low input signal at the zero crossing point, represents only an additional contribution to the ADC transfer characteristic offset. The output of the comparator is always well defined from a digital perspective, and well synchronized with the ADC clock.

6) Reference signal

A global reference signal (V_{REF}) of 2.5V is obtained by scaling up the voltage from a band-gap circuit. All other voltage references needed within the ASIC are derived from V_{REF} using a resistive string. In particular, the reference voltage (differential) for the ADC is ±2.0V around a common mode level of 1.5V.

Note that, because the reference signal is differential, the zero reference is error free. Also, the magnitude of the reference voltage for positive and negative inputs is the same, since the same two levels are used with one or the other polarity. The gain of the ADC transfer characteristic is affected by the magnitude of the reference voltage, as well as by several other sources within the ADC circuitry.

D. ADC channel calibration

The chosen type of ADC, a dual slope, is well known to be very linear, and have very good noise figures. On the other hand, the gain and offset errors of the static transfer characteristic can have relatively high values, and may result in measurement errors in the range of many V_{LSB}.

Offset and gain values will be different from ASIC sample to ASIC sample, but they may be measured, for the specific ASIC samples used in the final instruments, and their deviations can then be compensated through calculations. This is not a problem in the context of space applications. In particular, when the final objective is to measure some magnitudes and send the information to Earth, the corrections may be done on Earth, using the ASIC characterization data obtained at the time of building the instruments. However, offset and gain values may change in time due to their dependence with temperature, power supply level, aging, and other causes. For this reason, several fixed input voltages,

derived from the global reference V_{REF}, are included in the ASIC within the set of internal signals that are multiplexed to the ADC input. A careful measurement, on Earth, of the precise ratio of these reference voltage levels to V_{REF}, and assuming that this ratios will not change in time (they are given by ratios of resistors built using the same material, with the same current density, in the same environment, etc), the offset and gain errors of the ADC can be calibrated using correction parameters obtained in real time.

VI. The Thermal Control Loops

The function of the 12 thermal control loops is to maintain 12 external "hot dies" at a constant, prescribed temperature above the ambient temperature, and to measure the amount of heating current required by each external die for that purpose.

The 12 control loops are grouped into three sets of four control loops. The prescribed temperature for the four dies in each group is the same, but can be different from group to group. A digital to analogue converter (DAC) is used to set the reference temperature (equivalent voltage) for each group.

For each loop, the ASIC generates a bias current I_x, of nominal value 100μA, which is used to bias a grounded resistor R_x in the external hot die. The voltage (V_x) at the current output bonding pad (voltage at R_x) is compared to the DAC output. A constant heating current (I_{base}) is permanently applied to the heating resistor (R_{heat}) in the die, and an additional current (I_{delta}) is conditionally applied if the die temperature is found to be below the prescribed temperature. The feedback loop operates in discrete time, under the control of a low frequency clock generated in the digital control block by division of the master 2.4MHz clock. The low frequency can be chosen between 8.2 and 16.4 KHz. The controlling FSM counts the number of times the additional current was applied to each die. A common (to all loops) master counter of 14 bits controls every measuring period. Individual 14 bits counters are used for each loop to store their corresponding data. The overall measuring frequency is 0.5, 1.0, or 2 Hz depending on the selection of clock frequency. For the 2Hz mode, the maximum resolution is 13 bits, instead of 14.

A. *The bias current sources*

The 12 I_x bias current sources have a nominal value of 100μA, but can be individually programmed with 8 bits resolution between 94 and 106μA. This allows a precise compensation of resistors R_x variation (mismatch) from hot-die to hot-die. The current sources are calibrated to produce the same voltage drop in their corresponding resistors, at some reference temperature. This ensures that the four hot-dies in each group are actually kept at the same temperature.

The 94μA current source and the 0 to 12μA current-output DAC are implemented using conventional topologies. Again, cascode transistors are employed for high output impedance. The cascode transistors are also used as switches in this case.

All current values are derived from the reference current I_{REF} (see below) using current mirrors. High area transistors and careful layout techniques are used to minimize the effects of mismatch.

B. *The comparator*

A voltage comparator in each loops determines if the hot-die temperature is above or below the temperature prescribed for its group. It compares the voltage V_x at resistor R_x with the DAC output corresponding to the group. The result of the comparison is sent to the digital control unit which, if the temperature is lower than prescribed, enables the additional I_{delta} heating current and increases the digital counter used to measure the additional power delivered to that hot-die. This is repeated at the pace of the low frequency clock, under the control of the digital control block.

This comparator is a clocked, switched-capacitor comparator, with auto-zero. It is followed by a latch and a flip-flop, ensuring that the digital signal reflecting the result of the comparison is well defined during the whole clock cycle, with a relatively small delay (as compared to the slow clock cycle) after the hot-die temperature sampling instant. The control signals required by the switches in the comparator are generated by the digital control block.

C. *The heating current sources*

Heating current sources, I_{base} and I_{delta}, have some particular design concerns, because their maximum values are quite high. Each of them can be programmed, with common values for each group of four loops, from 0 to 15mA, with four bits resolution. This programmability is introduced because of the wide range of environmental conditions expected, which requires wide ranges of permanent and switchable heating powers. If all I_{base} and I_{delta} were set to their maximum values, the total current would be 360mA.

Special care has been taken in the power supply routing, using very wide metal lines, over the transistors area. Simulations of the distributed resistance effect have been carried out to ensure that the voltage drops in the power supply do not affect the current sources accuracy. Again, the current values are derived from the reference current I_{REF} using current mirrors. High area transistors and careful layout techniques are used to minimize the effects of mismatch.

As explained earlier, in order to maintain the ASIC supply current constant, the I_{delta} sources are actually not switched on and off, but redirected towards the heating resistor in the corresponding hot die (being added to I_{base} through the same bonding pad) or towards a sink resistor (through an alternative pad). Complementary switches are used for this purpose. The controlling signals of the complementary switches are overlapped in the on state, to avoid current glitches in the supply.

D. *The DACs*

Three voltage-output DACs, one per group of four loops, are used to set the prescribed temperatures for the hot dies in each group. Their resolution is of 10 bits.

The DACs use a conventional resistive divider and analogue multiplexer topology. The transfer characteristics are monotonic by construction. The reference voltage is obtained from V_{REF}, using a buffer to avoid kick-back transients on the global reference. Taking advantage of the (switched) capacitive input of the comparators, no buffer is

used at the analogue multiplexer output, avoiding offset effects. One single voltage buffer (with one offset value) drives the three resistive strings, which are shorted together every 32 unitary resistors, making the transfer characteristics of the three DACs essentially identical.

VII. The Communication and Control Unit

The digital control block, also called the communication and control FSM, performs the following functions:

- Receives and sends commands and data from the external interface with the instrument control unit (ICU). This is done through an Universal Asynchronous Receiver/Transmitter (UART) at a speed of 19600 bauds.
- Reads and writes configuration and data registers located in different parts of the chip. This includes configuring some programmable analogue circuit blocks, and reading the ADC channel output data.
- Controls the operation of the thermal control loops, its comparators, its heating current sources, and counts the additional heating current delivered to each hot die. It performs these operations according to various operating modes.
- Controls the AD conversion channel, and the sequence of conversion of the 20 channels that are time-multiplexed, according to various operating modes.
- Receives the alert signals from the over-temperature sensors corresponding to the hot-dies and the ASIC itself, and takes the corresponding actions when required.

The operating modes include a *cyclic mode* and an *on-request mode*, meaning that the ADC channel conversions and power measurements from the thermal control loops can take place periodically, or on-request. There are some auxiliary modes, like a test mode specifically devised to help in the characterization of the ADC, and others. The digital control block also interprets and executes the commands, enables and disables different circuit blocks in the ASIC, and receives parity checks from the many registers in the ASIC, reporting to the external ICU in case of errors. This digital block includes a scan-path port for testability purposes. The high-level design has been carried out by CRISA [5].

VIII. Auxiliary Blocks

A. The Band Gap and Voltage Reference

As mentioned earlier, all voltage references in the ASIC are derived from the global voltage reference V_{REF}, using one single resistive string taped at different points.

The global reference V_{REF}, nominally 2.5V, is obtained from a band-gap circuit, whose output is amplified using a feedback amplifier. The gain is defined by a resistor ratio. The global voltage reference is connected to a specific pad, and can be trimmed using four bits from an internal register, in order to cope with the opamp offset and resistor mismatch. Four additional bits can be used to trim the band-gap, in order to reduce the reference voltage variations with temperature.

B. The PTAT

A proportional-to-absolute-temperature (PTAT) current is generated from the band-gap. The voltage generated in a resistor is then used to measure the temperature of the ASIC die. This is one of the signals that is converted by the ADC channel, providing a real-time measurement of the ASIC temperature. This is important for two reasons. One is the possibility of compensating minor effects of temperature on the measurements for which the ASIC has been designed, provided that a previous calibration has been done. The other is to provide a safe-ward against excessive heating of the ASIC, something important due to the large heating currents and the low density atmosphere in Mars.

C. The Current Reference

A current reference circuit is used to obtain a stable current value I_{REF}. It is based on a voltage derived from V_{REF}, and an external resistor connected at a specific bonding pad. A feedback loop controls a current source that drives the resistor, until the resistor voltage is equal to the derived voltage (1.0V). The external resistor should have a temperature coefficient as low as possible. Values of 25 ppm/ºC are expected in the final flying modules. For the characterization of the ASIC, external resistors with 0.1ppm/ºC are being used.

Note that, neglecting the variation of the external resistor with temperature, it turns out that the reference current will change with temperature, and with ASIC sample, in the same way than the reference voltage V_{REF}. The offset of the amplifier in the feedback loop, which has been specifically optimized, has some effect but is negligible as compared to V_{REF} inter-samples variations. This V_{REF}-I_{REF} deviations correlation has relevant implications in measuring resistance values by means of measuring the voltage on a current biased resistor: because the reference voltage of the ADC and the biasing current (and therefore the resistor voltage) change in the same way, there is no effect on the resulting measurement.

Still, voltage and current stability with temperature are primary goals, because they do have an effect on other measurements, specially in the delivered current to the hot dies -with a squared effect on power-, as well as other voltage magnitudes not related to resistor measurements.

D. High-Temp Alarms & Auto Shut Down.

The ASIC contains some over-temperature protective functions, for it-self and for the hot-dies. The hot dies temperatures can be observed from their voltages V_x. These are compared to a reference, maximum voltage, representative of their maximum allowed temperature. Simple continuous-time, inaccurate comparators are used for this purpose, since accuracy is not too relevant in this function. The output of the four comparators associated to the four dies in each group is "ORed", and the result for each group is sent to the digital control block. If any die is over heated, the heating currents (I_{base} and I_{delta}) of that group are disabled. The internal temperature of the ASIC, taken from the output of the PTAT circuit, is also compared to a (different) voltage that

represents the maximum allowed temperature for the ASIC die, and sent to the digital control block. All heating currents are disabled in the event of an ASIC over-temperature.

E. Power-on Reset

A power-on-reset circuit is included to generate a reset event shortly after the power up. A specific pin performs the double function of allowing an external reset, and the evaluation of the internal power-up reset pulse. The ASIC can also be reset by software, using a reset command.

F. Measurement of the Power Supply Voltage

A resistive divider is used to down-scale the power supply voltage, placing it within the conversion channel input range. This is level is also multiplexed to the ADC channel, providing a real-time measurement of the power supply voltage. The purpose is to detect eventual improper power supply levels, and to allow the eventual calibration of power supply variations effects on the measurement function.

G. RS-422 Receivers and Transmitter

As mentioned earlier, RS-422 differential signals are used in the communications between the ASIC and the ICU. The ASIC receives two signals from the ICU: a 2.4MHz clock, and the incoming R_x data, at 19600 bauds. The ASIC in turn sends the outgoing T_x data to the ICU, at the same baud-rate. The receiver circuit is the same for R_x and clock, despite the different frequencies, for simplicity. Conventional circuit approaches are used for this function. The transmitter is designed to operate with self-limited slew rate, in order to reduce electromagnetic emissions from the transmission lines connecting the ASIC and the ICU.

H. Reference levels for ADC calibration

Six differential voltage signals with the proper common mode, which represent the 10, 50, and 90 percent levels of the (one side, positive or negative) input signal range of the ADC channel, for the gain 1 and the gain 150 configurations, are obtained from V_{REF} using a resistive divider. The same reference signals are used for both sides (positive and negative) of the input signal range by swapping the connections to the preamplifier input.

These signals can be observed and measured through the global nodes used for testing and observation of a large number of analogue and digital signals. This is important for precise calibration due to resistors mismatch, which limits the accuracy of these reference signals.

IX. RHBD and Low Temperature Measures

Concerning Radiation Hardening by Design (RHBD) measures, the design uses well known techniques, available in the literature, and builds on previous work by the authors in the characterization of radiation and low temperature effects on this specific CMOS technology [7],[8].

The analogue circuitry is full-custom, and uses enclosed-layout transistors (ELTs) for the nmos, and regular layout for pmos. Minimum length transistors are uncommon in analogue circuitry, and are avoided in general. These measures are aimed to increase the circuitry robustness against ionizing radiation. Although the specification of a maximum TID of 9Krad is quite low, and these techniques could probably be skipped, it was decided to use the procedures developed in previous RHBD mixed-signal ASICs [9],[11] to allow the eventual use of the ASIC in other environments.

Guard-rings are used around nmos and pmos devices, with the purpose of reducing the probability and the severity of single-event effects (SEEs) in the analogue circuitry. The type of converter used, the size of the capacitors employed in the sensitive signal nodes and switched-capacitor comparators, and other measures, makes it unlikely that a single particle impact could produce a single-event transient (SET) that could originate a severe degradation of the performance. Still, the role of the ASIC, being part of an atmospheric data measurement system, allows sporadic wrong behaviour without catastrophic effects. The situation is different concerning single-event latch-up (SEL). A latch-up event could potentially destroy the device, with permanent effects on the instruments. However, similar mixed-signal ASICs designed and tested using the same procedures in the same technology have been shown to be latch-up free up to at least 80 MeV·cm^2/mg. The same result is expected for this design.

The digital sections of the ASIC are semi-custom, and employ a library of RHBD digital cells developed in the past years by the authors. The RHBD techniques used in the digital cells are the same described above for the analogue circuitry. Several previous ASICs and test vehicles have shown more than sufficient TID tolerance, and latch-up free behaviour also up to at least 80 MeV·cm^2/mg. Regarding eventual single-event upsets, all registers in the ASIC include an additional bit for parity-check. Parity errors are reported to the digital control unit, which in turn reports this events to the ICU as part of an ASIC-status word.

With respect to temperature, the ASIC is specified to operate within -128 ºC to 50 ºC, ambient temperature. Concerning the electrical simulations used along the design and verification process, it must be noted that the foundry provided models are not qualified below -55ºC. The authors have measured transistors I-V characteristics down to -110ºC and verified that the transistor models can be used with reasonable accuracy down to this limit. Also, the actual temperature operation range of the die will be quite above the ambient-temperature operation range, due to self heating. This is specially true considering the low density of the Mars atmosphere, and therefore, the high temperature coefficients that can be expected from the ceramic package.

Specific radiation (TID & SEE) and low temperature tests in a "Mars Chamber", are planned for the coming months.

X. Experimental results

The ASIC has been tested from a functional perspective, at room temperature. Some specific magnitudes have also been measured in temperature down to -20ºC. Measurements further down are planned for the coming weeks. The following paragraphs describe present test results and measured performance.

A. Communication and Control functions

The ASIC is being tested using a specific test system based on a Raspberry Pi-2. The communication functions have been tested and are operative. Command executions, data transferences, and register configuration functions are also operative. In summary, the digital control block and the RS-422 receivers and transmitter are operating without problem. The transmitter output signals are slew-rate limited as required. The POR circuit is also operating within specs.

B. The ADC channel

The ADC channel has been functionally verified on a reduced number of samples. However, performance figures requiring measurements of a significant number of ASIC samples are still underway. Gain and offset values are correct. More detailed measurements are still required to separate noise from static characteristics, but preliminary results show that the Integral Non Linearity (INL) is within ±1 V_{LSB}, and r.m.s noise is also within specs, in the range of 1 V_{LSB}. The converter is inherently monotonic. Measurements show the same transfer characteristic for all 9 external channels, demonstrating that the multiplexer has no effect, as expected from the capacitive input impedance of the preamplifier. The bias current and reference voltages used to bias the external resistors have their expected values.

C. Thermal Control loops

The behaviour and stability of the thermal control loops has been verified using hot-die samples provided by UPC. In addition, the specific accuracy of the involved circuit blocks has been preliminarily evaluated, as required to asses their effects on the delivered power measurements.

The clocked comparators, with their auto-zero function, have an offset value below 0.1mV. The I_x bias currents have a dispersion below ±0.3%, and the heating currents below ±0.5%. These are measurements taken over the 12 units available in each ASIC. Concerning the DACs, which are monotonic by construction, their INL is below ±1 V_{LSB}.

D. Miscellaneous functions

The band gap, voltage reference, and current reference circuits are operating correctly. The observable nodes are the V_{REF} and I_{REF} nodes. The results are within specs. The average (over 12 ASIC samples) value of V_{REF} is 2.488V (nominally, 2.5). The standard deviation is 0.5%. Note that this includes the variations of the band-gap and those related to the amplifier, including the opamp offset. The nominal voltage at I_{REF}, where the external low-temperature-coefficient resistor is connected, is 1V. Average and standard deviation values are 0.9955V and again 0.5%. Further more, there is a very high correlation between the deviations of V_{REF} and those of the voltage at I_{REF}, meaning that resistors matching is quite good (non dominant) and that the feedback loop used to generate a current proportional to V_{REF} and inversely proportional to the external resistor is working properly. The maximum variations of V_{REF} with temperatures, between -20 and 100ºC, is below ±5mV (w.r.t. its central value). The equivalent variation at the band-gap output, assumed to be 1.2V, is 2.5mV approximately. In either case, equivalent to a ±0.2%.

The PTAT used to measure the ASIC die temperature is working properly. Accuracy figures are still to be determined, but are not too relevant since the main purpose of this function is to allow a correspondence between ASIC temperature and eventual correction/calibration factors, the precise value of temperature being somewhat irrelevant. The down-scaled version of the power supply voltage is also correct, with deviations in the range of resistors matching (~0.1%), again irrelevant. Finally, the temperature alarms (and corrective actions from the digital control unit) for the external hot-dies and ASIC die are also operative. Again, accuracy is not relevant because thresholds are usually set with enough tolerance. The analog and digital multiplexers used to observe internal signals are also operative.

XI. Summary

A rad-hard, mixed-signal ASIC in a standard 0.35 µm CMOS technology has been designed. It is an analogue front-end for the MEDA wind sensor for NASA's Mars2020 mission. The ASIC has been fabricated and tested. Some additional detailed measurements are underway. Radiation tests are planned for the coming months. They are expected to be satisfactory based on previous ASICs designed in the same technology using the same RHBD techniques and the same rad-hard digital library.

References

[1] http://mars.nasa.gov/mars2020/mission/science/for-scientists/instruments/meda/

[2] https://www.cab.inta-csic.es

[3] M. Domínguez, V. Jiménez, J. Ricart, L. Kowalski, J. Torres, S. Navarro, J. Romeral, and L. Castañer, “A hot film anemometer for the martian atmosphere,” Planetary and Space Science, vol. 56, pp. 1169 – 1179, June 2008

[4] L. Kowalski, J. Ricart, V. Jiménez, M. Domínguez, and L. Castañer, “Thermal modelling of the chip for the REMS wind sensor,” International Journal of Numerical Modelling: Electronic Networks, Devices and Fields, vol. 23, pp. 340–353, July - October 2009.

[5] http://www.crisa.es/

[6] http://ams.com/eng

[7] J. Ramos-Martos et al. “Evaluation of the AMS 0.35 µm CMOS Technology for Use in Space Applications”, Proceedings of the Analog and Mixed-Signal Integrated Circuits for Space Applications (AMICSA 2012), August 2012.

[8] J. Ramos et al. “SEE Characterization of the AMS 0.35 µm CMOS Technology”, Proceedings of the Conference on Radiation Effects on Components and Systems (RADECS 2013), September 2013.

[9] J. Ramos-Martos et al. “OWLS: A Mixed-Signal ASIC for Optical Wire-Less Links in Space Instruments”, Proceedings of the Analog and Mixed-Signal Integrated Circuits for Space Applications (AMICSA 2012), August 2012.

[10] S. Sordo-Ibáñez et al. "A Front-End ASIC for a 3-D Magnetometer for Space Applications Using Anisotropic Magnetoresistors". IEEE Transactions on Magnetics, Volume: 51 Nº: 1 January 2015

[11] S. Sordo-Ibáñez et al. “A Rad-Hard Multichannel Front-End Readout ASIC for Space Applications”, Proceedings of the 1st IEEE Workshop on Metrology for AeroSpace, May 2014.

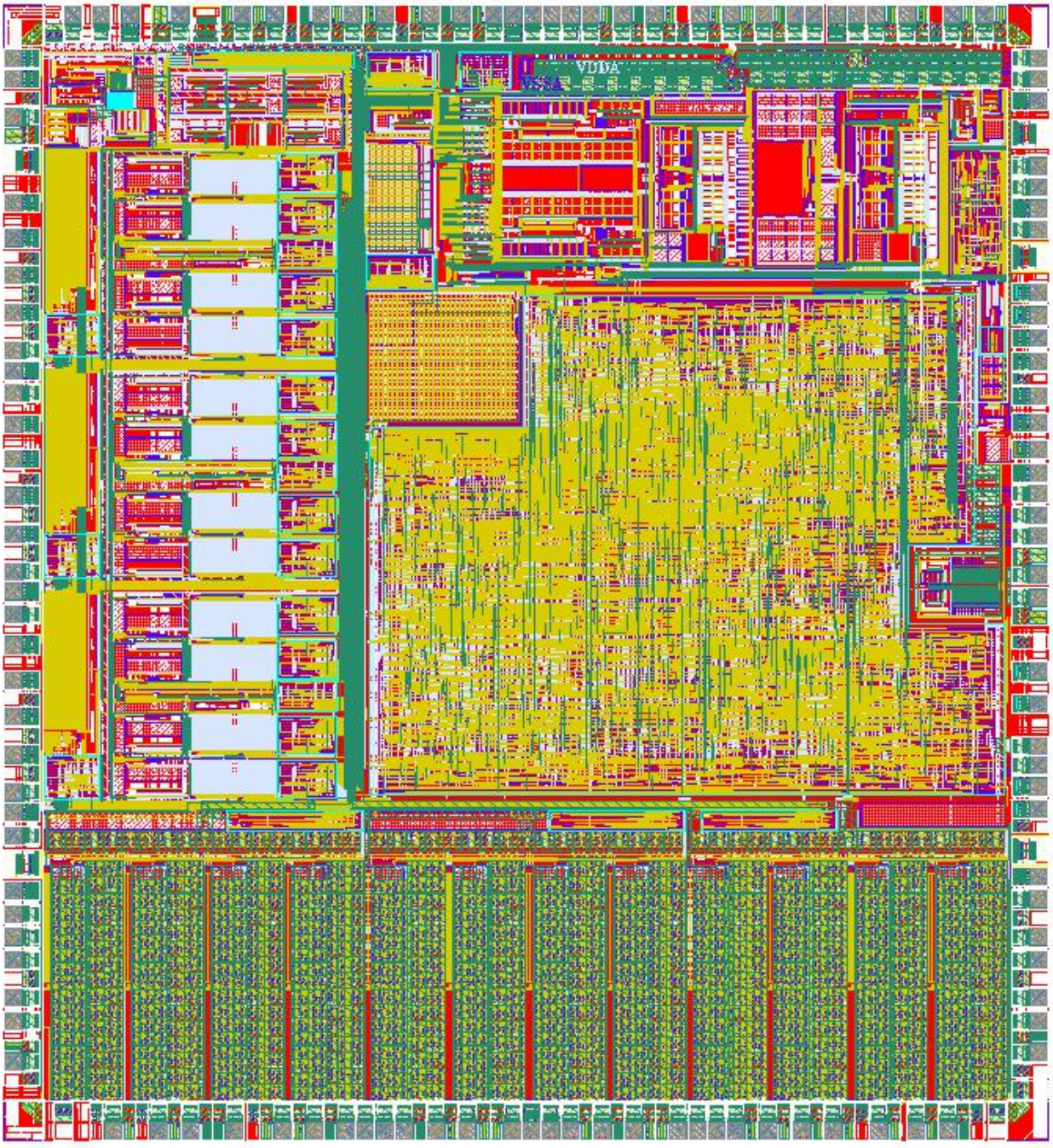


Figure 1: MEDA WS FE ASIC Layout. Dimensions are 5 x 5 mm.

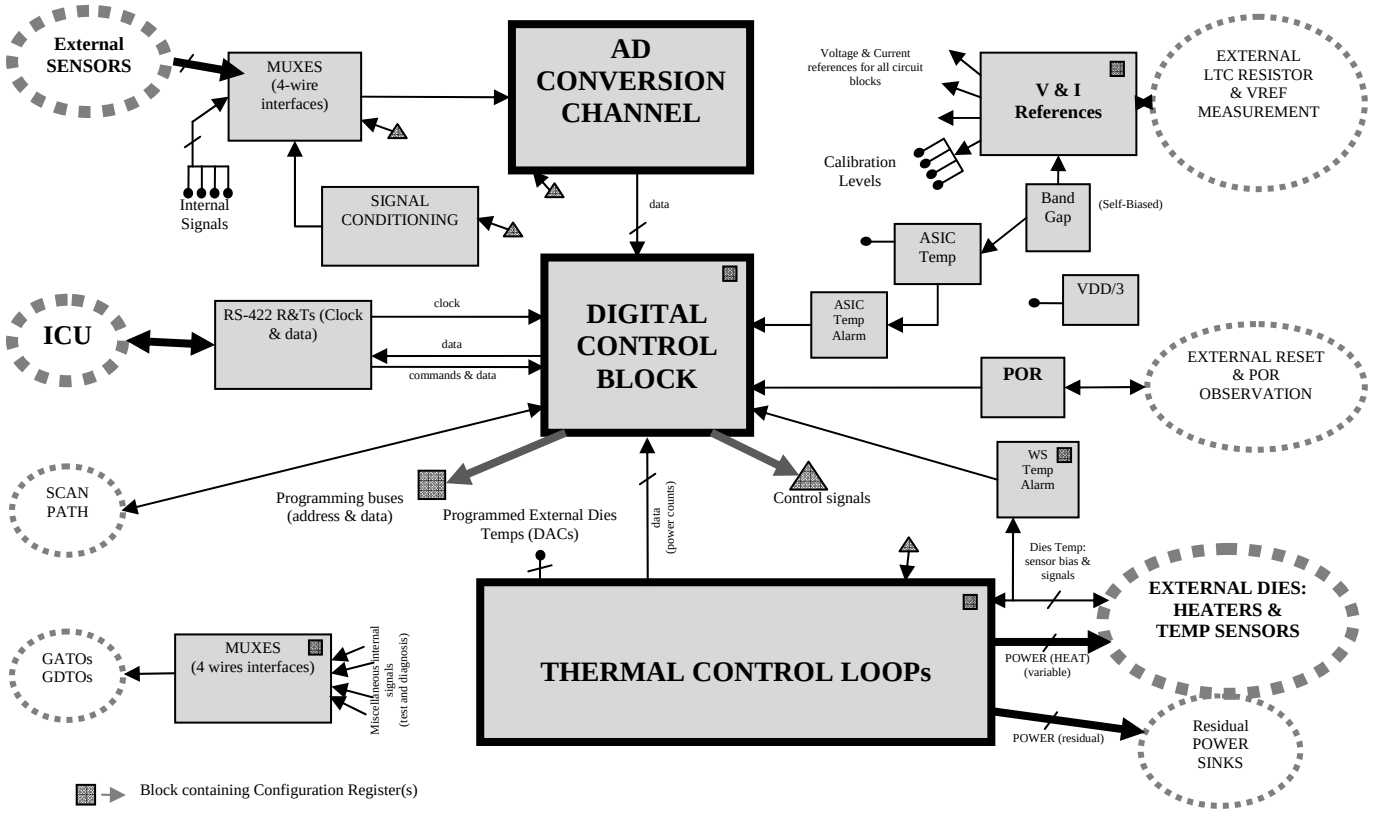


Figure 2: Simplified Block Diagram of the MEDA Wind Sensor Front-End ASIC.

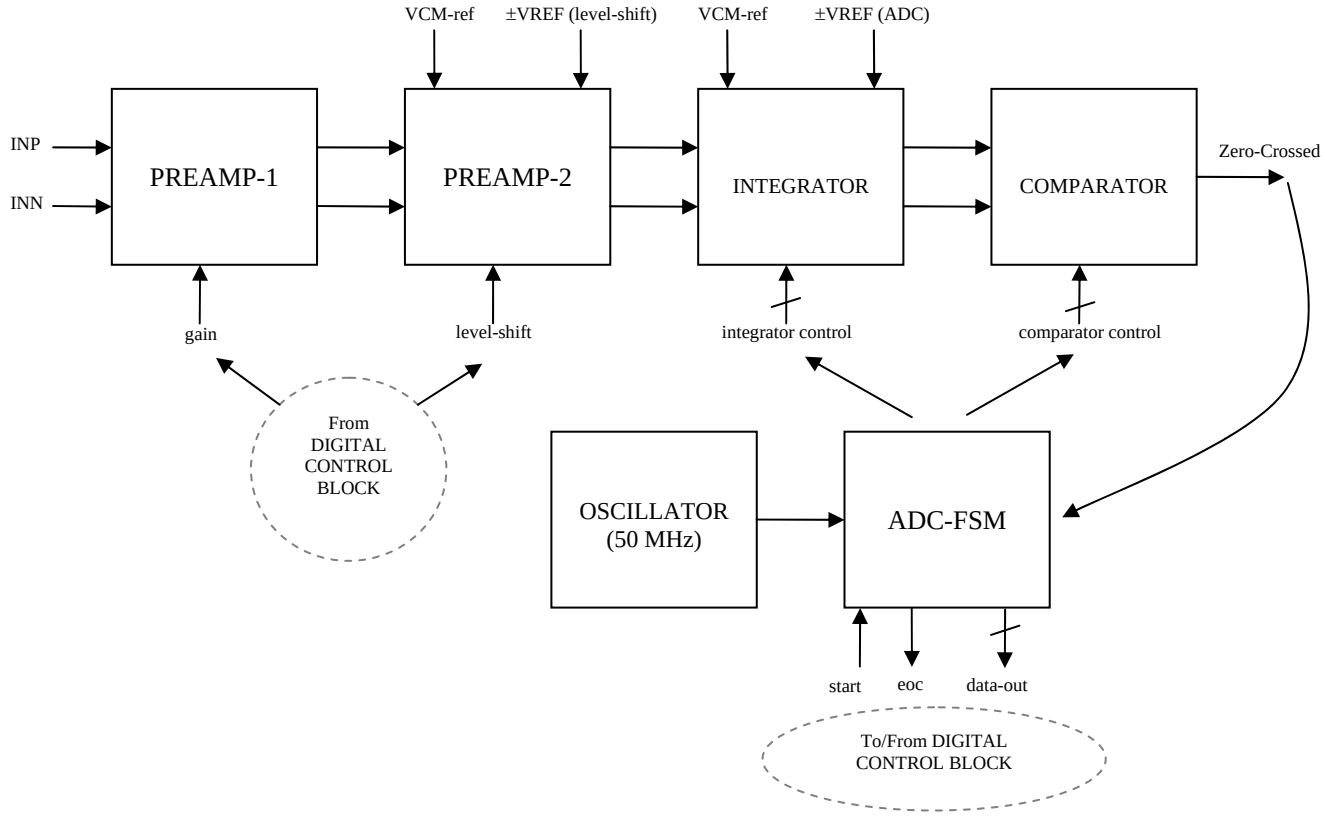


Figure 3: Block Diagram of the ADC conversion channel. Input multiplexer and bias currents are not shown.

25-Gb/s/Channel VCSEL Driver and Transimpedance Amplifier Array ICs in 0.25-µm SiGe:C BiCMOS Technology for Space Applications

M. Ko[a], K. Tittelbach-Helmrich[a], V. Petrovic[a], and D. Kissinger[a,b]

[a]IHP GmbH, 15236 Frankfurt (Oder), Germany
[b]TU Berlin, 10623 Berlin, Germany

ko@ihp-microelectronics.com

Abstract

We present monolithic VCESL driver and TIA ICs for multi-channel optical transceivers for space. The ICs provide 3 independent channels and are targeted to operate at the highest data rate of 25 Gb/s/channel and the lowest total power consumption of 5 mW/Gb/s. The driver for common-cathode VCSEL arrays consists of pre-driver, buffer, and output stage. The TIA IC consists of transimpedance input stage, gain stage, output buffer, and DC-cancellation loop. Each IC provides a standard SPI serial interface for advanced digital controllability. The radiation hardness is achieved by triple modular redundancy flip-flop design. Two generations of the ICs have been implemented with IHP's 0.25-µm SiGe:C BiCMOS technology. The Gen-1 ICs with simple analog control circuits have been electrically characterized by on-wafer measurements and successfully demonstrated with eye-diagram measurements up to 25 Gb/s for the TIA and even up to 40 Gb/s for the driver. The Gen-2 ICs equipped with full digital control circuits including SPI are under fabrication. They are expected to have very low power consumption of 1.8 and 2.6 mW/Gb/s for the driver and the TIA, respectively.

I. Introduction

As the demand for broadband communication has been explosively increasing, next-generation telecom satellites are needed to offer very high data rate connections, bringing massive digital data transfers between boards, modules, and equipment in a satellite. 850-nm optical interconnects based on vertical cavity surface emitting laser (VCSEL), photodiode (PD), and multimode fiber are the most attractive solutions for future intra-satellite networks as they can provide high-bandwidth, low-power, small-size and lightweight connections at a low cost [1]. In such a system, electronic ICs providing higher bandwidth and lower power consumption per data rate are very critical since at a given aggregated throughput these parameters determine the number of required parallel links and the overall power consumption.

In this work we present monolithic VCESL driver and transimpedance amplifier (TIA) ICs for multi-channel optical transceivers for space. The ICs provide three independent channels and are targeted to operate at the highest data rate of 25 Gb/s/channel and the lowest total power consumption of 5 mW/Gb/s. The ICs are equipped with a standard serial peripheral interface (SPI) for advanced digital controllability.

The paper is organized as follows: in Section II the circuit design methodology is described. Section II-A and II-B present the VCSEL driver and the TIA, respectively. Section II-C presents the digital control part. In Section III, high-speed characterization results of the driver and the TIA are reported. Finally Section IV concludes the paper.

II. Circuit Design

The 3-channel 25-Gb/s VCSEL driver and TIA ICs have been developed with the two-generation approach. The first generation (Gen-1) ICs focus on verification of high-speed signal path so they contain only analog control circuits for simple operation adjustment. And the Gen-2 ICs include advanced control functions with SPI. The ICs are realized with IHP's 0.25-µm SiGe:C BiCMOS technology.

A. VCSEL Driver

The VCSEL driver is designed to directly modulate high-speed common-cathode VCSEL arrays.

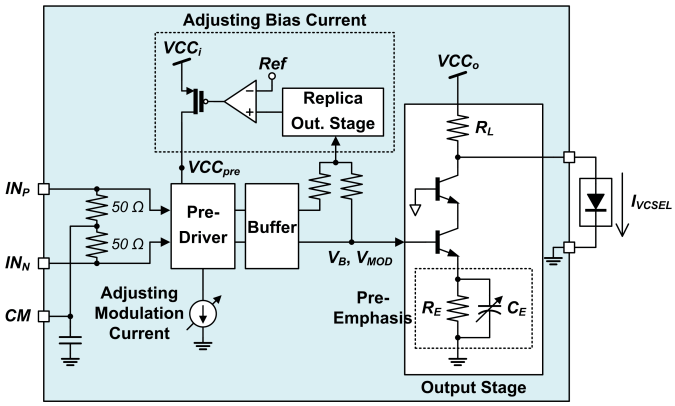


Figure 1: Schematic of VCSEL driver core.

The schematic of the single-channel driver core is shown in Figure 1. It consists of pre-driver, buffer, output stage with RC pre-emphasis, and feedback replica bias and control circuits. Differential input signals from digital modules come into the pre-driver with differential 100-Ω termination for input matching. VCSEL driving currents generated from the output stage are applied into the VCSEL anode. A ground for the VCSEL common cathode is provided from the driver.

The output stage is the most critical building block in low-power design because it consumes most of the total power dissipation in order to drive a large amount of currents to the VCSEL. In our driver a single-ended structure is used for output stage so that it can reduce power dissipation by up to 50% comparing to conventional differential structures.

On the other hand, the single-ended output stage is so sensitive to input voltage level that it's difficult to control the driving currents accurately. This sensitive biasing of the output stage is solved by using replica output stage and feedback loop. The exact amount of currents flowing through the output stage is read from the replica output stage and this information is compared with a reference signal representing the desired current level, and fed back.

A capacitive emitter degeneration technique is used for pre-emphasis. It improves the speed of the driver itself, and

moreover it can compensate speed reduction of the optical link, mainly from VCSELs and PDs. The pre-emphasis level can be optimized by adjusting a variable capacitor (C_E) with its control voltage.

The pre-driver and the buffer are biased with on-chip proportional to absolute temperature (PTAT) current sources and this enables bias and modulation currents to the VCSEL to be temperature-independent. The VCSEL bias current can be adjusted by changing the reference voltage (*Ref*) and the output stage supply voltage (VCC_o). The VCSEL modulation current also can be adjusted by changing the PTAT bias current of the pre-driver. The bias and modulation currents have the typical values of 3 mA and 3 mA_{pp} and can go higher up to 5 mA and 5 mA_{pp}, in order to prepare VCSEL performance degradation with time and temperature.

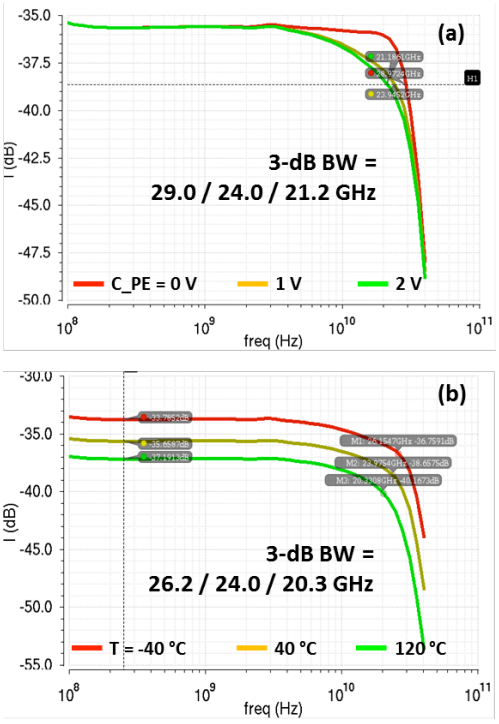


Figure 2: Post-layout simulated frequency responses of VCSEL driver at different (a) pre-emphasis levels and (b) operating temperatures.

Figure 2 and 3 show post-layout simulation results of the designed driver core. Figure 2 shows the frequency responses which are from the differential input voltage to the VCSEL output current (I_{VCSEL}). The responses at different pre-emphasis levels show that the bandwidth can be extended from 21.2 GHz up to 29.0 GHz which is very promising for faster data transmission than 25 Gb/s. Also, as shown in Figure 2 (b), the driver is designed to cover a wide temperature range from –40 °C to +120 °C. . At the nominal temperature of 40 °C, the 3-dB bandwidth is 24.0 GHz. The bandwidth is degraded as the temperature increases, and it goes down to 20.3 GHz at the highest temperature of 120 °C, which is still enough for 25-Gb/s operation.

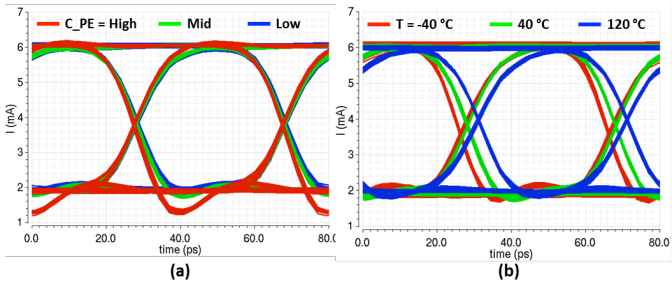


Figure 3: Post-layout simulated eye diagrams of VCSEL driver at different (a) pre-emphasis levels and (b) operating temperatures.

Figure 3 shows post-layout simulated eye diagrams at the data rate of 25 Gb/s and VCSEL bias/modulation currents of 4/4 mA. Figure 3 (a) shows the effect of controlling the pre-emphasis level. At stronger pre-emphasis the rise/fall time is enhanced and the pre-emphasis peak is occurred which can be used for compensating further band-limited optical link characteristics. The diagrams at different temperatures show that the PTAT current sources are well optimized since the DC level (bias current) and the swing (modulation current) do not change within the wide temperature range. Degradation of rise/fall time at high temperature due to the decreased bandwidth can be overcome by optimizing the pre-emphasis level.

B. Transimpedance Amplifier

The TIA converts small input currents from high-speed common-cathode PD arrays into differential voltage output.

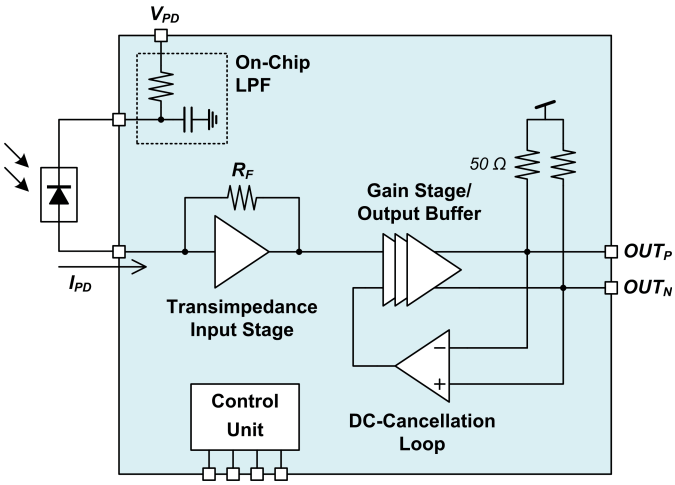


Figure 4: Schematic of TIA core.

Figure 4 shows the schematic of the TIA core [2]. It consists of transimpedance input stage, gain stage including output buffer, DC-cancellation loop, and bias and control circuits. The PD anode is connected to the TIA input pin, and differential output signals from TIA are applied to off-chip devices with differential 100-Ω termination for output matching. The PD cathode bias voltage is not generated by the IC but provided externally (V_{PD}) because it is higher than the circuit supply voltage. It is fed to the PD cathode via on-chip RC low-pass filter which has a cut-off frequency of around 100 MHz. The photo-generated current from the PD is converted to voltage by the input stage, and amplified to a sufficient voltage swing for the next stage. The output buffer enables to drive external differential 100-Ω load. Because the input stage is single-ended, the DC offset can be occurred at differential TIA output. A DC-cancellation feedback loop is

employed to eliminate the offset. In order to give freedom to performance optimization, the IC has a diversity of adjustability, which are gain, output swing, jitter, and zero crossing point controls.

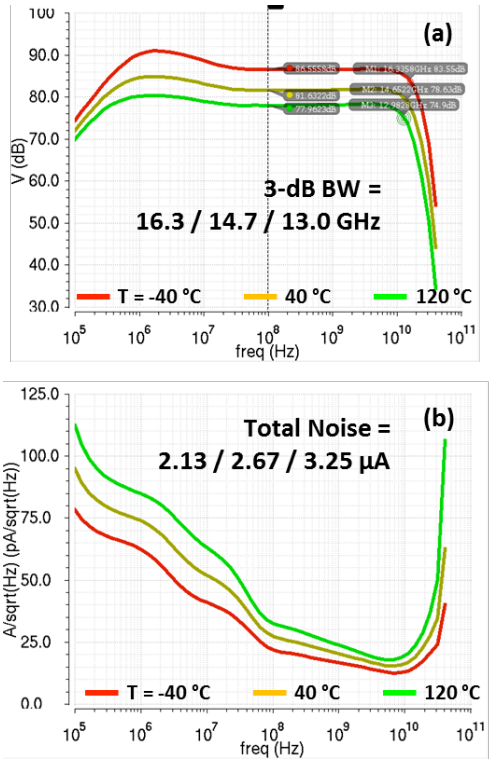


Figure 5: Post-layout simulated (a) transimpedance gain and (b) input-referred noise current density responses of TIA at different operating temperatures.

Figure 5 (a) shows the simulated transimpedance gain responses of TIA at different temperatures and process corners. At the nominal temperature of 40 °C, the TIA gain is about 81.6 dB (or 12.0 kΩ) and the 3-dB bandwidth is 14.7 GHz which is adequate to 25-Gb/s transmission. As the temperature changes, the gain and the bandwidth varies from 78.0 to 86.6 dB and from 13.0 to 16.3 GHz, respectively. Decreased bandwidth can be overcome by pre-emphasis at the transmitter.

The input-referred noise current density responses at different temperatures are shown in Figure 5 (b). Total input noise current integrated up to 20 GHz is about 2.67 µA at the nominal temperature and varies from 2.13 to 3.25 µA as the temperature changes.

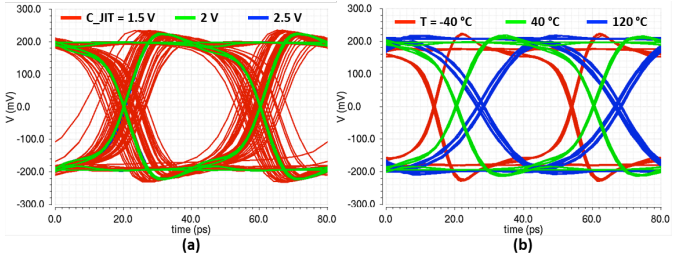


Figure 6: Post-layout simulated eye diagrams of VCSEL driver at different (a) jitter optimizations and (b) operating temperatures.

Figure 6 shows the eye diagrams at the data rate of 25 Gb/s and the input PD current of 100 μA_{pp}. The eye diagrams when adjusting the jitter optimization control voltages (C_JIT) show that jitter performance is optimized at 2 V, comparing to the eye diagram at 1.5 V which shows large deterministic jitter. The effect of different operating temperatures can be seen in Figure 6 (b). Degradation in jitter and rise/fall time at the high temperature is not significant and can be improved by optimizing bias voltages.

C. *Digital Control*

The Gen-2 ICs are equipped with a digital serial interface in order to enable advanced digital control functions such as channel on/off function, various digital controls, and diagnostic/status information.

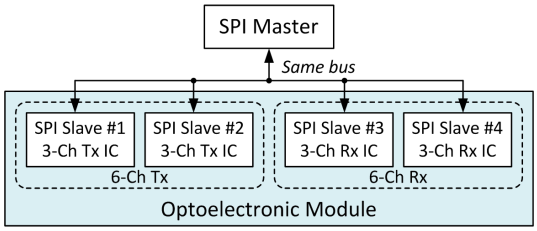


Figure 7: Serial communication interface configuration for 6-channel optoelectronic module.

Figure 7 shows the serial communication interface configuration for the optoelectronic module using SPI standard. Since the 6-channel transceiver module consists of two 3-channel driver (Tx) ICs and two 3-channel TIA (Rx) ICs, All 4 ICs should be connected to the same bus but controlled independently. Also, it should support autonomous start-up operation with pre-defined initial control values when the master controller is not connected.

The block diagram of the SPI slave is shown in Figure 8. The SPI block has basic SPI bus pins (SCLK, CS, MOSI, MISO) and a reset (RST) pin equipped with automatic power-on reset circuit. 2-bit address Addr<0,1> is used to indicate the chip ID necessary since identical SPI slaves are used for all 4 chips (Tx/Rx #1/2). It has 7/1 write/read registers (8 bits each) and the preset values for the write registers can be set by connecting each init pin with logic high or low. Supply voltage for I/O is downscaled from 3.3 V to 2.5 V to enhance single-event latch-up tolerance and reliability. In overall digital circuit design, triple modular redundancy flip-flops are used to enhance the radiation hardness.

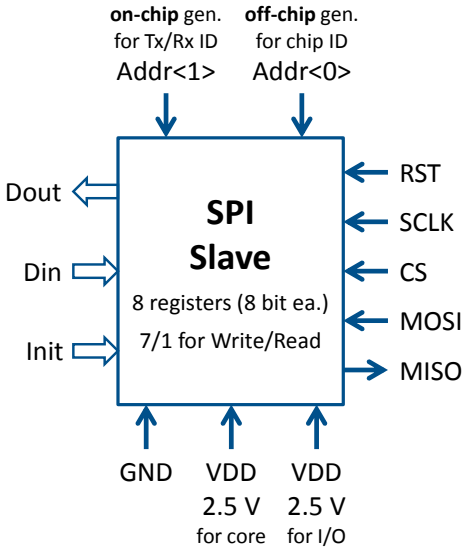


Figure 8: Block diagram of SPI.

Control parameters of Tx and Rx using digital SPI are summarized in Table 1.

Table 1: Control parameters of Tx and Rx.

Tx/Rx	Control	# Bit per Channel	Note
Common	Channel ON/OFF	1	
Tx	VCSEL bias current	4	0 – 5 mA
	VCSEL mod. current	4	0 – 5 mA_{pp}
	Pre-emphasis	3	
Rx	Jitter	4	
	Gain	4	4 to 13 kΩ
	Output amplitude	4	0 to 750 mV_{ppd}

III. Measurement Results

The Gen-1 3-channel 25-Gb/s VCSEL driver and TIA ICs have been fabricated with IHP's 0.25-µm SiGe:C BiCMOS technology. The chip photos of each IC are shown in Figure 9. They have three identical circuit cores and occupy the dimensions of 0.74 mm × 1.34 mm (driver) and 1.04 mm × 1.54 mm (TIA). The area for TIA is bigger than that of the driver because the gain stage/output buffer chain occupies quite much area.

Their performances have been characterized with on-wafer electrical measurements with 50-Ω equipment instead of a real VCSEL/PD array. Figure 10 shows the measured eye diagrams of the VCSEL driver at different cases. The eye diagrams at different data rates show that the driver operates well at lower data rates of 6.25 Gb/s for low bit rate option and even up to 40 Gb/s. The eye diagrams at different channels show good inter-channel uniformity.

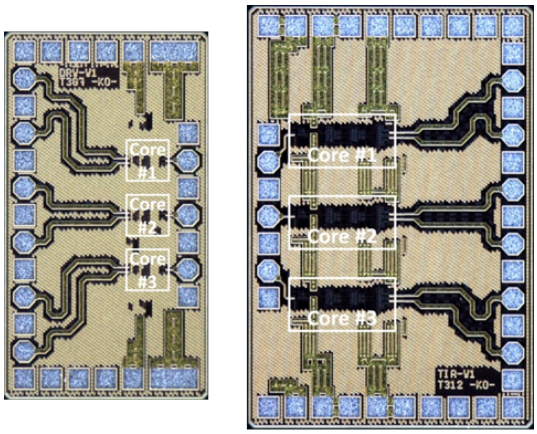


Figure 9: Chip photos of Gen-1 VCSEL driver and TIA.

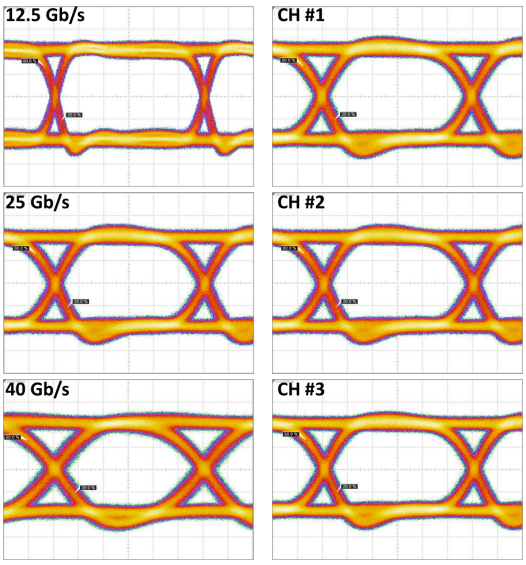


Figure 10: Measured eye diagrams of Gen-1 VCSEL driver.

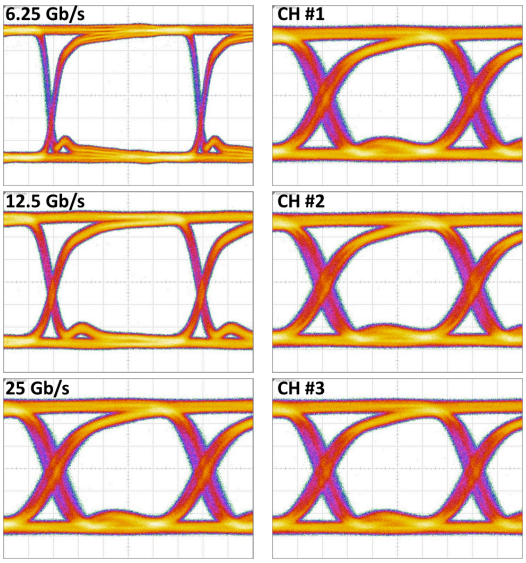


Figure 11: Measured eye diagrams of Gen-1 TIA.

Figure 11 shows the measured eye diagrams of the TIA at different cases. The eye diagrams at different data rates show that the TIA operates well from 6.25 to 25 Gb/s with clear open eyes. Also they show good uniformity among three channels. Figure 12 shows the output noise voltage and its histogram at the single-ended output measured by using an oscilloscope with channel bandwidth of 50 GHz. The input probe was detached from the chip to measure noise components only generated by the TIA. The measured rms value is about 3.5 mV and this is matched to the simulation result of 4.65 mV if considering the cable loss of about 2 dB from the measurement setup.

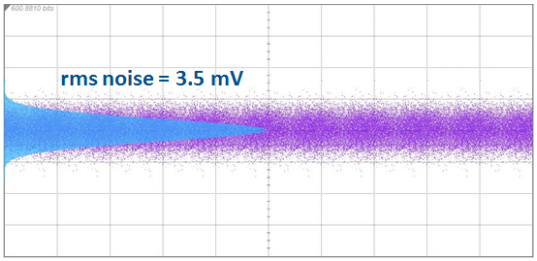


Figure 12: Measured output noise voltage of Gen-1 TIA.

IV. Conclusion

Monolithic SiGe BiCMOS VCESL driver and TIA ICs for multi-channel optical transceivers for space have been reported. The Gen-1 ICs have been electrically characterized up to 25 Gb/s for the TIA and even up to 40 Gb/s for the driver. The Gen-2 ICs with digital controls are under fabrication and rad-hard testing for Gen-2 ICs is under contemplation.

V. Acknowledgements

The research leading to these results has received funding from the European Union Seventh Framework Programme for research, technological development and demonstration under the Grant number 607274 (Multi-Gigabit, Scalable & Energy Efficient On-Board Digital Processors Employing Multi-Core, Vertical, Embedded Opto-Electronic Engines). The authors would like to thank the colleagues who have contributed the work.

VI. References

[1] L. Stampoulidis, E. Kehayas, M. Karppinen, A. Tanskanen, V. Heikkinen, P. Westbergh, J. Gustavsson, A. Larsson, L. Grüner-Nielsen, M. Sotom, N. Venet, M. Ko, D. Micusik, D. Kissinger, A. C. Ulusoy, R. King, R. Safaisini. (2014, Octorber). The European Project "MERLIN" on Multi-Gigabit, Energy-Efficient, Ruggedized Lightwave Engines for Advanced on-Board Digital Processors. Presented at International Conference on Space Optics (ICSO).

[2] Behnam Sedighi and J. Christoph Scheytt. (2012, August). Low-Power SiGe BiCMOS Transimpedance Amplifier for 25-GBaud Optical Links. IEEE Transactions on Circuits and Systems II: Express Briefs. 59 (8), 461-465.

First S-Band Capable Dual 12-bit 1.5 GSps ADC in Flip-Chip Hermetic Technology

N. Chantier[a] , E. Savasta[a], R. Pilard[a], M. Stackler[a], G. Wagner[a] , C. Lambert[a], O. Boillon[a], J-P. Amblard[a], E. Bajat[a], F. Malou[b]

[a]e2v Semiconductors, 4 rue de Rochepleine, 38120 Saint-Egrève, France
[b]Centre National d'Etudes Spatiales (CNES), 18 avenue Edouard Belin, 31400 Toulouse, France

eric.savasta@e2v.com, romain.pilard@e2v.com, nicolas.chantier@e2v.com

Abstract

In partnership with CNES, a new ADC has been developped to meet the high dynamic range as well as channel integration requirements of telecommunications payloads.

It is a dual channel single core 12bit 1.5GSPS designed by e2v on ST Microelectronics BiCMOS9 technology which features 0.13µm CMOS and SiGeC NPN HBT bipolar technology (Ft/Fmax = 166/175GHz).

The device is built in a hermetic flip-chip package using Aluminum Nitride material in order to reach optimized thermal performance and higher pin density.

A new European Flip-Chip assembly line is being used for this device.

I. Context

The challenge of telecommunication payload manufacturers is to respond to the demand of telecom operators in terms of flexibility and performance. Those requirements are reached thanks to Digital Transparent Processors (DTP) architecture whose performance is highly dependent on analogue-to-digital (ADC) and digital-to-analogue (DAC) converter performance.

Furthermore, in order to enlarge product acceptance and profitability, e2v is looking for synergy with adjacent markets such as Defence and Industrial ones. e2v ambitions to be the leader in Europe and world-wide in developing and manufacturing such converters, giving Europe a strategic independence for such key components.

This drives the context of developing a new ADC able to meet high dynamic range and high bandwidth as well as channel integration requirements of telecommunication payloads and defence applications, in partnership with the French Space Agency (CNES) [1] and French Department of Defence (DGA). It is a dual channel single core 12-bit 1.5 GSps ADC based on ST Microelectronics BiCMOS9 technology featuring 0.13 µm CMOS and SiGeC NPN HBT bipolar technology (Ft/Fmax = 166/175 GHz) [2].

II. Market Needs

This new device targets primarily telecommunications payloads and earth observation synthetic aperture radar (SAR) payloads such as the Sentinel-1 series and similar programmes.

Future generations of telecommunications payloads aim to make intensive use of antenna array techniques for more flexibility through dynamic beam control (dynamic beam focus, power adjustments, TDMA beam hoping) [4], [5], [6]. This ADC has been designed with features such as chained synchronization to further extend the electronically steerable antenna array capabilities using software beam control.

SAR payloads such as Sentinel-1 operating in C-band ([7], [8]) can take advantage of this ADC input bandwidth for direct digitization of the SAR signals without the use of frequency down-conversion.

III. Product Overview

The device is built on two kinds of packages using flip-chip assembly for higher pin density and better RF performance.

EV12AD550A is a dual 12 bit 1.5GSps ADC featuring low latency LVDS parallel output with a built in selectable 1:2 or 1:1 DEMUX to compromise between power consumption and ease of interfacing. It is built into a hermetic package realized in Aluminum Nitride (AlN) material in order to reach optimized thermal performance and comply with ESCC9000 quality grade level.

EV12AD500A is a dual 12 bit 1.5GS/s ADC featuring selectable serial output on 4 (or 2) lanes per ADC core, with a data rate at twice the master clock rate, or a selectable parallel output LVDS in 1:1 mode. It is built in a non-hermetic ceramic package realized in High Temperature Coefficient of Expansion (HiTCE) by Kyocera [3]

The two channels can operate in phase or in opposition, thus allowing synchronous or interleaved sampling. Each channel is composed of a single core ADC sampling at up to 1.5GSps. Based on an innovative architecture without interleaving, it provides high spectral purity. It offers an analog input bandwidth of up to 4.3GHz with 2 selectable configurations to optimize SNR performance when working in lower Nyquist zones or linearity performance in higher Nyquist zones. It also features a novel synchronization method to ease the synchronization of a large number of ADCs. The device is controlled through an SPI interface. All sensitive areas of the device have been triplicated to increase

robustness. This includes, but is not limited to, clock circuitry and SPI registers.

Both the EV12AD550A and EV12AD500A are based on the same die but they offer different data output options as well as different package.

This paper will focus on EV12AD550 ADC (cf. Figure 1) which is dedicated to space applications with hermetic package.

Figure 1: Picture of EV12AD550 (before and after hermetic sealing)

IV. Features and Targeted Performance

- Dual channel 12 bits 1.5GSps ADC
- Single core architecture ADC
- Differential analog input voltage: 1Vppd
- Full Power Input bandwidth (-3dB): 4.3GHz
- Differential clock input
- Power consumption: 2.3W / channel
- Power supplies: Single Rail 3.4V or Dual rail 3.4V/2.5V
- Output interface: LVDS DEMUX 1:1 or 1:2
- Package: Hermetic CCGA323 21x21mm / 1mm pitch, Aluminum nitride material, Six Sigma columns and LGA.
- SPI configuration with space protection control.
- Multiple ADC chained synchronization.
- Test mode: ramp, flash, PRBS.
- Control bit: parity, in-range, trigger.

PERFORMANCE

- 4.3GHz analog input bandwidth (-3dB)
- 50 dB measured NPR over 1st Nyquist
- 48 dB estimated NPR over 3rd Nyquist
- 71 dBFS SFDR at 100MHz, -1dBFS
- 73 dBFS SFDR at 1900MHz, -8dBFS
- 73 dBFS SFDR at 3730MHz, -12dBFS
- TBD SFDR at 5300MHz, -12dBFS

V. Synchronization of Multiple High-Speed Data Converters

A novel method for synchronizing multiple data converters is proposed. It is based on a daisy chain approach between data converters and one or multiple processing units, i.e. Field Programmable Gate Array (FPGA) or Application Specific Integrated Circuit (ASIC). A synchronization pulse is propagated between data converters. The Figure 2 shows a diagram of the interface between multiple data converters and a processing unit.

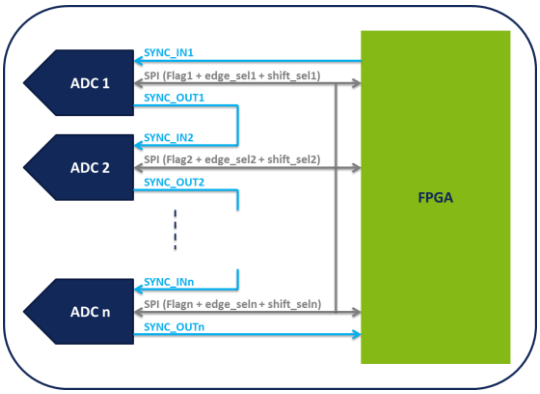


Figure 2: Multiple-device synchronization system overview

Three settings are necessary to manage or configure each ADC:

- Flagx: this signal indicates whether the synchronization pulse is in a meta-stability zone in regards to the clock of the data converter;
- Edge_selx: this signal is configured to choose which edges of the clock of the data converter is used to recover the synchronization pulse;
- Shift_selx: this signal is configured to add a certain number of clock cycle delays to the synchronization of the device after the pulse has been recovered by the data converter

The SYNC_OUT is a copy of the SYNC_IN that is sampled on the reference clock common to all data converters to ensure repeatability of the timings between power-ups and each time the synchronization process is started. Using the three settings, and a training of the system, the different data converter can be synchronized.

Calibration procedure and first measurement results are shown in [9].

This synchronization process brings multiple advantages to systems having very large count of channels:

- The parameters are accurate between power-ups, synchronization process and printed circuit board based on the same design. This is useful to develop industrial scale system, as the determination of the parameters can be done during prototyping only;
- This method relaxes all layout constraints on the SYNC signal. This means that it can be propagated on one board, or between multiple boards through a backplane which is unavoidable when systems have hundreds of channels to synchronize;
- This method is also compatible with different implementation. The daisy chain shown in Figure 2 is one of them but a tree configuration is possible as

well as any hybrid between the two. This brings flexibility to the system;

- Finally, this method does not impact the sampling clock performance. This is essential as some synchronization method adding delays on the sampling clock can degrades its jitter and thus degrade the SNR (Signal to Noise Ratio) performance of the data converters. Communication and wideband radar are two applications which performances are limited by SNR.

In terms of limitations, there are still layout constraints on the reference clock that needs to be time aligned at the input of all the data converters which is not easy to achieve. However, method exists to help either through digital processing or using a slow reference and PLLs to generate the fast clock fed to the high-speed data converters.

Speed wise, this method is limited by the setup and hold time and jitter achievable compared to the reference clock.

VI. Package Technology

For EV12AD550, the option of FlipChip technology appeared naturally. The benefits of flip chip are very interesting in terms of performances, package size, thermal dissipation through top of lid and Thermal Interface Material(TIM). Also, hermeticity was mandatory and hermetic flip chip qualification had never been qualified before in Europe. In addition, standards are required for Space applications.

e2v is a key player in Europe acting as prime contractor of a cooperative project to develop a European Flip Chip hermetic assembly process (cf. Figure 3) in collaboration with Thales Alenia Space, ATMEL, AIRBUS and funded by ESA. also e2v works with other European partners on the evolution of the ESCC9000 and ESCC2269000 to take into account specific requirements of hermetic FlipChip assembly process [10]. As a consequence, EV12AD550 has been developed using flip-chip assembly technology to improve performance and size (cf Figure 4 and Figure 5).

Aluminum Nitride (AlN) material has been chosen in order to achieve the best possible thermal performance with Rth < 4°C/W and only 4.7°C/W from junction to soldering joints, and reduced thermal expansion mismatch between silicon and substrate. The selected supplier of AlN material for EV12AD550 is Kyocera.

Extensive RF and electromagnetic simulations have been performed to secure the target performances.

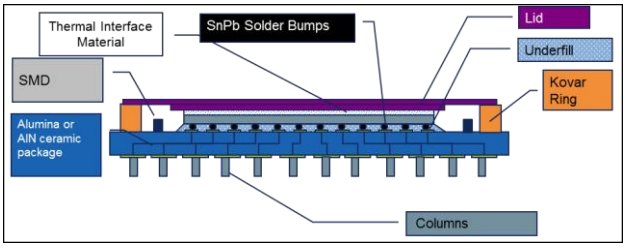


Figure 3: Hermetic FlipChip Package drawing for space

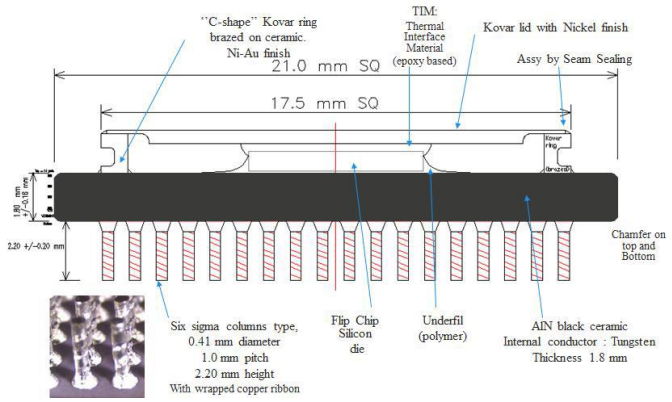


Figure 4: EV12AD550 Package drawing cross section

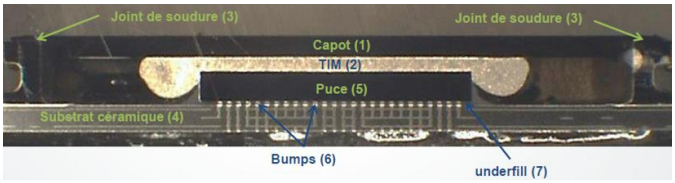


Figure 5: EV12AD550 Package cross section

VII. Radiation Hardening

ST BiCMOS9 technology does not propose rad hard library. A radiation campaign performed on a similar product - same type of product designed in the same technology and using a similar architecture - without any design rad hard protection has allowed giving a first level of confidence in intrinsic technology and architecture robustness.

Designing EV12AD550 a lot of special cares both in product architecture, cells designs, layout implementation have been done in order to either limit the impact of radiation event and/or decrease the event occurrence by increasing the required critical charge threshold to trig an event.

A. Layout for radiation considerations

Specific implementation rules have been defined and adapted case to case to limit ionization leakage current propagation into parasite path.

Some examples of adopted rules:

- NMOS transistor isolation with a P+ guard ring.
- Bulk tie have largely been implanted in order to limit leakage current between transistors.
- Minimization of bulk resistance by placing bulk tie as close as the active device.

For the prevention of latchup, special rules as the following have been used:

- A deep NWELL NISO is used to isolate the digital blocks (cf. Figure 6).

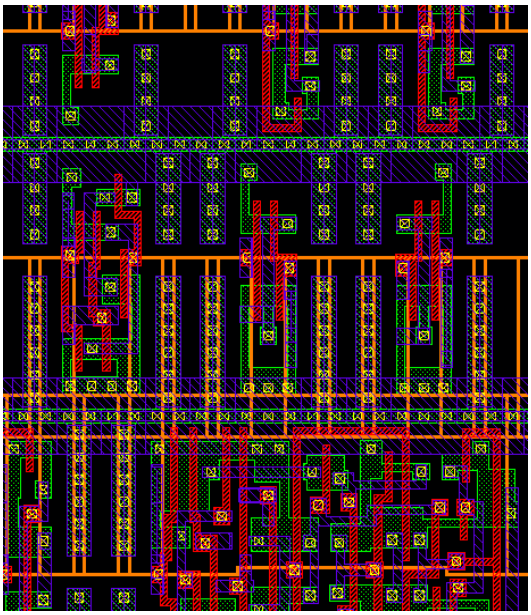


Figure 6: Detail of digital block circuit

- Enlarge minimum space between p and n zones in all analog part by adding deep trench isolation, isolated bulk including rail power supplies.

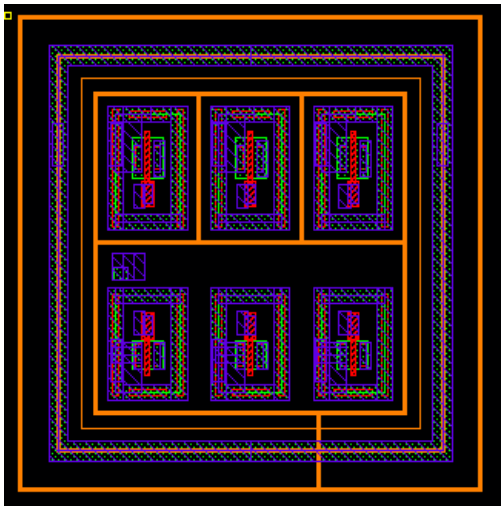


Figure 7: Detail of analog block circuit

- Reduce the serial resistance of the parasite thyristor to prevent from activation.
- Multiply the number bulks and substrates ties
- Larger of guard ring should not be too much resistive ie it is mandatory to not open them.
- Increase minimum distance between guard ring.
- Between NWELL and PWELL it is necessary to put a double guard ring connected to VDD/VSS.

Specific tools such as DRC (Design Rules Check, fault injection,…) have been developed by e2v for superior automation.

B. Design protection approaches

Design protection techniques to prevent occurrence of events include: large drive current of transistors, large transistors, large capacitance.

1) Analog architecture

When possible, analog redundancy has been used. That consists of parallelizing "n" times a circuit and connecting replicated nodes to a common node. So that the perturbation effect is divided by "n".

Analog Filtering is recommended to reduce SET. In order to increase node time constant and then increase the parasite critical charge required to produce a SET, Miller capacitance and/or resistance have been used.

2) Digital architecture

The protection of digital blocks is one of the most challenging topics as no rad hard library are available. In addition to the layout protection listed above, architecture will be optimized by implementing:

- TMV (triple redundancy voting)
- Antiglitch structure.
- A special mode (SE Protect) has been implemented to strengthen the radiation immunity to Single Event Functional Interrupt (SEFI).

However the drawback of all those protections is that they constrain the performances in terms of power consumption, speed, and size. That is why a specific study has been done on each block in order to protect the most critical nodes.

VIII. MEASUREMENTS

In this section we present some of the measurement results in terms of electrical performance and radiation test results.

A. Electrical performance highlights

Achievements of targeted performance are demonstrated in the figures below (cf. Figure 8, Figure 9, Figure 10, Figure 11). These measurements have been made on first silicon run leading to conclude the design is a first time right achievement.

B. Radiation results highlights

Preliminary Total Ionizing Dose (TID) measurement results are available at dose rate of 180 Rad(Si).h^{-1}. A complete radiation test will be published on the manufacturer webpage when available [11]. No significant drift is observed up to 150 kRad (cf. Figure 12 and Figure 13).

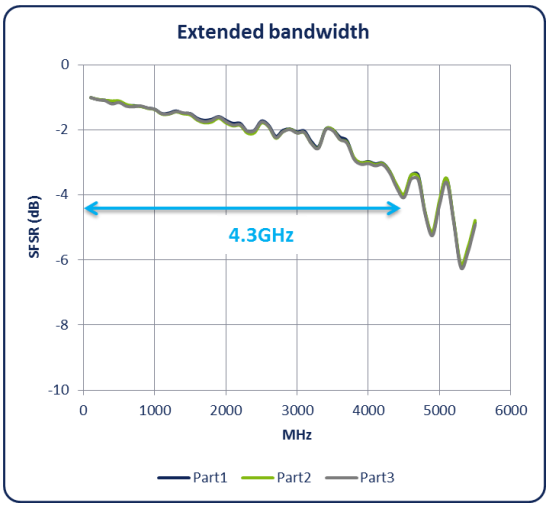


Figure 8: Analog input bandwidth

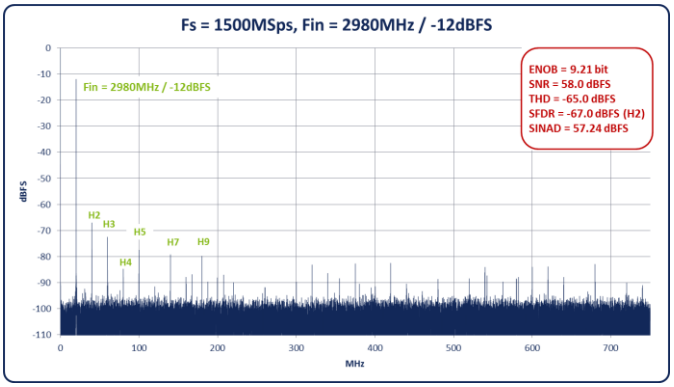


Figure 9: Typical spectrum in 4th Nyquist zone

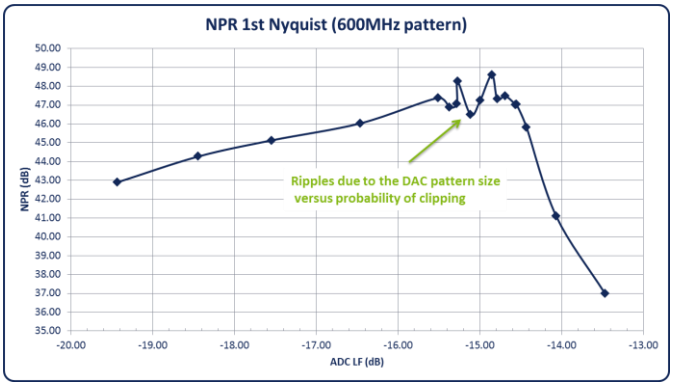


Figure 10: NPR measurement in 1st Nyquist

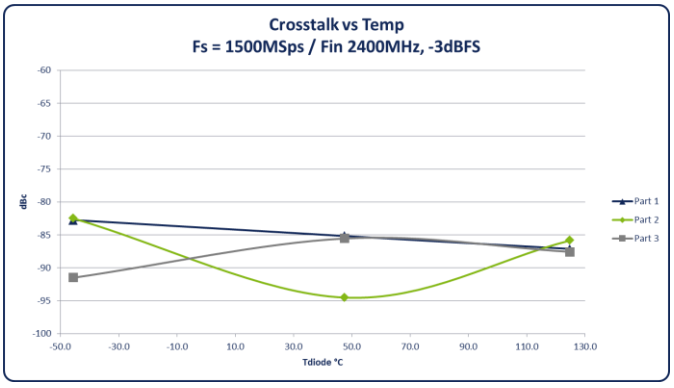


Figure 11: Crosstalk measurement versus temperature

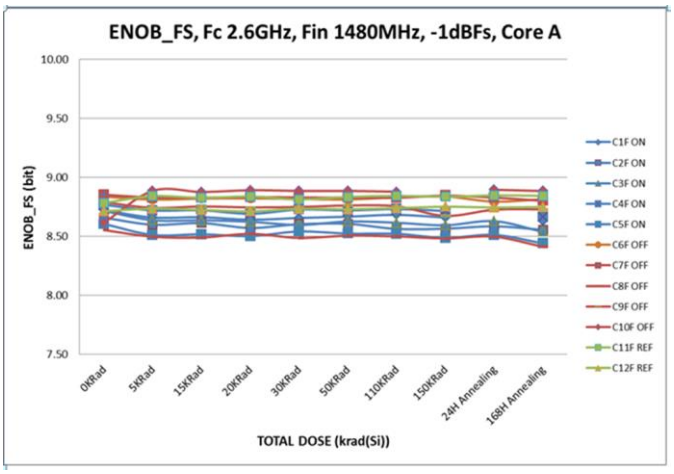


Figure 12: TID results (ENOB vs Total Dose) Fclock = 2.6 GHz

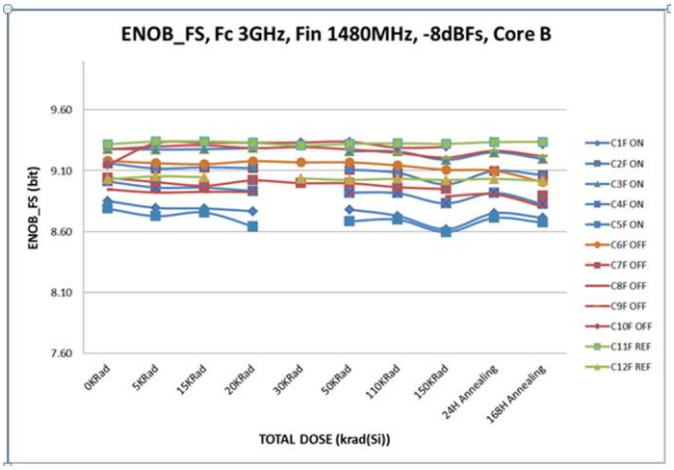


Figure 13: TID results (ENOB vs Total Dose) Fclock = 3 GHz

IX. Conclusion

- This product demonstrates a successful combination of innovations (hermetic flip chip in AlN, Rad Hard product on STM BiCMOS9 technology, Single rail operation, first time S-band digitization on dual channel with solid crosstalk performance in only 21x21 mm^2 hermetic package
- As of today first time right design demonstrated by early measurements on silicon.
- R&D works to reach further optimization are on-going.
- Industrialisation & ESCC evaluation and Manufacturer Qualification works are in progress.
- Performance improvement works are also expected thanks to the implementation of embedded algorithms from e2v's newly acquired Sweden-based team at SP Devices - Linköping.

X. REFERENCES

[1] F. Malou et al, "First telecom application of digital components developments: 65nm ASICs and Data Converters", Proceedings of ESCCON 2016

[2] M. Laurens, et al., "A 150 GHz Ft/Fmax 0.13 µm SiGe:C BiCMOS technology", IEEE Bipolar / BiCMOS Circuits and Technology Meeting, pp. 199-202, 2003

[3] Available on Kyocera's Website: www.global.kyocera.com/prdct/semicon/index.html

[4] H. Fenech, et al, "Eutelsat Quantum-class satellites, answering the operator's need for flexibility", 3rd ESA Workshop on Advanced Flexible Telecom Payloads, 2016

[5] A. Le Pera, "HTS gateway network optimization by using on-board regenerative processor", 3rd ESA Workshop on Advanced Flexible Telecom Payloads, 2016

[6] H. Gachon, et al., "Spaceflex digital transparent processor for advanced flexible payloads, 3rd ESA Workshop on Advanced Flexible Telecom Payloads, 2016

[7] G. Adamiuk, et al., "SAR architecture based on DBF for C-band and X-band applications", Proceedings of 10th European Conference on Synthetic Aperture Radar (EUSAR), 2014

[8] A. Panetti, et al., "Sentinel-1 spacecraft", Proceedings of 10th European Conference on Synthetic Aperture Radar (EUSAR), 2014

[9] M. Stackler, et al., "A novel method to synchronize high-speed ADCs", Proceedings of IEEE Radar Conference, 2016

[10] J.P. Peltier, "The insertion of FlipChip technology in space systems", Proceedings of ESCCON 2016

[11] e2v's webpage: http://www.e2v.com/products/EV12AD550

On the Design of a Rad-Hard Signal Conditioning ASIC for Pressure Modules

A. Mitrovgenis[a] , G. Fikos[a], P. Broutas[a], N. Valantassis[a], A. Papadimitriou[a], T. Athanassopoulos[a]
A.Michalakou[a], A.Depastas[a], I. Llambro[a], G. Metaxas[a], K. Spyropoulou[a], S. Filippas[a], E. Zervakis[a]

[a]European Sensors Systems, 19400, Koropi, Attiki, Greece

{mitrovgenis, fikos, broutas, valantassis, papadimitriou, athanassopoulos, michalakou, depastas, llambro, metaxas, spyropoulou, filippas, zervakis}@esenssys.com

Abstract

European Sensor Systems has designed, fabricated and tested a radiation tolerant signal conditioning ASIC for capacitive sensors in the course of an ESA activity for "Standard Accuracy Pressure Transducer". This paper presents the architecture of the ASIC, the radiation mitigation strategy, the electrical characteristics and the radiation results.

I. INTRODUCTION

European Sensor Systems develops and manufactures high quality sensors based on MEMS technology. In the course of ESA activity "Standard Accuracy Pressure Transducer" [1], European Sensor Systems has been developing a "Space Qualified Family of MEMS Pressure Modules for Satellite Applications". European Sensor Systems has designed four MEMS sensors to cover the application's pressure ranges (7, 22, 150, 310 bar) with dimensions 2×2×0.4 mm^3 using European Sensor Systems TM30P1111 technology, which is a combination of SOI, bulk and surface micro-machining process for the fabrication of capacitive pressure sensors. European Sensor Systems is the IP owner and exclusive user of this process.

A custom radiation-hardened capacitive sensor signal conditioning ASIC has been designed to interface with the MEMS. Based on the architecture of its commercial counterpart ASIC, the chip is built using X-FAB XH018 Process, a 0.18 micron Modular Mixed Signal HV CMOS Technology.

The structure of the paper is as follows. Section I presents the detailed architecture of the ASIC, Section II presents the radiation mitigation strategy, Section III presents the ASIC characteristics and Section IV presents the radiation results.

II. ARCHITECTURE OF THE ASIC

The architecture of the ASIC is shown in Figure 1. It is a mixed-signal radiation-hardened capacitive sensor signal conditioning ASIC.

The external voltage supply is 5.7V and is internally regulated to 3.3V both for the analog and digital part. The core of the ASIC is the capacitance-to-voltage converter. The output of this block is converted to a 1-bit output by second-order ΣΔ modulator, which is then down-sampled and low-pass filtered in the digital domain.

The ASIC provides two pressure outputs: a 32-bit digital output accessible via the serial communication interface along with a Pulse Width Modulation output bit stream of 10-bit resolution.

The ASIC also features an internal temperature sensor with a 32-bit digital output accessible via the serial communication interface.

The trimming of the device is performed via register programming using an I^2C compatible Two Wire Interface (TWI). A specific configuration can be written to the One Time Programmable (OTP) memory. The internal analog and digital regulator, the bandgap reference, the oscillator and the power-on reset eliminate the need of any additional components.

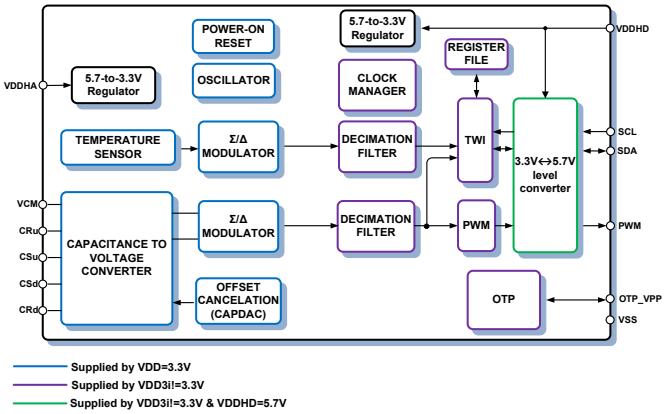


Figure 1: Functional block diagram of ASIC

A. Voltage regulation scheme

The ASIC has two distinct power domains: the 3.3V digital domain and the 3.3V analog domain with common ground. The chip is supplied by Texas Instruments' LM117 [2], which is configured to provide 5.7V. The output voltage of the external regulator needs to be converted to 3.3V for the operation of the digital and analog sub-blocks. This is realized using a 5.7-to-3.3V regulator for the digital part and a 5.7-to-3.3V regulator for the analog part. The I/O communication is performed using the high 5.7V supply in conjunction with appropriate level-shifting of 3.3V to 5.7V and vice-versa.

B. Capacitance to Voltage Converter

MEMS capacitive pressure sensors consist of two sense capacitors ($C_{Su,}$ C_{Sd}) and two reference capacitors ($C_{Ru,,}$ C_{Rd})

and typically have a steady-state capacitance C_0 in the order of few pF. MEMS capacitors share a common plate. The Capacitance to Voltage Converter implements Eq. (1).

$$\Delta V_{OUT} = \frac{\left(C_{Su} - C_{Ru} + C_{Sd} - C_{Rd}\right)}{C_F} \cdot \frac{V_{DD}}{2} \qquad \text{Eq. (1)}$$

where C_F is an internal capacitor for gain adjustment in a fully differential configuration. The fully differential topology offers many advantages such as rejection of common mode non-idealities and noise and suppression of even order non-linearities. Noise reduction techniques were implemented to reduce the low-frequency noise and offset.

Offset cancellation capability is implemented by digitally trimming internal capacitor arrays in parallel to each MEMS input capacitor.

C. ΣΔ A/D converter

ΣΔ modulators are low complexity oversampling A/D converters appropriate for baseband narrowband applications. The theoretical Signal to Noise Ratio (SNR) of an L^{th} order modulator with an N-bit quantizer and decimation rate DR is given by Eq. (2).

$$\text{SNR}=10log_{10}\left[\frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)(2^N-1)^2 DR^{2L+1}\right] \qquad \text{Eq. (2)}$$

The design of the modulator is based on a switched-capacitor topology with implementation of noise reduction techniques to eliminate the noise. It is a second-order topology based on a cascade of resonators with 1-bit quantizer. It combines a non-delaying and a delaying integrator to form a stable resonator. The choice of 1-bit quantizer is a compromise between complexity and performance.

The outputs of the capacitance-to-voltage converter Vout-p and Vout-n are sampled by the modulator. The 1-bit output is processed by a low-pass decimation filter. The architecture of the filter is based on cascaded integrator-comb (CIC) filter. By using a CIC filter the computational complexity is reduced compared to narrowband low-pass Finite Impulse Response (FIR) filters. An efficient way to realize a decimation filter consists of a series of L cascaded accumulators followed by a cascade of L differentiators [3] implementing Eq. (3).

$$\text{H(z)}=\left[\left(\frac{1-z^{-M}}{1-z^{-1}}\right)^L\right] \qquad \text{Eq. (3)}$$

where L is the order of the filter and M is the differential delay.

D. Pulse Width Modulation Unit

The filtered output of the CIC filter is converted to a 10-bit resolution pulse width modulation (PWM) bit stream at the frequency of 10 KHz, which corresponds to the raw analog signal from the sensor. The PWM signal is then filtered off-chip by an RC filter in order to generate an analog signal. The PWM output pulse can be adjusted in terms of scale factor and offset.

III. RADIATION MITIGATION STRATEGY

In order to address the problem of Single Event Upsets (SEUs), the Triple Module Redundancy (TMR) method with voting has been adopted. This mitigation scheme uses three identical logic circuits performing the same task in parallel with corresponding outputs being compared through a majority voter circuit. The technique has been applied at the level of digital synthesis. The TMR technique has been applied to all flip-flops of the digital part.

For Single Event Latch-up (SEL) immunity in the digital part, a library of custom digital cells has been designed and modeled in house. The library contains combinational, sequential and special cells (layout fillers, antenna protection cells). It was based on existing cells of the digital library D_CELLSL_JI3V (triple-well junction isolated cells for 3.3V operation). The increase of the layout area of the rad-hard cell compared to its conventional counterpart varies from 2x to 4x.

In the analog part, all PMOS devices have been enclosed by N-type guard rings and all the NMOS devices have been enclosed by P-type guard rings.

IV. ELECTRICAL CHARACTERISTICS

The layout of the ASIC is shown in Figure 2.

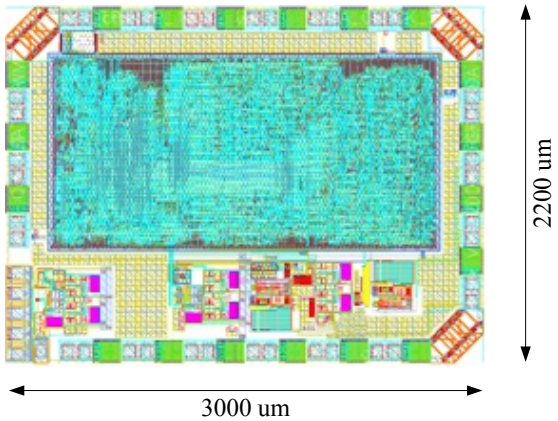


Figure 2: ASIC layout

The PCB with the fabricated ASIC and MEMS is shown in Figure 3.

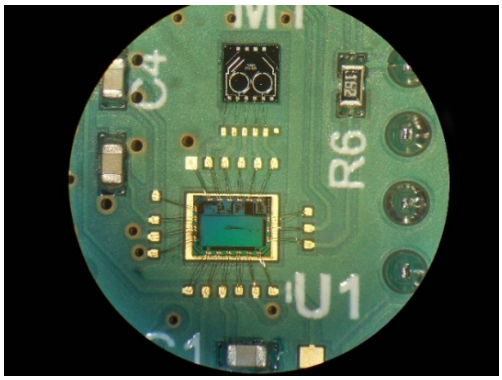


Figure 3: PCB with ASIC and MEMS

The ASIC characteristics are summarized in Table 1.

Table 1: ASIC Characteristics

VOLTAGE/CURRENT LEVELS	
Analog Part Voltage Supply (VDDHA)	5.2V-6.2V
Digital Part Voltage Supply (VDDHD)	5.2V-6.2V
Regulated Analog Voltage	3.3V, PSRR 50 dB @1KHz
Regulated Digital Voltage	3.3V, PSRR 50 dB @1KHz
OTP Programming Value	7.2V
Current Consumption	7mA
CLOCK	
Oscillator Frequency (programmable)	10MHz
CAPACITANCE TO VOLTAGE CONVERSION	
C_0: Base Capacitance	20pF (typ) to 100pF (max)
ΔC: FS Input Capacitance Range	± 2.8 pF
Digital Pressure Output Resolution	> 19 bits @10 Hz
Decimation Rate (BW)	256-32768 (1.3KHz-10Hz)
PWM OUTPUT	
PWM resolution	10-bits
PWM frequency	10 KHz
TEMPERATURE SENSOR	
Accuracy	±1°C
Resolution	0.1°C
Sensitivity	1.6 mV/°C
ENVIRONMENTAL CONDITIONS	
Temperature Range	-40°C to 100°C
SERIAL COMMUNICATION INTERFACE	
Two Wire Interface, I^2C compatible	
ISD Interface	

V. Preliminary Radiation Tests Results

For the radiation tests a low-pass RC filter with cut-off frequency f_c at 10 Hz is used.

Ten ASICs –shown in Figure 4- have been tested for Total Ionization Dose (TID) up to 100 Krad at ESA ESTEC facility.

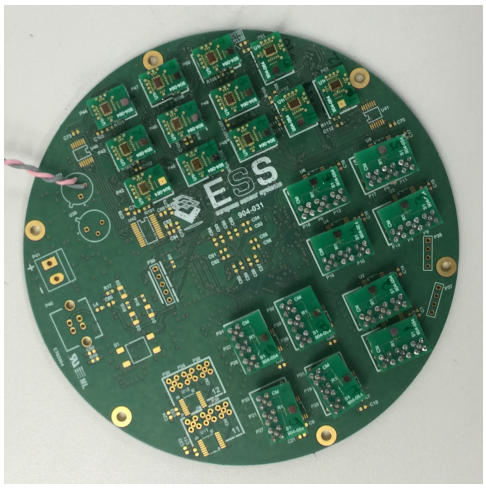


Figure 4: PCB with mounted DUTs for TID

Figure 5a shows that the digital pressure output varies less than 1 mV over all irradiation steps. Figure 5b shows a drop of approximately 325mV in the RC filtered PWM output versus TID dose.

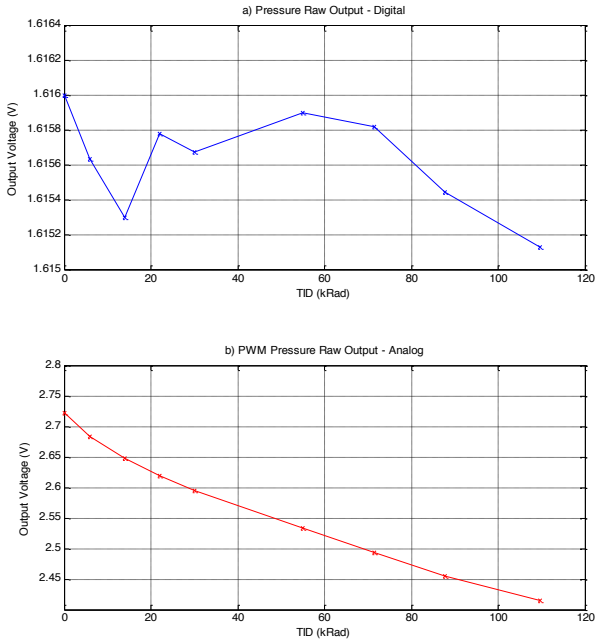


Figure 5: a) Pressure raw digital output b) PWM pressure output vs. TID dose

The digital output of the PWM block has a range of 0V to 3.3V. It is up-converted to the range of 0V to 5.7V. The inverter of the last stage of the level-converter is implemented using high-voltage transistors (Figure 6). Due to irradiation the off-resistance of transistor M_1 is decreasing [4], thus its sink current is increasing explaining the voltage drop shown in Figure 5b.

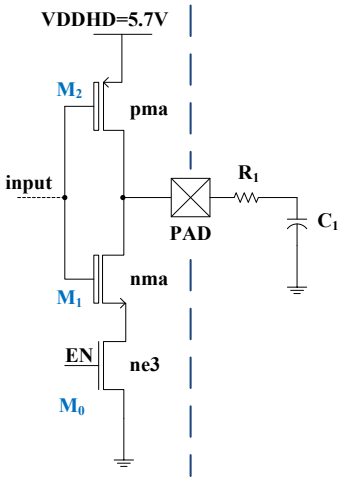


Figure 6: Output stage of 3.3V-to-5.7V level converter and RC filter

Figure 7a shows the outputs of the analog (blue line) and digital (green line) regulators. The experimental shift (increase) over radiation is about 1%, and is attributed to the incorporation of several High-Voltage transistors, as in the case of the regulators' pass element.

Figure 7b shows the digital temperature output (solid blue line). The predicted digital temperature output (dashed blue line, Figure 7b), assumes constant temperature and takes into account the aforementioned analog regulator's output shift. By comparing the two curves, it is deduced that the analog regulator's output shift, is mostly responsible for the shift on the digital temperature output. The remaining difference is well within the environment's temperature variation, suggesting that the temperature sensor, which is based on a bandgap-type circuit with bipolar transistors, is also tolerant to TID (up to 100 Krad).

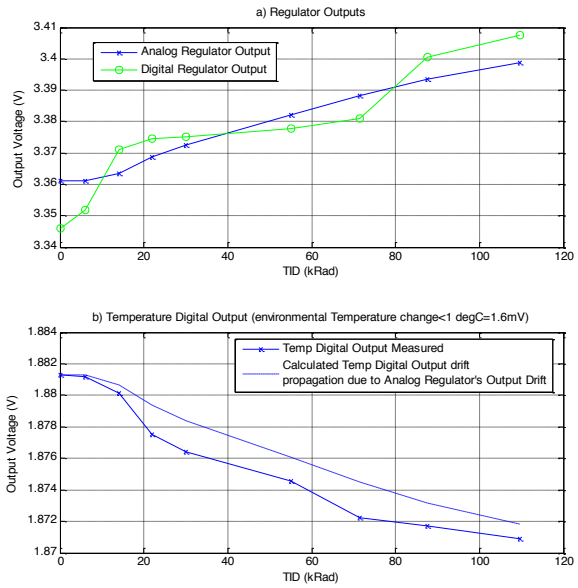


Figure 7: a) Regulator outputs b) Temperature Digital output

Three ASICs have been tested for SEE/SEL in the UCL cyclotron accelerator facility – as shown in Figure 8. The ASIC exhibited SEL immunity up to 62.5 MeV/(mg/cm^2) using Xe-995. Instantaneous increases of current consumption were visible in the digital part and can be attributed to SEFIs. Restore to normal operation performance occurred without any external intervention.

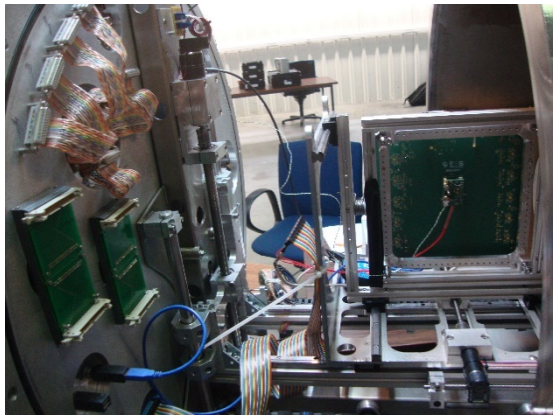


Figure 8: SEE test setup

Preliminary post-processing of irradiation results suggests SEU immunity at least up to 32.4 MeV/(mg/cm^2) using Kr-769.

Displacement damage tests have been performed at three ASICs at UCL up to 62 MeV and a LET of $8.39 \cdot 10^{-3}$ MeV/(mg/cm^2) without any performance degradation.

VI. Conclusions

The design of radiation tolerant ASIC in a standard 0.18um CMOS process has been presented. The fabricated chip exhibited immunity to SEL, SEU and DD proving that the radiation mitigation strategy was successful. TID up to 100 Krad did not affect the ASIC's core, which utilizes Low-Voltage transistors, while High-Voltage transistors are responsible for any performance degradation.

European Sensor Systems is currently assessing the necessary redesign steps to address the above issues.

VII. References

[1] ESTEC Contract No: 4000 111841/14/NL/CBi

[2] Texas Instruments, LM117, LM317-N Wide Temperature Three-Pin Adjustable Regulator Datasheet Available: http://www.ti.com/lit/ds/symlink/lm117.pdf

[3] E. Hogenauer, (1981). "An economical class of digital filters for decimation and interpolation". IEEE Transactions on Acoustics, Speech and Signal Processing, Vol. ASSP-29, No 2, p. 155–162.

[4] D. Moroni (Airbus DS) et al, "Radiation-Tolerant High-Voltage ASIC Library Evaluation for Space Applications", AMICSA 2014.

SOI CMOS Frequency Synthesizer for Flexible Communications Payloads

Seong-Mo Moon, and In-Bok Yom

Electronics Telecommunications Research Institute (ETRI), 34129 Daejeon, Korea

smmoon@etri.re.kr

Abstract

This paper presents designed and measured results of a fractional-N frequency synthesizer in SOI CMOS Technology for next generation flexible communication payload. A tuning range from 4 GHz to 6 GHz is achieved using three integrated voltage-controlled oscillator (VCO), which enables all frequencies generation bellows 6 GHz by frequency division. Using current mismatch compensation circuit in charge pump, in-band phase noise of -93 dBc/Hz is achieved at 100 kHz offset in fractional-N mode. Also, to design radiation hardened Frequency synthesizer, we use design technique such as radiation hardening by design (RHBD), radiation hardening by process (RHBP), and radiation hardening by shielding (RHBS).

I. INTRODUCTION

The COMS payloads, up and down link frequency and the bandwidth are all fixed during the lifetime of the satellite. But increasing satellite lifetimes of more than 15 years, the ability to adapt the payload to new scenarios such as flexibility would be highly advantageous. So an agile-tunable Local Oscillator (LO) is the key components in the next generation flexible payload and needed for the development of the next generation satellite payloads. The agile wide-band frequency synthesizer based on a fractional-N PLL should be able to generate the wanted frequency within the wide-band such as S-band, C-band, and Ku-band.

Spacecraft designed to provide communications require the necessity to generate several LO frequencies for various up/down converters in the payload. The conventional technique of frequency multiplying a highly stable fixed reference signal to generate a number of LO signals will make the spacecraft higher in DC power, size and mass. In order to provide a lower spacecraft mass, size, and DC power, the LO signal generation must be accomplished by miniaturized digital integrated frequency synthesizers based on phase locked loops. Many circuits in Silicon, BiCMOS, Silicon-on-Insulator (SOI), GaAs, and SiGe make it easier to develop systems with frequencies up to several GHz and beyond. [1], [2] Depending on the device technology and manufacturing process, the SEU hardness or total dose tolerance may be such that they may not be suitable for high reliability space applications.

To design radiation hardened frequency synthesizer, these design techniques such as radiation hardening by design (RHBD), radiation hardening by process (RHBP), and radiation hardening by shielding (RHBS) are required. In this paper, we designed SOI CMOS frequency synthesizer using RHBP, and RHBD based on layout technique. And we will adopt the others technique such as RHBS and RHBD such as triple-redundancy technique in current project.

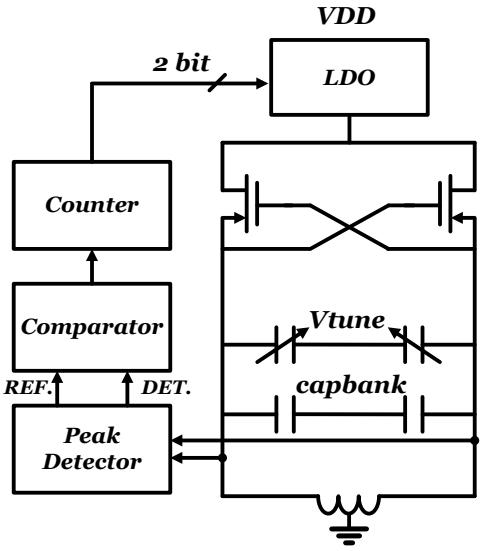


Figure 1: Block diagram of the VCO core

II. DESIGN

A. VCO core design

To increase flexibility in LO, a large frequency tuning range and excellent phase noise characteristics are a critical required in VCO core. First, in order to enhance phase noise characteristic in VCO, the current source is eliminated to reduce 1/f noise from bias line. But this architecture has other problems in VCO performance such as pushing and pulling figure, and process variation. So we use low drop-out (LDO) regulator with 2-bit output voltage control circuit in supply of VCO as shown in Fig. 1. Thus, output power and current consumption in VCO should be changed according to LDO. And this output current should also be fixed according to oscillation frequency and temperature variation to get stable phase noise performance. However, this circuit requires additional die area and noise source from LDO output is not eliminated completely. PMOS cross coupled topology is used for VCO core circuit and using five VCOs to reduce VCO gain variation according to wide range of oscillation frequency from 3.6 GHz to 6.1 GHz. 5-bit switched MIM capacitor array in each VCO is used to cover oscillation frequency of 3.6 GHz to 4.1 GHz, and 4.1 GHz to 4.6 GHz, 4.6 GHz to 5.1 GHz, and 5.1 GHz to 5.6 GHz, and 5.6 GHz to 6,1 GHz, respectively.

Due to stable operation of LDO, phase noise variation is within 2.4 dB over 1.6 ~ 2.0 V power supply and -40 ~ 85^{O}C temperature range. VCO core including LDO draws 2.8 ~ 5.6 mA according to oscillation frequency from 1.8 V supply voltage. Frequency synthesizer consists of three VCOs, PTAT bias, LO generation block such as divider and buffer (or drive) amplifier, loop-filter and fractional-N PLL.

B. PLL design

Fig. 2 shows the block diagram of the designed frequency synthesizer including 5 on-chip VCOs. The sigma-delta fractional N frequency synthesizer includes a 20-bits sigma-delta modulator of third-order MASH type so that it achieves a fine frequency resolution of about 34 kHz. The charge pump using an analog calibration method with two op-amps eliminates output current mismatch. The external loop filter is used to optimize loop bandwidth each selected frequency bands. To calibrate loop bandwidth, the charge-pump currents are able to control by programmable digital logic according to band selection. The prescaler including true single-phase clocked (TSPC) type D-type flip-flop (DFF) in N dividers has up to 1.5 GHz operations. The feedback divider consists of 10-bit pulse counter and 4-bit swallow counter.

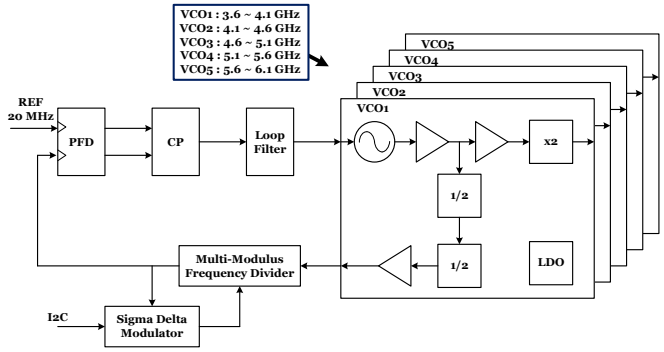


Figure 2: The block diagram of the designed frequency synthesizer including 5 on-chip VCOs.

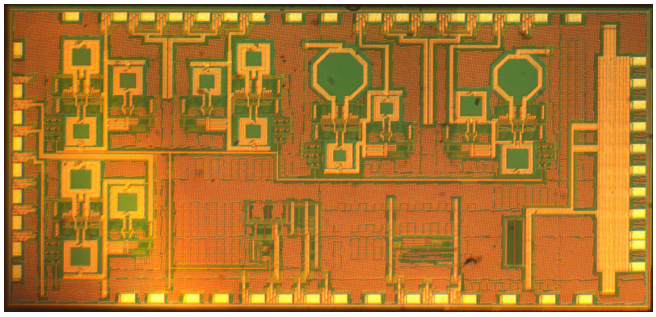


Figure 3: The chip photograph of the proposed Frequency Synthesizer including VCOs, I2C and PTAT

Fig. 3 shows the chip photograph of the proposed frequency synthesizer. The integrated frequency synthesizer including 5 VCOs, LO generation block, LDO, bias, and I2C, occupies 5.0 mm by 2.5 mm. And this IC is fabricated using 1P4M 0.18 um RF SOI CMOS process.

C. Frequency Synthesizer using External VCO

To overcome the limitation of the phase noise characteristic in on-chip VCO, we added input/output port in designed frequency synthesizer chip to use external low-phase noise VCO. Fig. 4 shows the block diagram of the designed frequency synthesizer using external VCO. Because the operation frequency in the prescaler has up to 1.5 GHz, we use divider-by-8 circuit between VCO output and PLL input. And to control VCO tuning voltage from 0 V to 15 V, active loop filter and level shifter is used in frequency synthesizer module.

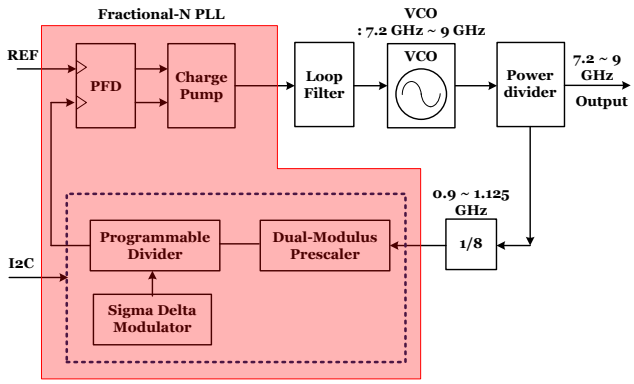


Figure 4: The block diagram of the designed frequency synthesizer using external low-phase noise VCO and divider-by-8.

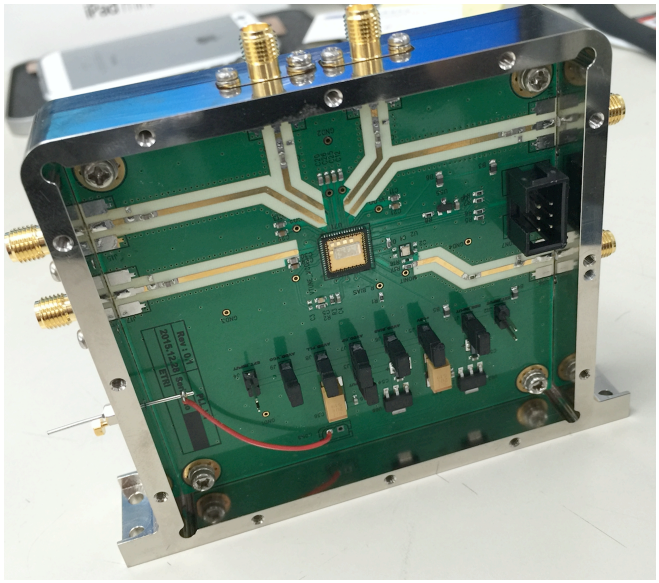


Figure 5: PLL based on on-chip VCO test board and test fixture

III. Measurement

A. On-Chip VCO measurement

The chip is fabricated in the TowerJazz 0.18 um 1P4M CMOS SOI process as shown in Fig.1. The chip size is 5 mm X 2.45 mm, and all circuit blocks have been successfully integrated on chip, including VCO, bias circuit, and I2C. The chip is measured with a 1.8V supply voltage and consumes 66 mW under maximum current settings, and 61 mW in low-current mode. The measured frequency range is from 3.6 GHz to 6.1 GHz, corresponding to a frequency tuning range of 14%. The measured PLL output spectrum at 10 GHz is shown in Fig. 7, where the phase noise is about -93 dBc/Hz, and -117 dBc/Hz at 100 kHz, and 1 MHz offset frequency. In this work, the VCO frequency tuning range is divided into 8 sub-bands, and the measured VCO gain (Kvco) is about 80 MHz/V.

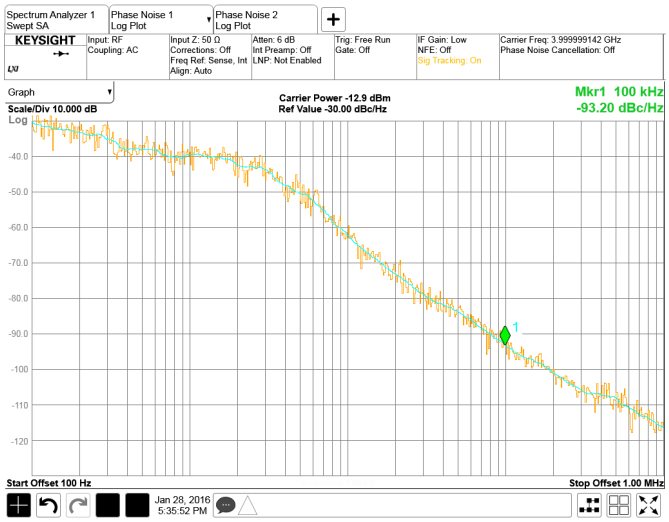


Figure 6: Measured PLL based on on-chip VCO phase noise at 4 GHz

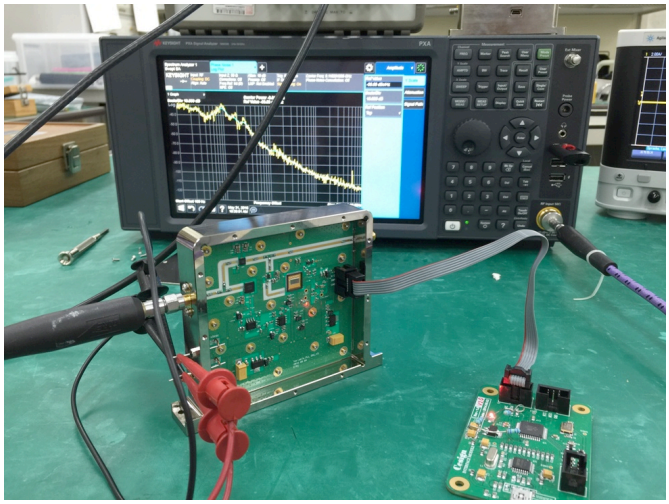


Figure 7: Frequency synthesizer using external VCO test fixture and test setup photograph.

B. External VCO measurement

The PLL module using designed SOI CMOS PLL is fabricated based on Rogers4003C substrate and using Hittite HMC509LP4E VCO, and HMC494LP3 frequency divider as shown in Fig. 2. Fig. 6 shows the PLL module and test set-up. The test fixture size is 100 mm x 94 mm, and all circuit blocks have been successfully integrated on chip, including VCO, bias circuit, and I2C. The frequency synthesizer module is measured with a 5V supply voltage and consumes 1250 mW in typical value. The measured frequency range is from 7.2 GHz to 9.0 GHz. The measured PLL output spectrum at 8.95 GHz is shown in Fig. 7, where the phase noise is about -100 dBc/Hz, -112 dBc/Hz, and -131 dBc/Hz at 100 kHz, 1 MHz, and 10 MHz offset frequency. In VCO, the VCO frequency tuning range is determined by voltage tuning from 0 V to 15 V, and the measured VCO gain (K_{VCO}) is about 100 MHz/V at control voltage of 5 V. Table 1 compares the PLL performance with that of other PLLs designed 10 GHz applications.

Figure 8: Measured PLL using external VCO phase noise at 8.5 GHz

IV. Conclusion

This paper provides an overview of frequency synthesizer design techniques for Communications Satellite payloads. The proposed flexible LO architecture shows wide-band, low-power, and low phase noise performance with optimal current consumption for various satellite payload frequency band. Thus, this type of synthesizer can be used in multi-band flexible agile LO.

V. Acknowledgments

This work was supported by ICT R&D program of MSIP/IITP. [No. B0101-16-0141, Development of Flexible Payload Technologies for Next Satellite Broadcasting and Communications]

VI. References

[1] L. Dayaratna, L.G. Ramos, M. Hirokawa, and S. Valenti, " Multi output Frequency Generation System for AMC 15/16 spacecrafts", 22nd International Communications Satellite Systems Conference, Monterey, CA, May 2004

[2] Author L. Dayaratna, J. Tanzini, and L. G. Ramos. "The Architecture for Controlling 420 Frequency Synthesizers On Board the Asia Cellular Satellite System (ACeS)", 19th AIAA International Communications Satellite Systems Conference, Toulouse, France, April 2001.

[3] Y.-J. Lai and T.-H. Lin, "A 10-GHz CMOS PLL with an agile VCO calibration," in Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC), Nov. 2005, pp. 213–216.

[4] Yu-Jen Lai and Tsung-Hsien Lin. "An Agile VCO Frequency Calibration Technique for a 10-GHz CMOS PLL" IEEE Journal of Solid-State Circuits Vol. 42, NO. 2, Feb. 2007.

[5] Sin-Jhih Li, Hsieh-Hung Hsieh, and Liang-Hung Lu, "A 10 GHz Phase-Locked Loop with a Compact Low-Pass Filter in 0.18 um CMOS" IEEE Microwave and Wireless Components Letters, Vol. 19, NO. 10, Oct. 2009.

Table 1: Summary table for comparison with other PLLs.

Ref.	Unit	[3], [4]	[5]	This paper On-chip VCO	This paper External VCO
Frequency Range (GHz)	GHz	8.67 GHz ~ 10.12 GHz (14.3%)	10.1 ~ 11 GHz	3.6 GHz ~ 6.1 GHz	7.2 GHz ~ 9 GHz
Phase noise (1 MHz offset)	dBc/Hz	-102 dBc/Hz	-100 dBc/Hz	-117 dBc/Hz	-112 dBc/Hz
Technology	Nm	TSMC 0.18 um 1P6M CMOS	0.18 um CMOS	TowerJazz 0.18 um 1P4M SOI CMOS	TowerJazz 0.18 um 1P4M SOI CMOS
Power consumption	mW	44mW/70mW	113 mW	66mW	1250 mW (including external VCO, divider)
KVCO	10	~ 300 MHz/V	-	~ 80 MHz/V	~ 100 MHz/V
Chip Size	12	1400 um x 964 um	0.86 x 0.68 mm	5000 um x 2450 um	600 um x 700 um (PLL only)
Reference spurs	dBc	-48	-50	-50	-50

Challenges of Designing a Radiation Tolerant Motion Control System on Chip

B. Ferguson[a]

[a]Microsemi Inc, One Enterprise, Aliso Viejo, California, USA

bferguson@microsemi.com

Abstract

Complex motion control systems encompass power drive electronics, sensor electronics and digital control algorithms. The system functions can be partitioned into several integrated circuits to optimize the IC processes for sets of functions with common characteristics. Applications typically have a degree of commonality that can be exploited to provide versatility for a given chip set. Versatility is also facilitated in the IP blocks developed for the control algorithm. Radiation tolerance is achieved by process choices and radiation tolerance by design. Radiation testing includes total ionizing dose, enhanced low dose radiation sensitivity, and single event effects.

I. Introduction

The system design challenges involve conceptualizing a versatile part to support a wide range of motion control applications. The design challenges for developing a radiation tolerant motion controller involve partitioning the circuit into realizable functions that can be implemented within the limitations of the intended power and voltage rating of the IC process used for a particular block. The challenge for the process engineer is finding or developing a radiation tolerant IC process technology that can effectively implement the blocks. The circuit design of the motion control circuit blocks are challenging given the ground differences and level shifting required implementing some analogue functions. The circuit design task is complicated even more due to the unavailability of certain generally available devices that can't be used due to their radiation intolerance; this presents a challenge for the circuit designer to find innovative techniques to work around these limitations. Digital code must be written for the controller to implement the necessary algorithms and proven on the test bench. Finally the test engineer must prove functionality of the part over the environmental extremes as well as under radiation exposure.

Table 1: Challenges for Motion Control System Implementation

- System definition and specification
- Design partitioning
- Process development and characterization
- Circuit Design
- Package Design or selection
- Digital IP block development
- Functional testing
- Radiation testing

II. Discussion

System definition begins by analyzing the applications and their requirements. In a motion control system there is typically an electric motor that provides the electric to mechanical energy conversion and position feedback to monitor the progress of the movement. Motors are typically three phase and either brushless DC (BLDC) motors or stepper motors. [1] Motor drive currents vary depending on the motor size and torque it delivers. Motors are typically powered from the satellite bus power rail which can range from 22V to 150V, and may have a ground potential difference to the isolated control electronics. The motor shaft movement can be monitored using an encoder, hall-effect sensors or a resolver. Resolvers are also used to monitor rotation of structures such as antennas. If movement is linear as results from an actuator, a Linear Variable Differential Transformer (or LVDT) may be used. Since the position information is often used in a motion control system, it was decided to integrate a generic position sensing interface with a high power switch driver. In the LX7720, the motor driving switches are external and so can be optimized for the voltage and current requirements of the motor.

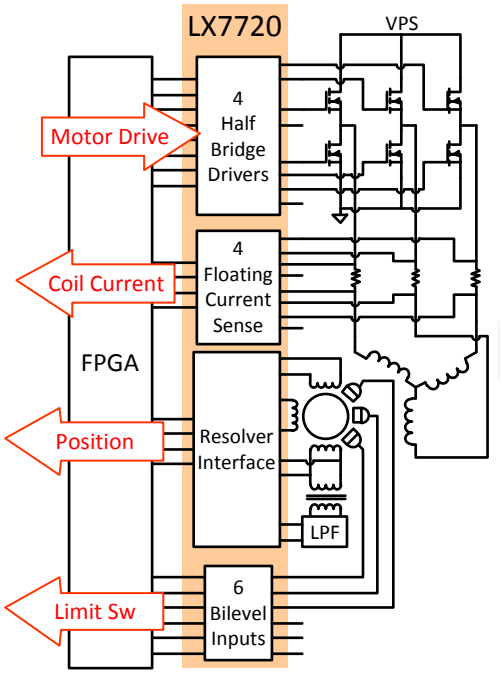


Figure 1: Block diagram of Motor Control System

The first step in partitioning a versatile design approach is to look for the common elements in all the different applications. BLDC motors require some type of switching device to sequence and regulate current to the motor coils, many applications require a pulse width modulated switch in a

half bridge configuration. Stepper motors may use a high side, a low side or a half bridge driver and in cases of a bipolar stepper motor requires two full bridge outputs.

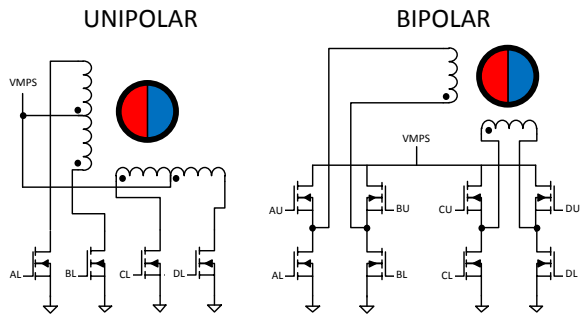


Figure 2: Two phase stepper motor configurations

When designing a half bridge driver, it's common knowledge that an N channel MOSFET is typically better performing as a switch than an equivalently sized P channel MOSFET; therefore a size and cost efficient system will utilize all NMOS power switches and floating high side drivers. All closed loop motor control algorithms require current sensing since the motor torque is proportional to the coil current; a versatile system design will provide floating current sensing that can be configured as power line (high side) sensing, ground current sensing and motor terminal (in-line) current sensing. Current sensing that is referenced to the switched node of a half-bridge configuration presents the challenge of extracting a tiny current sense voltage from a large common mode voltage signal and extremely fast common mode slew rate.

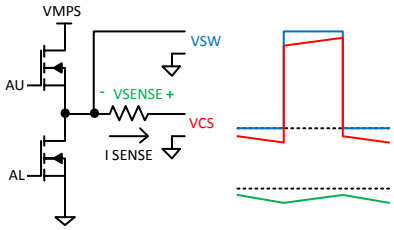


Figure 3: In-line current sense on switch node

Position sensors such as resolvers or LVDTs consist of a transformer primary driven by an exciter reference. The transformer secondary must be sampled to extract the position information. A closed loop system known as tracking conversion can compensate for a known latency based on the acceleration, speed and position errors.

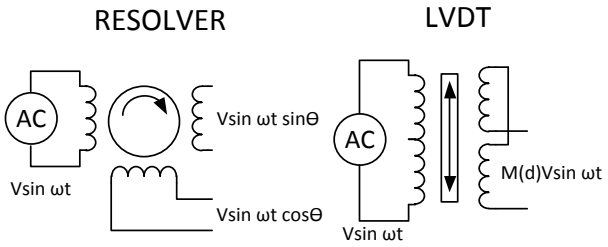


Figure 4: Resolver and LVDT

The algorithms used to control a Permanent Magnet Synchronous Motor (PMSM) are much different than what is required to control a stepper motor; a versatile system has programmable logic to adapt to the application. A versatile system with consideration for all the fore mentioned attributes is shown in Figure 1. [2]

The motion control electronics can be partitioned into three specific IC process requirements. Since motors in spacecraft can operate from voltage rails up to 150V, a process that can withstand these higher voltages is required. Also since the MOSFET drivers typically require high currents, a DMOS process is the most effective. For the signal processing and logic for the sigma delta modulator, a lower voltage process with higher density and greater bandwidth is needed. For the FPGA, a very small geometry CMOS process is required.

Processes that are adopted from commercial processes that were not specifically designed for use under radiation exposure require the development of special Process Design Kit models that take into account the effects of radiation exposure. [3] This involves exposing the devices to radiation and modeling their behavior. Later, when simulations are performed before and after radiation exposure simulations are conducted. When circuit designer uses these PDK models to design circuitry this takes into account the anticipated radiation effects and helps make the resulting circuit topologies radiation tolerant by design.

An example of a function that is partitioned between the three different ICs in this system is the floating current sense. The floating current sense uses the wide dynamic range of the high voltage IC to interface to the current sense resistor. There is an initial gain stage implemented in the high voltage process that feeds its output to an instrumentation amplifier implemented in the 5V process. The 5V IC shares the same signal ground with the FPGA. Once level shifted from floating high voltage to a signal ground referenced, the analog signal is sampled using a second order sigma delta modulator implemented in the BiCMOS process. The lower voltage process can implement functions in less space and at higher bandwidth due to the attributes of its smaller geometry. The output of the modulator is "ones density" data stream that is voltage compatible with the FPGA. The data stream consumes just one package pin as it is routed between the analog front end (AFE) and the FPGA.

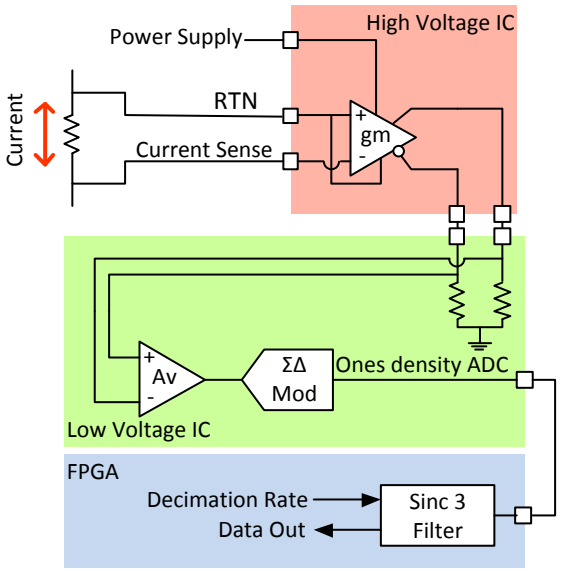


Figure 5: Floating current sense design

In the FPGA a specialized IP block performs a sinc3 filter and decimation function. In the FPGA this can be done at a speed that could not be supported in the AFE 5V process. This

pipeline from sense resistor to FPGA control loop takes full advantage of the unique capabilities of each of the ICs it passes through. The high voltage and low voltage analog silicon chips can be co-packaged as a device that appears from the pins out to be a single IC even though it contains two chips. A technique of wire bonding between the chips has been demonstrated successfully in production. This co-packaging of chips exploits the advantages of each process.

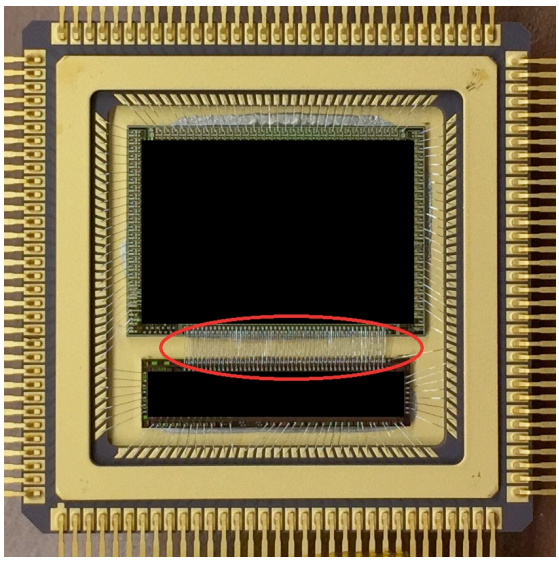


Figure 6: Interconnection between two co-package die

The use of a radiation tolerant FPGA alongside a versatile analog front end as its companion chip is the essence of our "System Manager" total system approach. The digital signal processing of the motor control function can be partitioned into functional blocks to provide the greatest level of IP reuse. Figure 3 is a block diagram of existing motor control IP blocks for a three phase BLDC motor that were developed for the SmartFusion2 fabric with the addition (in red) of new blocks that provide an interface to the sigma delta modulator outputs of the LX7720 sensor interface and the fault monitoring pins unique to the LX7720. An FPGA, such as RTG4, which includes math blocks, is recommended for this implementation.

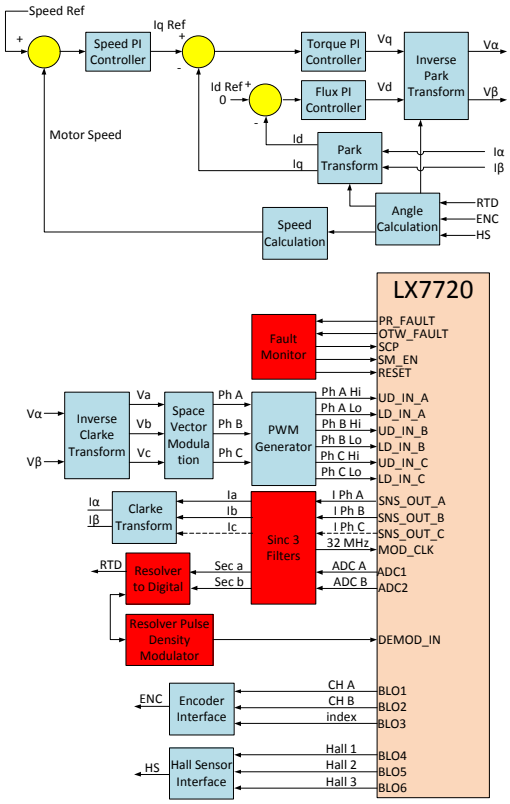


Figure 7: PMSM IP blocks using LX7720

Functions can be added or removed to an application depending on what type of control algorithm is needed. Individual blocks can be customized by setting variables. An example of a variable that controls a performance tradeoff is decimation rate setting in the sinc3 filter IP block; signals with a higher oversample rate will have higher resolution at the cost tradeoff of longer latency [4]. A CAD design tool such as Libero SoC allows blocks to be configured and customized.

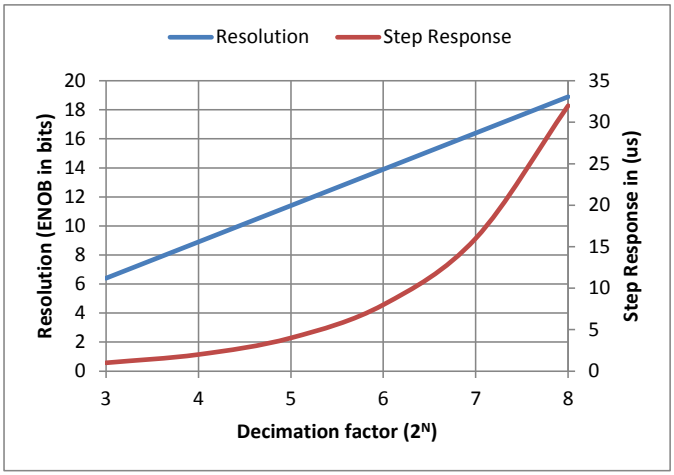


Figure 8: Decimation Trade-offs on Latency and Resolution

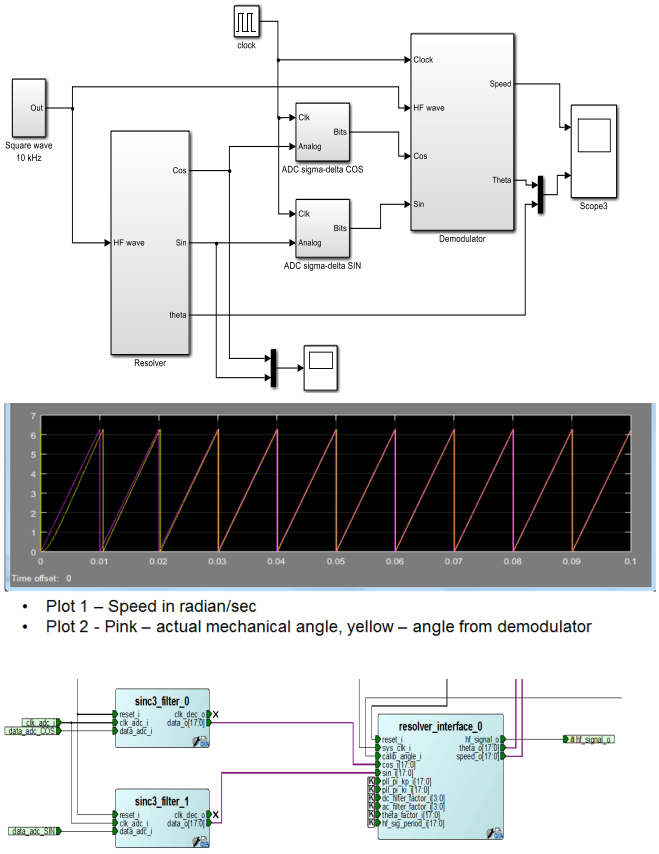
The design flow we've used for developing the new IP blocks involves specification of the inputs and outputs of the required function. Next a top down system design of the required

function, followed by a bottom up development of a working mathematical model; we used Matlab Simulink to design, simulate and fine tune our conceptual design. The next step was to generate the HDL code for our functional block; this can be generated from Simulink or coded separately. The HDL code can then be imported into Libero SOC Smart Design where it can be integrated with the existing IP blocks to create the total device model. After this point, the design is system tested with hardware and compared with Matlab results. The overall performance of the hardware is verified to meet the specifications.

Table 2: Design Flow for IP Block Development

- Determine block inputs and outputs
- Specify system requirements
- Develop system mathematical model
- Generate HDL code
- Create hierarchal block
- Simulate at top level
- Test on the hardware

An example of this IP development procedure is demonstrated with the procedure is the development of the resolver and demodulator. An example of the Matlab model is shown below. The blocks within the model can be drilled down to the actual algorithm implementation. The Simulink output shows the shaft angle in radians vs time for a spinning resolver. The implementation of the IP block in Smart Design shows the inputs and outputs as well as variables.



- Plot 1 – Speed in radian/sec
- Plot 2 - Pink – actual mechanical angle, yellow – angle from demodulator

Figure 9: Development of Resolver to digital IP Blocks

Radiation tolerance for this design will be demonstrated by testing for TID to100krad total ionizing dose at approximately 50 rad/sec, ELDRs to 50krad using a enhanced low dose rate of 0.0035 rads/sec and (SEE) single event effects using a fluence of 1 x 10^8 parts/cm and linear energy transfer of approximately 85 MeV/mg-cm^2. [5] [6] Single event latchup (SEL) is measured with the power supply rails adjusted to their maximum voltage levels. Single Event Transients (SET) tests monitor supply rail input currents and regulated output voltages. We also monitor the sensor modulated outputs and driver outputs for glitches and excursions. Cold spared vulnerability to SET is tested with the power rail removed. For Single Event Upset (SEU) we run a scan chain test routine that cyclically monitors the integrity of the latched data. Single Event Functional Interrupts (SEFI) can occur on Power on Reset or UVLO lines that could initiate and erroneous reset.

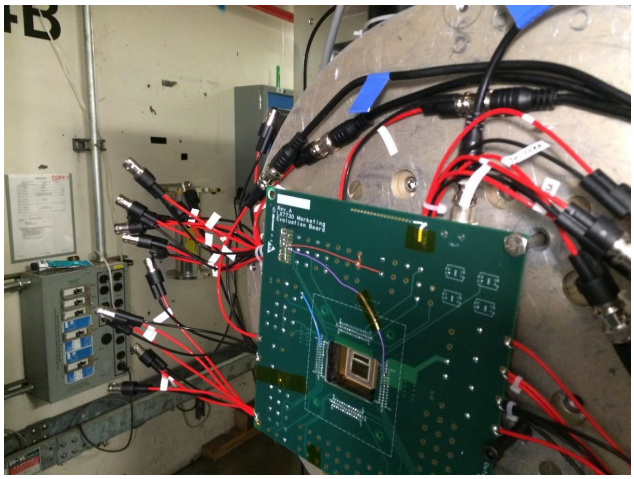


Figure 10: LX7730 in the SEU test set up at UC Berkeley

III. Summary

The development of a radiation tolerant motion control analog front end proposed many challenges for the mixed signal design team at Microsemi. The analog front end was partitioned into two chips, a high voltage BCD process and a low voltage BiCMOS process to take advantage of the different process attributes. The designs were performed using proprietary design guidelines and simulated using proprietary Process Design Kits. Both chips were co-packaged in a 132 lead ceramic quad flat pack with interconnecting bond wires between the dies. New IP blocks were added to the motor control IP library to provide a resolver interface. The parts will undergo radiation tolerance testing for TID, ELDRs and SEE.

IV. References

[1] Microsemi Application Note (AC445). Motor Control using SmartFusion2 and IGLOO2 Devices (July 2015)

[2] LX7720, Rad Hard Spacecraft Power Driver with Rotation and Position Sensing, Datasheet, Microsemi (available on request)

[3] Helmuth Spieler. (1997) Introduction to Radiation-Resistant Semiconductor Devices and Circuits

[4] Max W. Hauser. (1991) Principles of Oversampling A/D Conversion
[5] Richard H. Maurer, et al (2008) Harsh Environments: Space Radiation Environment, Effects, and Mitigation
[6] (2015), Single Event Radiation Report, Microsemi LX7730, 64 Analog Input RAD Tolerant Telemetry Controller, TDRS-0020-4

SEPHY: An Ethernet Physical Layer Transceiver for Space

J. Lopez[a] , P.Reviriego[b], M. Sánchez-Renedo [c], V. Petrovic[d], J.F.Dufour[e] ,J.S.Weil[f]

[a]Arquimea Ingenieria S.L.U, Spain
[b]Universidad Nebrija, Spain
[c]Thales Alenia Space, Spain
[d]IHP microelectronics, Germany
[e]TTT Computerterchnik AG, Austria
[f]Atmel, France

jlopez@arquimea.com

previrie@nebrija.es

manuel.sanchez@thalesaleniaspace.com

petrovic@ihp-microelectronics.com

jean-francois.dufour@tttech.com

Jean-sebastien.Weil@atmel.com

Abstract

Since its development, Ethernet has experienced an impressive growth and has become the dominant technology for wired local area networks. It has also more recently expanded beyond computer networks to cover also industrial and automotive networks. This adoption is driven by the lower costs enabled by reusing existing technology. For critical applications, Ethernet has to be extended to ensure timely and reliable delivery of frames. A number of technologies that can solve the reliability and real time issues have been proposed, for example Time Triggered Ethernet (TTE). Space systems are an example of critical applications and Ethernet has been used in some missions like NASA´s Orion and in launchers. However, there is an additional problem in space applications that has so far prevented a wider adoption of Ethernet. Electronic circuits that operate in space are exposed to radiation that causes errors and make most commercial devices not suitable for space missions. This means that special components have to be designed for space use. For Ethernet, most components like switches or Medium Access Controllers (MACs) are purely digital. There is however one exception, the physical layer transceivers (PHYs) that are by nature mixed-signal devices. The availability of rad-hard Ethernet PHYs qualified for space use is crucial to enable the widespread adoption of Ethernet in space. This paper presents the options for a space Ethernet PHY and the SEPHY project that is currently developing a 10/100 Mb/s European Ethernet transceiver for space.

I. Options for a Space Ethernet PHY

The IEEE 802.3 standard defines many PHYs covering different transmission media and speeds. The most commonly used media in Ethernet are Unshielded Twisted Pairs (UTP). Assuming that the space PHY will use UTP, the IEEE 802.3 standard provides several alternatives. The most relevant ones are: 10BASE-T defined in IEEE 802.3i , 100BASE-TX defined in IEEE 802.3u, 1000BASE-T defined in IEEE 802.3ab and 10GBASE-T defined in IEEE 802.3an. Each of those standards provides a 10x speed increase over the previous one, starting with the 10 Mb/s of 10BASE-T. From a performance point of view, the best would be to select the highest speed PHY for rad-hard implementation. However, there are other factors that should be considered when making a decision. As the speed increases, so does the complexity of the PHY. For example, 10GBASE-T PHYs are currently manufactured in 40 or 28 nm technologies and consume several watts. Implementing that PHY on the older nodes qualified for space use will most likely not be feasible. The development cost also increases with speed. Therefore, the selection of the PHY standards to implement for the space market needs shall weight both the speed and the cost/complexity.

The first standards (10BASE-T and 100BASE-TX) use only two pairs in half duplex mode. Therefore, there is no echo and no far-end crosstalk. This greatly simplifies the transceiver design. For 100BASE-TX the speed increase is achieved by using a larger transmission frequency and number of levels. In any case both standards can be implemented with a moderate cost on an old technology node. On the other hand, the 1000BASE-T and 10GBASE-T standards use the four pairs in full duplex. This means that the receiver on each pair needs to cancel the echo and the crosstalk from the other three pairs. Additionally, these two

standards incorporate a more sophisticated coding scheme (Trellis Code Modulation in the first case and Multilevel Coset Coding in the second) that need complex decoders. This makes the implementation of the transceiver a challenging task.

II. A European Ethernet transceiver for space: SEPHY

The Space Ethernet PHYsical layer transceiver (SEPHY) project funded by the European Union Horizon 2020 research program, is currently developing a radiation hardened PHY. The availability of a European PHY is key to ensure that access to the PHY is not restricted by the United States International Traffic in Arms Regulation (ITAR) and the Export Administration Regulation (EAR), and as a consequence, the non-dependence for the European space industry is guaranteed. The goal of the project is to deliver a production-worth PHY in 2017.

The technology selected to implement the SEPHY device is Atmel´s 150 nm Silicon On Insulator (SOI), as it provides a sufficient level of radiation tolerance that qualifies it for space applications. It is also the same technology for which other European Ethernet components are being developed in the FLPP3 Time-trigered Ethernet Space ASIC project.

The project consortium is formed by different European companies and research centers led by Arquimea that will develop the analog components. IHP will focus on the digital design and Universidad Antonio de Nebrija on the verification. Atmel will be in charge of the fabrication of the integrated circuits. Finally, TTTech and Thales Alenia Space Spain will integrate and test the silicon prototypes on a network and perform also radiation testing.

The project targets the implementation of the 10BASE-T and 100BASE-TX standards. This will provide 10Mb/s and 100Mb/s connectivity in space systems. This compares to the solutions currently used in the space domain like the Mil-Std-1553B (low data rate, large cable length) or SpaceWire (high data rate, short cable length). The proposed transceiver will meet the cable length (100m) and data transfer (100Mbps) requirements not only for launchers applications where cable length is the main constraint but also for the onboard communication requirements where high data rate is required. Those standards can be likewise implemented with a reasonable cost and provide a solution to the industry needs in the short term. The development of a 1000BASE-T PHY would imply much larger cost, time and risk and could jeopardize the adoption of Ethernet. Additionally, starting with lower speeds gives the opportunity to the new standards being developed to mature potentially providing more choices for the second generation of SEPHY. In fact, the project also includes a roadmap activity to identify the best alternative for a second generation of SEPHYs. This will target at least 1Gb/s and its feasibility will also be studied and linked to the future technology nodes planned for space devices.

III. Acknowledgements

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No.64024.

Radiation Tolerant CAN Transceiver for Space

R.J.E. Jansen[1], S. Lindner[2], G. Furano[1], C. Boatella-Polo[1] and B. Glass[1]

[1]European Space and Technology Centre, Noordwijk, The Netherlands
[2]Ecole Polytechnique Fédérale de Lausanne, Lausanne, Switzerland

Abstract – **To fully exploit the advantages of the CAN bus for space a radiation tolerant CAN transceiver on a space ASIC technology is required to realize the integration of the interface and application in a single integrated circuit. The feasibility of realising a CAN interface in a standard digital radiation tolerant CMOS technology has been investigated. The lack of high-voltage devices and high current diodes as well as the low 3.3V operating voltage of the process makes the compliance to the CAN bus severe -2V to 7V common-mode range and -3V to 16V failure tolerance voltage difficult to realise. However by spreading the bus voltage over several transistors and monitoring the bus voltage as well as current, failsafe operation can be realised. The architecture of such a CAN transceiver has been realised and implemented in the DARE180U technology. The transceiver has been electrically and radiation tested and found to be compliant to the space CAN standard. The radiation tests demonstrated a low cross-section for both the receiver and transmitter and demonstrated voltage tolerance up to 16V.**

Keywords—CAN, wireline, bus, transceiver, high-voltage circuit, voltage extension, CMOS,space, radiation.

I. INTRODUCTION

In the latest years a trend towards modularity, reuse and versatility of on board avionics is accelerating. As a consequence, most of the analogue acquisition electronics are "pushed away" from the On Board Computer (OBC) and treated as much as possible at peripheral unit's level. We can foresee future systems where the use of 'legacy' discrete spacecraft interfaces as described in the ECCS-E-ST-50-14C standard [1], like discrete telemetry, PPS as well as most of the direct ON/OFF commands are replaced by the CAN bus.

This makes extensive use of CAN bus interface capabilities, like in modern automotive powertrain systems or distributed industrial controls, possible. The exploited capabilities are:

- High availability: if a control unit fails, the rest of the system must continue to be functional as far as possible in order to exchange information.
- High data density: all control units have the same information status at all times. This means there is no difference in data between the control units. In case of faults anywhere in the system, all the connected users can be informed with equal certainty.

Since the transmission of a CAN message may be initiated by any node of a system (multi-master capability) as soon as the bus is idle, any node of the system may exchange information with any other node. This feature is very important because it very efficiently supports event-oriented message transmission.

II. CAN FOR SPACE

Recognizing CAN maturity and popularity, several European space missions have already adopted the CAN Bus on their spacecrafts, subsystems or payloads. So far the benefits of CAN bus have been mostly exploited in payload busses, due to the limited availability of recurrent units (like AOCS sensors) mounting CAN interface.

These experiences have prompted ESA to drive a standardization process resulting in recommendations to extend the CAN bus and CANOpen specification to cover aspects that are required to satisfy special needs that have been identified as being commonly required on-board spacecraft.

The very extensive experience of the use of CAN bus in terrestrial applications, such as automobiles and factory process control, often in applications that have demanding safety and reliability requirements, and operate in hostile environments that have similarities to spacecraft on-board applications, have been taken into account when issuing the standard for the use of the CAN bus in space, ECSS-E-ST-50-15C [2]. It baselines the ISO 11898 Physical layer as preferred solution for space-borne CAN networks.

The availability of Low Voltage Rad-Hard CAN transceiver will allow more future mission to benefit from the additional features provided by CAN, furthermore reducing European dependence on interface drivers (RS-485, MIL-1553) coming from US manufacturers.

Given that the number of nodes that can be supported by the CAN bus and sub-branches is a ten to hundredfold larger than for the MIL-BUS-1553, the customary separation between transceiver and application integrated circuit may not longer convenient from cost and application printed circuit board area considerations. Therefore an integrated circuit with both application circuit and CAN interface has to be contemplated.

The CAN bus, as defined by the physical layer standard ISO 11898-2 [3], consists of a 120 Ohm CAN H and L differential bus that is terminated at both ends by 120 Ohm onto which the multiple CAN node transceivers are attached. The bus knows two states "recessive" and "dominant" through which communication between the nodes takes place. The

recessive state has both lines around a 2.5V potential, while for the dominant state the differential voltage between the lines is increased to above 1.5V. Common-mode variations on the CAN H and L lines are specified to range from -2V to 7V. In addition during a fault condition the lines could be shorted to supply or ground and thus extend the input voltage range of the H and L CAN ports, for which the transceiver should operate from -3V to 16V. For proper operation of the bus the H and L input impedance should be less than 10kOhm and match within 3%.

The application circuit attached to the interface dictates a nominal supply voltage of 3.3V and for space should ensure fail-safe operation. The latter implies that in case of a failure like a short or open of the CAN H and L lines, no failure propagation should take place. This could occur either through the erroneous reception or transmission of data in case of an open circuit, the burn-out of the driver in the case of a short to ground or the reverse powering of the integrated circuit through the CAN ports for shorts to higher supply voltages. Therefore the architecture of the CAN transceiver on the integrated circuit should not only comply to the CAN standard in radiation environment, but should also guard against failure propagation. These and additional constraints on the operation of the CAN bus in space are stipulated in the space standard [2].

In the following sections (i) the CAN transceiver architecture is presented, (ii) the implementation of the transceiver circuit is discussed, (iii) the electrical measurement results on the CAN transceiver are shown and (iv) the radiation test results on the CAN transceiver presented.

I. ARCHITECTURE

A. Technology

The fail-safe operation of the CAN transceiver requires tolerance to high voltages and the prevention of reverse powering through the bus ports. The customary solution to these requirements is through the selection of a power integrated circuit technology that supports high voltage transistors and high current diodes. The former ensures high voltage tolerance, while the latter operation at 3.3V without reverse powering. For the commercially available devices the most typical implementation for the driver are shown in Figure 1. The high voltage transistor ensures tolerance to the high common-mode voltage range and shorts to higher supply voltages. The high current diodes ensure that the 1.5V differential voltage can be achieved in the dominant state in presence of a double diode voltage drop from a minimum 3V supply.

For space digital CMOS integrated circuit technologies are well established and suitable for the space applications at hand. The availability of high voltage transistors and high current diodes is less common for space integrated technologies and should therefore not be relied upon in the realisation of a CAN transceiver for space. As baseline the DARE180U technology is chosen to demonstrate that the developed CAN transceiver can be realized on most comparable space technologies.

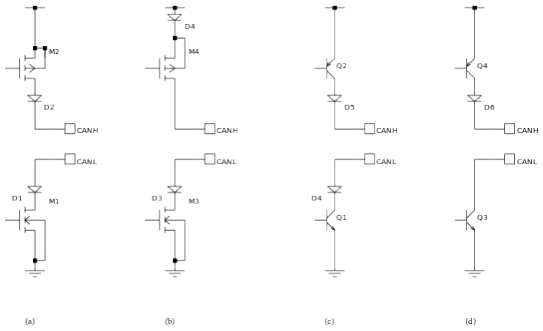


Figure 1. Commercial Transmitter Implementations

B. Architecture

The high voltage tolerance is realised in the selected technology through the stacking of transistor floating in their well such that each of them remains within it safe operating voltage range. The implementation of the driver circuit is further discussed in section II.

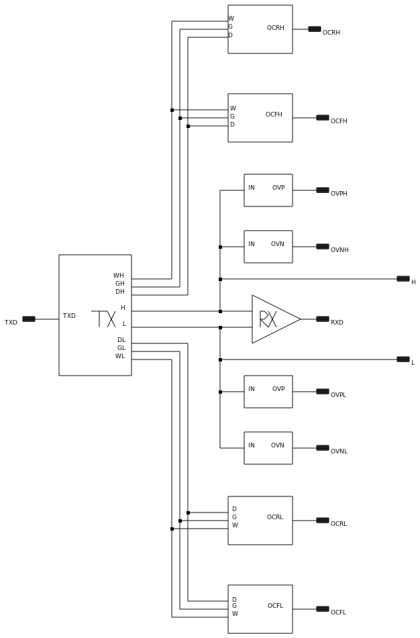


Figure 2. CAN Transceiver Architecture showing the transmitter, receiver and protection circuits for over-current in the forward as well as the reverse direction and for over-voltage conditions.

The fail-safe operation of the CAN driver and receiver requires additional support circuitry that detects the existence of open and shorts on the CAN bus lines, such as to protect the operation of the CAN transceiver. In particular the driver has to be protected against (i) reverse leakage and powering, (ii) high currents and (iii) over-voltages. This can be realised with the reverse current, over-current and over-voltage detectors as shown in Figure 2.

While these detectors monitor and protect the CAN driver from shorts, they can not completely determine the state of the CAN bus. In particular the existence of open circuits is not detected. For these the bus differential voltage and transceiver port currents have to be sampled at the end of a dominant

transmission period. In particular the bus differential voltage, CAN H and L port undercurrent as well as a CAN H and L port current imbalance has to be detected.

The complete state of the CAN bus can now be determined from these 8 detection measures; the H and L port forward and reverse over-current detectors, the H and L port over-voltage detectors, the H and L under-current detector, the H and L sampled current unbalance detector and the H and L bus sampled voltage differential voltage.

II. IMPLEMENTATION

A. Receiver

For the receiver the large input range from 7V to -2V must be compressed into a smaller 3V supply voltage range, with the removal of the common-mode signal. Detection of the dominant bus state should occur for differential bus voltages above 1.2V, while the recessive state is identified for differential bus voltages below 500mV. For a differential threshold voltage of 900mV and 50mV hysteresis the receiver would be compliant to the standard. In reducing the signal input range, the signal to noise ratio should not be compromised in order to maintain the high noise and spurious immunity figures.

B. Transmitter

With only a limited 3.6V source to drain, source to gate, gate to drain and gate to well voltage allowed in a Mixed-Mode 180nm CMOS technology with 350nm devices, the output driver devices have to be stacked to limit the voltages across its terminals. The driver output stage is shown in Figure 3. The resistor string ensures that in the recessive state the voltage across the devices is always less than 3.6V, irrespective of the CAN H or CAN L port voltage. The output stage specific pre-driver is not shown in Figure 3 and will be the subject of future publication [4].

Reverse leakage in the recessive state is limited by sharing the wells between pairs of devices near the port and biasing it from the mid voltage via a resistor. The resistor ensures that for port voltages outside the supply voltage range no excessive leakage occurs through the forward bias wells. With this construction the CAN H bus line can be lifted above the supply rail and the CAN L bus line below ground level.

Given the recessive state port voltage levels between 2V and 3V, the minimum supply voltage level feasible is 3.3V, with a minimum voltage of 3.0V and maximum of 3.6V. For this voltage the minimum differential voltage between the CAN H and L ports in the dominant state should be 1.5V over all the temperature, voltage and process manufacturing conditions.

The minimum CAN H port voltage should according to the space CAN standard [1] should be 2.75V. Given the minimum supply voltage of 3.0V, the lower mobility of the PMOS transistors and that ideally the PMOS pull-up and NMOS pull-down string should be as much as possible symmetrical to realize impedance matching, a minimum 2.35V voltage appears feasible. Commercial 3.3V CAN transceiver devices indicate a minimum of 2.45V.

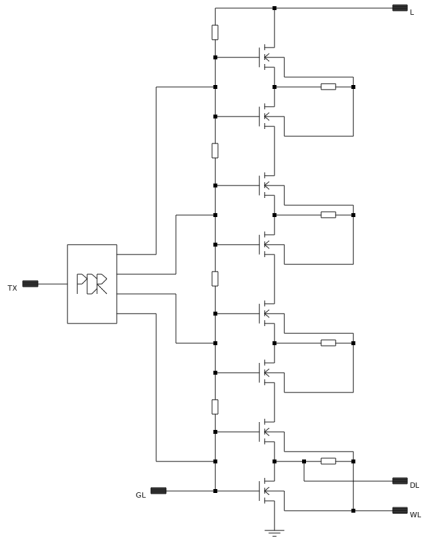


Figure 3. CAN Transmitter

The choice of the recessive voltage level and of the individual CAN_H and CAN L port voltage in the dominant state should take EMC issues into account. Minimum EMC emissions occur when equal voltage swings in opposite directions are achieved for the CANH and CANL ports. The recessive voltage levels should be within the 2V to 3V range to realize compatibility with older devices and prevent too large a DC current to flow between the nodes at different recessive voltages. Striving for an equal voltage swing for both CAN H and CAN L port of 750mV, this leads to the choice of the recessive port voltage around voltage 2.1V, a dominant CAN H port voltage of 2.85V and CAN L port voltage of 1.35V. However the inclusion of margin against manufacturing variations, supply voltage, temperature and the constraint to keep the port impedances equal to within 3%, leads us to the following choice of target port voltages; recessive port voltage 2.2V, dominant CAN H port voltage 2.75V and CAN L port voltage 750mV, with a dominant differential voltage of 1.9V.

C. Forward over-current detector

In case the CAN H or L port is shorted to ground or supply too large a current can flow in the dominant state through the transmitter driver circuit, which could damage the integrated circuit through over-heating. To circumvent this problem the current through the driver can be measured and compared with the acceptable maximum current. For the CAN H port the current is measured by applying the same drain, gate and drain voltages to a smaller copy of the transistor used in the driver of the transmitter and measuring the current. The implemented circuit is shown in Figure 4. For the CAN L port a complementary circuit is implemented to detect over-current due to shorts of the CAN L port to positive (up to 16V), supply voltages.

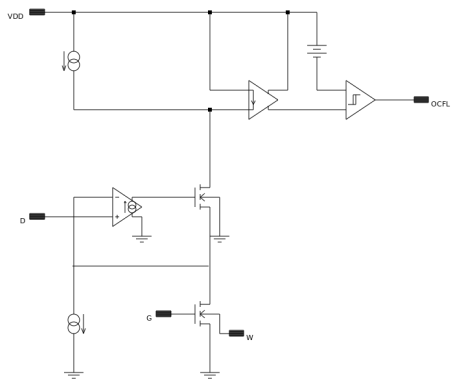


Figure 4. Forward CAN L driver over-current detection circuit

D. Reverse over-current detector

As for the forward over-current detector a large current can flow through the transistor of the driver of the transmitter in the dominant state when the CAN H port is shorted to a higher (up to 16V) supply voltage or the CAN L port is shorted to the lower supply voltage (down to -3V). The current flows than through the transistor in the reverse sense and correspondingly a reverse current copying circuit has been created. Again the drain, gate and source voltage of the transistor of the driver of the transmitter are applied to a smaller version whose current is measured. The circuit is shown schematically in Figure 5.

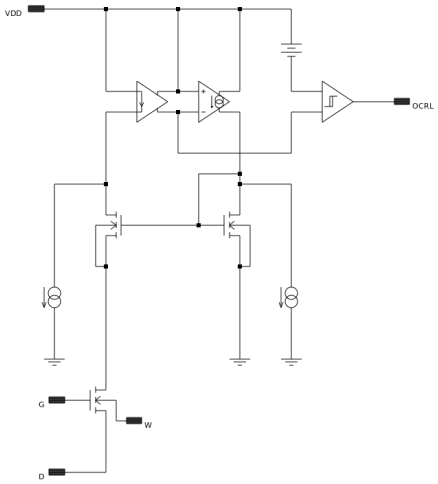


Figure 5. Reverse CAN L driver over-current detection circuit

E. Over-voltage detector

In case that the bus voltage is shorted to a voltage above 16V or below -3V and the transmitter in recessive state, excessive in-rush currents could occur when switching the transmitter to the dominant state. To avoid the occurrence of such events an over-voltage detector is implemented. The circuit is realized with a simple voltage divider attached to each of the state, whose output is compared with a reference voltage.

F. Sampled under-current detector

At the end of the dominant period the current through the H and L port should be about 1.5V/60Ohm = 25mA. Failure to reach this current is indicative of an open or short on the CAN bus lines. The forward current copying circuit is reused for this detector to determine the current in both the H and L ports at the end of the dominant period. In case deviations occur an alarm is raised.

G. Sampled current unbalance detector

Towards the end of the dominant state the current out through the H port should match the current going into the L port. A mismatch between these currents is indicative that a weak short or open circuit exists on the CAN bus. The current unbalance detector re-uses the smaller copy of the port currents to determine the mismatch between the H and L port at the end of the dominant period.

H. Sampled under/over voltage detector

Lastly in the absence of arbitration the CAN bus voltage should be in excess of 1.5V to ensure compliance to the CAN bus standard. Measured voltage above or below indicate the existence of the short or open circuit on the CAN bus lines. This detector samples the voltage at the end of the dominant period and compares it with given threshold voltages. Deviations from the 1.5V trigger an alarm.

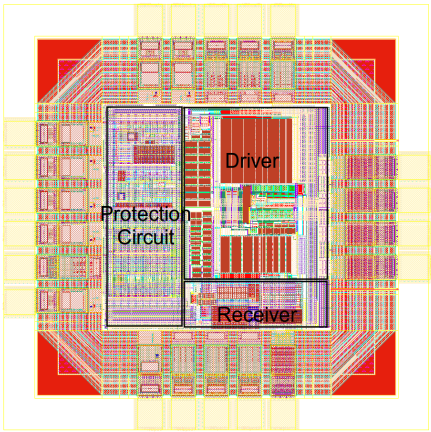


Figure 6: Layout and Chip photo of CAN Transceiver

I. Implementation

The CAN transceiver as described with the forward and reverse over-current and over-voltage detectors for both ports has been realized on DARE180U radiation tolerant technology. The layout of the transceiver and chip photo is shown in Figure 6 and the chip photo in Figure 7. The driver, receiver and transceiver protection circuits are indicated.

III. Measurement Results

The transceiver has been manufactured and tested over temperature and with radiation. Measurements have been carried out to determine the receiver input threshold and hysteresis, the transmitter output levels as well as the transceiver current consumption, port impedance, propagation

delay and high-voltage resilience. Figure 8 shows the CAN transceiver in loop back configuration operating at 200kbit/s, successfully transmitting and receiving.

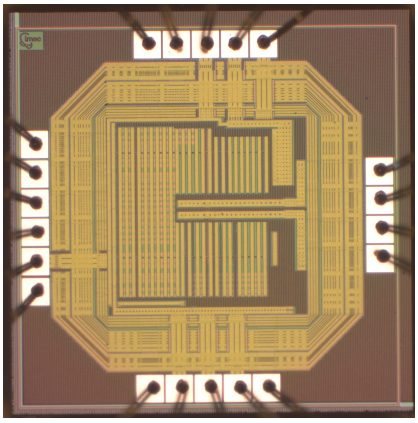


Figure 7: Chip photo of CAN Transceiver

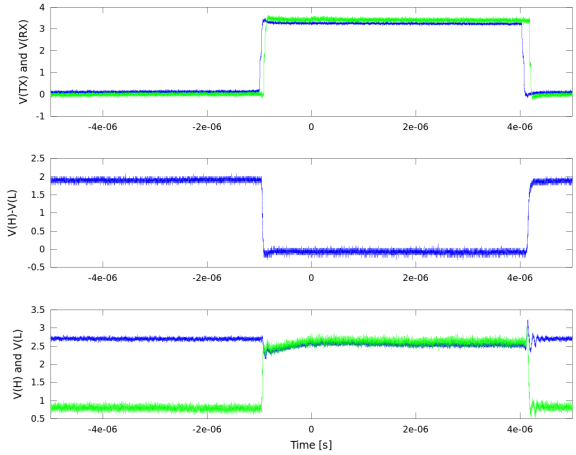


Figure 8 CAN transceiver signals at 200kbit/s

A. *Receiver – Threshold, Hysteresis*

The input receiver threshold levels for recessive to dominant and dominant to recessive transitions have been measured over a supply voltage range from 3.0V to 3.6V and over a temperature range from -55C to 125C. Over the whole supply and temperature range the hysteresis is maintained. The standard imposed transition levels for dominant at 900mV and recessive at 500mV are adhered to.

Description	Symbol	Unit	Min	Typ	Max
RX Threshold: D->R	$V_{diff,TH,RD}$	V	557	684	782
RX Threshold: R->D	$V_{diff,TH,DR}$	V	630	750	843
RX Hysteresis	V_{HYS}	mV	48	66	88

Table 1, Receiver measurement results

B. *Transmitter – Output levels*

The output levels have been measured over a supply voltage range from 3.0V to 3.6V and over a temperature range from -55C to 125C, with as typical condition 25C and 3.3V. The dominant CANH port voltage, and recessive CANH, CANL port voltages are slightly lower than expected, probably due to additional parasitic track resistances.

Description	Symbol	Unit	Min	Typ	Max
CANH Dominant	$V_{CANH,D}$	V	2.340	2.668	3.012
CAN L Dominant	$V_{CANL,R}$	V	0.587	0.693	0.879
CANH Recessive	$V_{CANH,D}$	V	1.991	2.196	2.404
CANL Recessive	$V_{CANL,R}$	V	1.989	2.195	2.403
Dominant Differential	$V_{diff,D}$	V	1.538	1.973	2.379
Recessive Differential	$V_{diff,R}$	V	0.001	0.001	0.001

Table 2, Transmitter measurement results

C. *Transceiver – Current consumption, Port impedance, Propagation delay*

The current consumption has been measured over a supply voltage range from 3.0V to 3.6V and over a temperature range from -55C to 125C, with as typical condition 25C and 3.3V. The port input resistance and capacitance as well as the loop delay has been measured for typical conditions.

Description	Symbol	Unit	Min	Typ	Max
Current Recessive	I_R	mA	2	3	4
Current Dominant	I_D	mA	29	37	45
Input resistance	R_{in}	Ω		22	
Input resistance matching	M_{in}	%			1
Differential input resistance	R_{diff}	Ω		22	
Input capacitance CANH	$C_{in,CANH}$	pF		3.5	
Input capacitance CANL	$C_{in,CANL}$	pF		3.5	
Differential input capacitance	C_{diff}	pF		3.8	
Propagation Delay CMOS -> CAN: R -> D	$t_{TX,RD}$	ns	70	90	115
Propagation Delay CMOS -> CAN: D -> R	$t_{TX,DR}$	ns	30	35	40
Propagation Delay CAN -> CMOS: R -> D	$t_{RX,RD}$	ns	20	25	30
Propagation Delay CAN -> CMOS: D -> R	$t_{RX,DR}$	ns	25	30	45
Propagation Delay Loop R -> D	$t_{LOOP,RD}$	ns	100	120	140
Propagation Delay Loop D -> R	$t_{LOOP,dR}$	ns	60	65	75

Table 3, Transceiver measurement results

D. *Transceiver – High voltage tolerance*

The CANH port has been connected in its recessive state with a 1kΩ resistance to a voltage in excess of 16V for 24 hours without any noticeable changes in post-stress performance.

IV. Radiation Measurement Results

A. *CAN transceiver – Radiation low-voltage SEE Sensitivity*

Low voltage bias radiation tests have been carried out on the CAN transceiver at the LNS facility in Catania. The ions, angle, temperature used as well as the LET and fluence obtained are summarized in table 4.

Ions	Angle [deg]	LET [MeVcm^2/mg]	Fluence [cm^{-2}]	Temp. [C]	Bias [V]
Ar-40	0	6.4	1 x10^7	40	2.1
Kr-84	0	24.0	1 x10^7	40	2.1
Xe-129	0	49.0	1 x10^7	40	2.1
Xe-129	45	72.1	1 x10^7	40	2.1

Table 4: Low-voltage radiation test parameters

The bias voltage is shown in the electrical test set-up diagram in figure 9. It is the voltage of the voltage source that lifts the CANL line via a 1kOhm resistor to the bias supply voltage.

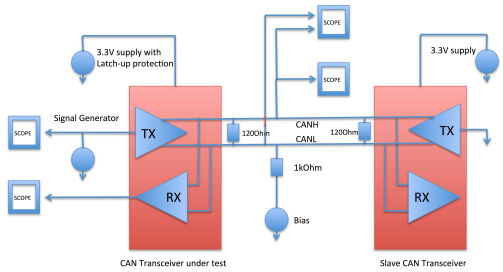


Figure 9 Electrical diagram of the radiation test set-up.

No SEL, SEB and SEGR radiation events have been detected. However radiation SET have been observed in the driver and receiver in the form of single bit errors. The combined receiver and transmitter cross-section are summarized in table 5.

LET [MeVcm^2/mg]	RX+TX cross-section [cm^2]
6.4	4.5 x10^{-7}
24.0	1.5 x10^{-5}
49.0	2.8 x10^{-5}
72.1	3.3 x10^{-5}

Table 5: Combined CAN receiver and driver measured SET radiation cross-section

Further analysis of the data shows that the cross-section for the driver is very much smaller than that of the receiver., such that the performance of the device can be significantly improved with a straight forward TMR implementation of the receiver.

B. *CAN Driver – Radiation high-voltage SEE Sensitivity*

High voltage bias radiation tests have been carried out on the CAN driver at room temperature at the GANIL facility in Caen. The ions, angle, temperature used as well as the LET and fluence obtained are summarized in table 6. A picture of the radiation test-setup is shown in figure 10.

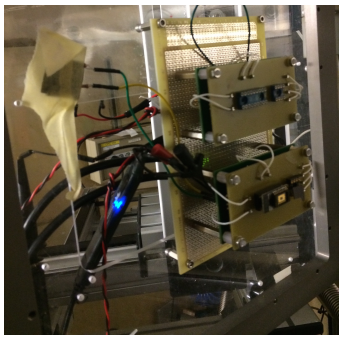


Figure 10 Radiation test set-up.

Ions	Angle [deg]	LET [MeVcm^2/mg]	Fluence [cm^{-2}]	Temp. [C]	Bias [V]
Xe-136	0	61.02	1 x10^7	25	2.0
Xe-136	0	61.02	5 x10^6	25	5.5
Xe-136	0	61.02	5 x10^6	25	7
Xe-136	0	61.02	5 x10^6	25	10
Xe-136	0	61.02	1 x10^7	25	16.0
Xe-136	0	61.02	1 x10^7	25	22.5

Table 6: High-voltage radiation test parameters

The actual CANH and CANL line voltage is lower than the bias voltage due to the input impedance of the driver ports. The measured CANH line voltages in recessive state for the different bias voltages are given in table 7.

Bias [V]	CANH Voltage [V]
2.0	2.2
5.5	4.0
7	6.5
10	9.2
16.0	14.0
22.5	16.0

Table 7. Recorded CANH lines voltages in recessive state as a function of applied bias voltage.

For each of the applied bias voltages no SEB, SEGR and SEL has been observed during the radiation test. It can be concluded that the driver circuit is robust in the presence of radiation. The observed SET on the receiver and driver are shown in figure 11 and 12 respectively. No significant increase of SET cross-section has been observed with increasing port common-mode voltage. Furthermore all SETs observed appear to last only a fraction of the transmission period and consequently are not expected to impact the data communication. Further BER tests should be performed to confirm this behaviour.

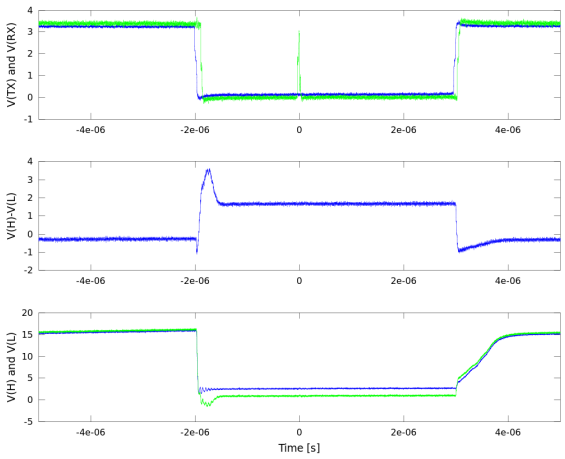


Figure 11 RX SET shown for the CAN transceiver signals at 200kbit/s with a 16V CM signal.

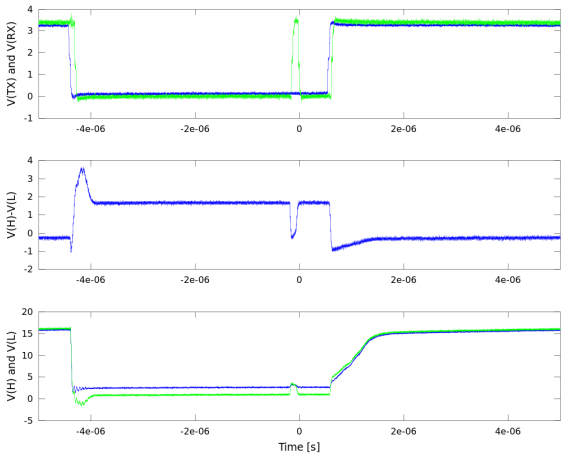


Figure 12 CAN transceiver signals 200kbit/s with a SET in the TX circuit with a 16V CM signal.

V. Conclusion

A CAN transceiver circuit has been implemented in the DARE180U technology with 350nm multi-well MOS transistors and tested over temperature and radiation. Aside from the CANH port output level in the dominant state the implemented CAN transceiver is found to be compliant to the CAN standard and radiation tolerant.

Acknowledgment

The authors would like to thank D. Englisch, F. Guettache, A. Valverde, A. Fernandez-Leon, P. Armbruster, G. Magistrati, F. Tonicello for their continued support in the development, manufacturing and testing of the CAN transceiver.

References

[1] "Spacecraft Discrete Interfaces", ECSS-E-ST-50-14C, http://www.ecss.nl/forums/ecss/dispatch.cgi/standards/showFile/100655/d20081111145033/No/ECSS-E-ST-50-14C(31July2008).pdf

[2] "Road vehicles Controller area network (CAN), Part 2: High-speed medium access unit", International Organisation for Standardisation International Standard, 11898-2, Rev. 1, December 2003.

[3] "CANBus Extension Prototcol", ECSS-E-ST-50-15C, http://www.ecss.nl/forums/ecss/dispatch.cgi/home/showFile/100816/d20131213151003/No/ECSS-E-ST-50-15C-DIR1(13December2013).pdf

[4] R.J.E. Jansen and S. Lindner, "High-Voltage Tolerant Tri-State Driver in Mixed-Mode 180nm Technology " to be published

FPGA Radiation Hardening by Design in CMOS65nm

Q. Croenne, O. Lepape, P Piquet, O. Turkilmaz, D. Haghighitalab

NanoXplore, Burospace Bièvres, France

qcroenne@nanoxpore.com

Abstract

In a radiative environment, when a particle with a given LET (Linear energy transfer in MeV.cm²/mg) hits the substrate of a circuit, it creates electron-hole pairs along its trajectory; this causes current injections between junctions and consequently upsets node voltages resulting in a possible loss of information. Due to technology down-sizing and reduction of supply voltage, circuits become even more sensitive to radiation.

In this work we designed a full custom radiation hardened library for FPGA using ST CMOS 65nm process. In order to improve the reliability of our FPGA, dedicated to the applications in radiative environments, our full custom library has been simulated using IROC software (TFIT). The general methodology and particularly the different steps of a SRAM reliability improvement will be presented.

I. Design Methodology for Hardening

During the hardening process, two kinds of studies were carried out:

- The Single Event Upsets (SEU) that is a direct upset of a sequential logic (SRAM configuration and latches of the Flip Flop (FF)) leading to a bit flip.
- The Single Event Transient (SET)
    - The SET in the clock networks can have 2 effects: jitters that occur at the clock edge and the glitches that occur between the clock edges [1]. These effects can make a bit error to propagate in FF. The design efforts are put on the glitches considering a static clock. In our designs, the jitters are less probable than glitches because the minimum period of a clock is 5ns whereas the SET duration is less than 300ps for a LET less than 58 MeV.cm²/mg in normal incidence as shown in Figure 1. The smallest clock glitch to write in FF is 150ps. Hence the clock glitches longer than 150ps are considered as a SET error.
    - The SET in the reset networks: a glitch longer than 150ps on reset signal can reset a FF storing "1" to "0".

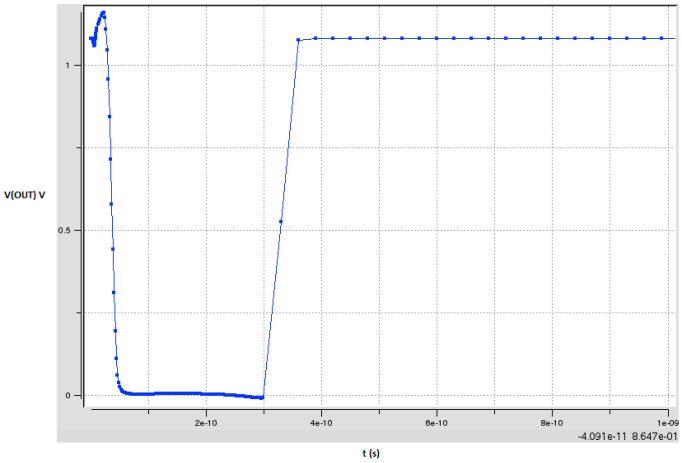


Figure 1: Max duration SET for normal incidence, a LET of 58Mev.cm²/mg

SEU and SET effects are studied and radiation hardening is performed on all the library cells that are sensitive to these effects:

- SEU in configuration memory: configuration memory of our SRAM based FPGA; they are very critical and require a high level of hardening.
- SET on clock/reset buffer and matrix: they propagate clock and asynchronous or synchronous reset into the circuit with a low skew.
- SEU/SET Digital Flip Flop: user register.

For each cell under study, the smallest capacitive load for charge collection in a particle incidence was considered as the worst case.

In order to improve the reliability, design optimizations are made on structure and layout of the library cells. First the structure is hardened by identifying sensitive nodes with a current injection model of particle incidence and then the layout is optimized using TFIT software [2]. TFIT uses a realistic compact model of the technology to calculate current injection and their effect by running electrical simulation for different positions and angles of incidence. By defining an error criterion, TFIT gives the cross section which represents the whole sensitive area (normal to the incidence) through which a particle impact causes a SEU/SET. The simulations are done for normal incidence with a max LET of 58MeV.cm²/mg, 50nm position step, under lowest supply voltage of 1.08V, typical corner and 25°C temperature. Figure 2 shows the sensitive area for normal particle incidence on an unhardened SRAM: for each incidence position TFIT gives

the critical LET for SEU error. The cross section is reduced by putting more distance between sensitive nodes and by bringing the tap closer to them. Other simulations that consider different incidence angles are also done.

II. Step by step hardening of a configuration SRAM in a cell example

For a cell containing a configuration SRAM, different step of hardening were done:

- A first test chip (kipsat3) designed with two version of this cell:
  - with unhardened SRAM
  - with hardened SRAM without layout optimization
- A chip ng_medium designed with a hardened SRAM with layout optimization with TFIT.

At each step the same layout area is kept for this cell.

For each cell TFIT gives the sensitivity map which gives the minimum LET that causes a SEU for normal incidences at each position:

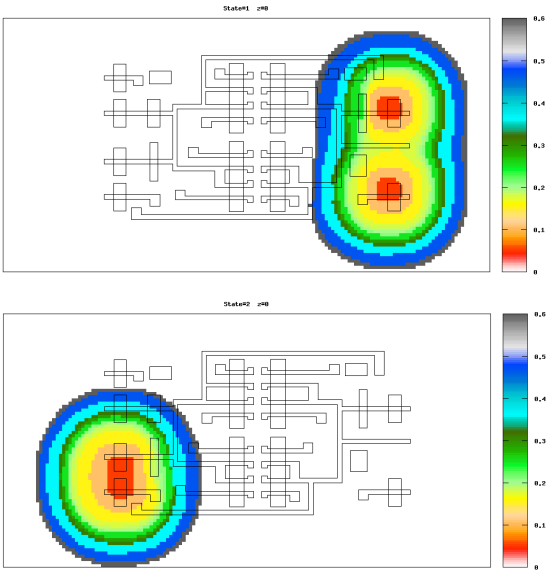
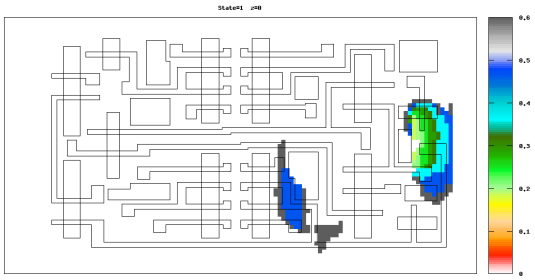


Figure 2: Sensitivity map **unhardened SRAM** LETmin(x,y) pc/um



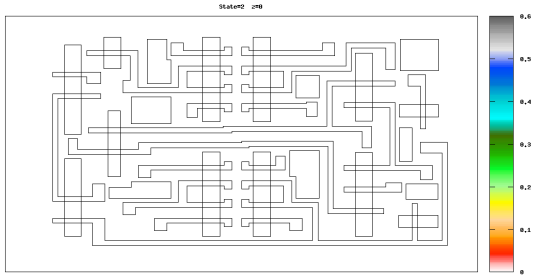


Figure 3: Sensitivity map for **hardened SRAM without layout optimization** LETmin(x,y) pc/um

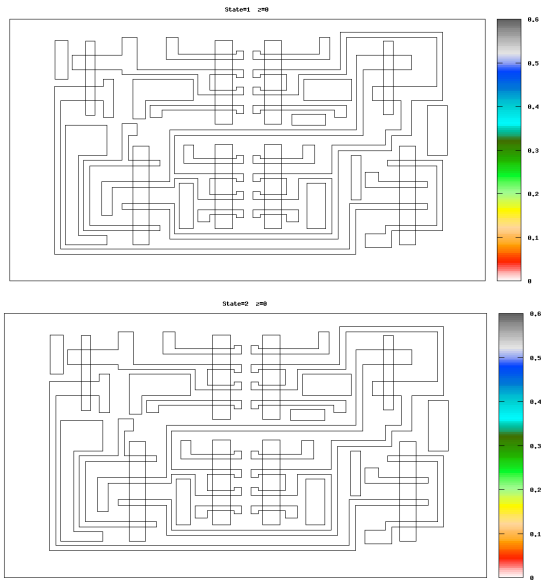


Figure 4: Sensitivity map for **hardened SRAM with layout optimization** LETmin(x,y) pc/um

The unhardened cell contains the N tap and there is a P tap cell that is placed every 3 cell at maximum. The hardened cell without layout optimization has a tap cell placed exactly every 6 cell. Whereas the hardened cell with layout optimization has its own N/P tap.

III. SRAM Structure hardening

A first state of art has been performed using a double exponential current injection model for a particle impact [3] that give an approximation of the current injection through source/bulk or drain/bulk junction (diffusion), as show on the Figure 5.

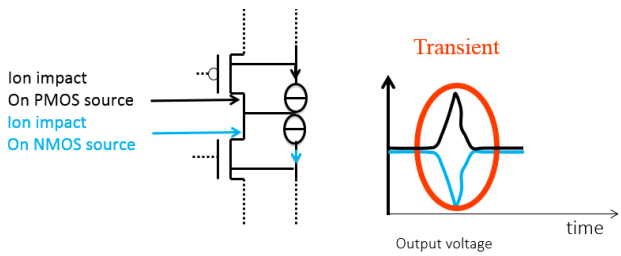


Figure 5: Single event effect on circuit and voltage

The double exponential model [3] calculates the current as follow for a given LET: $I_{rad}(t) = \frac{Q_c}{\tau_d - \tau_r}\left(e^{-\frac{t}{\tau_d}} - e^{-\frac{t}{\tau_r}}\right)$.

With [4]:

τ_r: Collection time of junction ≈ 200ps,

τ_d: Ion track time constant ≈ 50ps,

Qc the total amount of charge created by the ion track:

$Q_c = q\frac{\rho \cdot LET \cdot d}{E_g}$.With d~1um depending on technology, very difficult to be estimated.

Even if this model gives an estimation of the current wave and has difficulties to relate charge and LET, it shows the MOS junction through which a current injection could make a bit flip, and it give the minimum/critical charge that makes SEU. The unhardened structure based on 6T SRAM can have SEU by upsetting only one of the two nodes as show below:

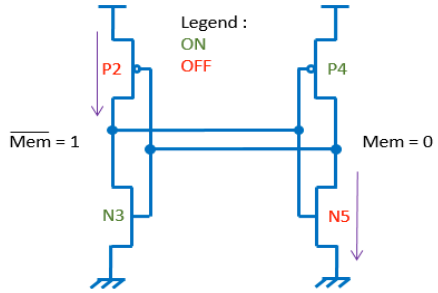


Figure 6: Unhardened SRAM schematic

Table 1: Unhardened SRAM critical charge with double exponential model.

MOS sensitive junction	Critical charge (fC)
P2	21
N5	9

Our hardened SRAM based on the DICE structure [5] can have a bit flip only if the current is injected through several junctions. This has been simulated by considering that the current is divided between the junctions with a sweep on the ratio. Table 2 gives the min critical charge for the injections in junction couples:

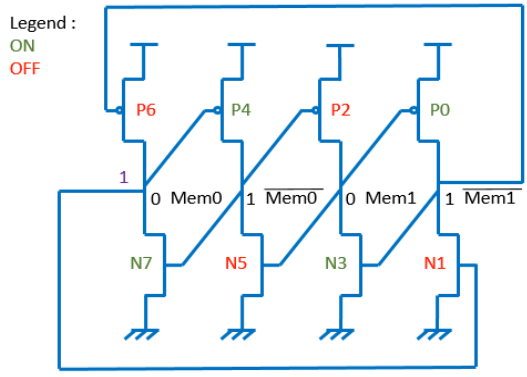


Figure 7: Hardened SRAM critical charge with double exponential model for multiple node injection

Table 2: Hardened SRAM critical charge with double exponential model for multiple node injection

MOS sensitive junction couples	Critical charge (fC)
P2 - P6	42
N5 - N1	21
P6 - N5	11
P2 – N1	11

The DICE structure can only be upset by some of the couples among the P2, P6, N5 and N1 junctions when storing a 0, whereas the other junction helps to retain the data, they will be called retaining junction. These junctions should be placed between sensitive nodes in layout. For the other state this is the opposite : P2, P6, N5 and N1 are the retaining junction whereas some of the couples among the other junctions, are sensitive.

IV. SRAM Layout Optimization

The hardened SRAM is a redundant structure which can only have SEU by upsetting certain diffusions couples depending on the state. In order to optimize the layout for a given state, the distance between the diffusions of each sensitive couple is maximized and the diffusion that help to retain the data, are put between them. The following diagram show that the critical distance is multiplied by four after the layout optimization.

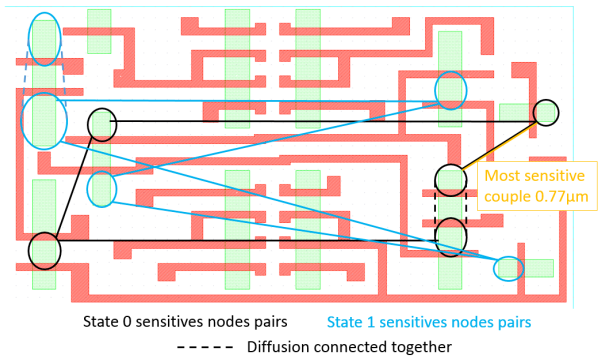


Figure 8: Distance between sensitive and retaining junctions for **hardened structure without layout optimization**

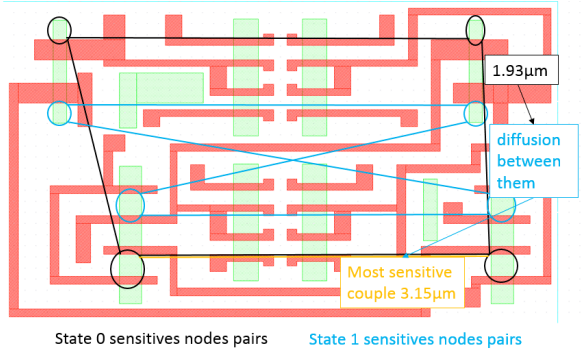


Figure 9: Distance between sensitive and retaining junctions for **hardened structure with layout optimization**

V. Results

A. Simulation

For normal incidence of a particle with a LET of 58MeV.cm²/mg as in Figure 12, the normal cross section is reduced by a factor of 6 by using the hardened structure without layout optimization.

For the hardened structure with layout optimization, the normal cross section is zero. Since the redundant DICE SRAM cross section has a high angular dependency [6], the structure has been simulated for 3 tilt angles (33.6°, 60°, 80.4°) 8 rotation angles with 45° step. For a tilt of 80.4° and a rotation of 180° the hardened structure shows a cross section as in the Figure 10 below. In comparison with the Figure 9, the sensitive area on Figure 10 is on trajectories between the sensitive node couples.

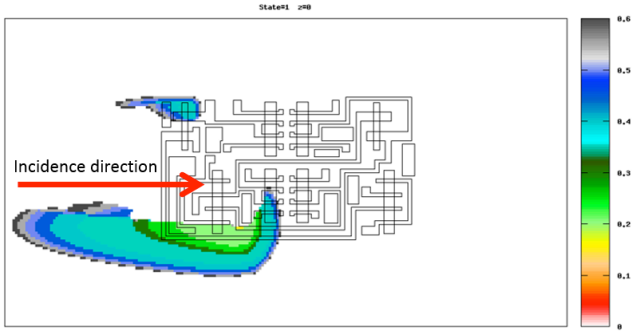


Figure 10: hardened structure with layout optimization: layout projected cross section for state0 tilt 80.4° rot 180

As shown on the Figure 11, for a given LET and position, the solid angle for which the structure is sensitive is reduced by putting distance between sensitive node couples.

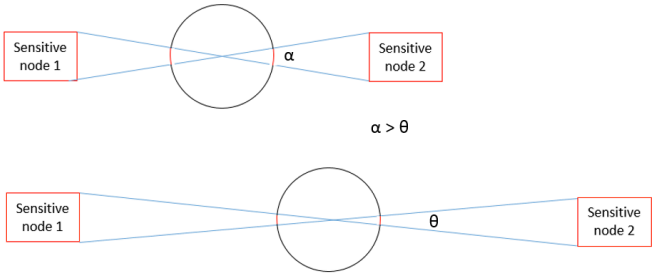


Figure 11: angular cross section dependency with sensitive nodes couple distance

VI. Measurements

The unhardened SRAM and the hardened SRAM were tested. The radiation tests were performed at the Cyclotron Resource Centre located in the Université Catholique de Louvain (UCL) at Louvain-la-Neuve, Belgium. We used their Heavy Ion Irradiation Facility (HIF).

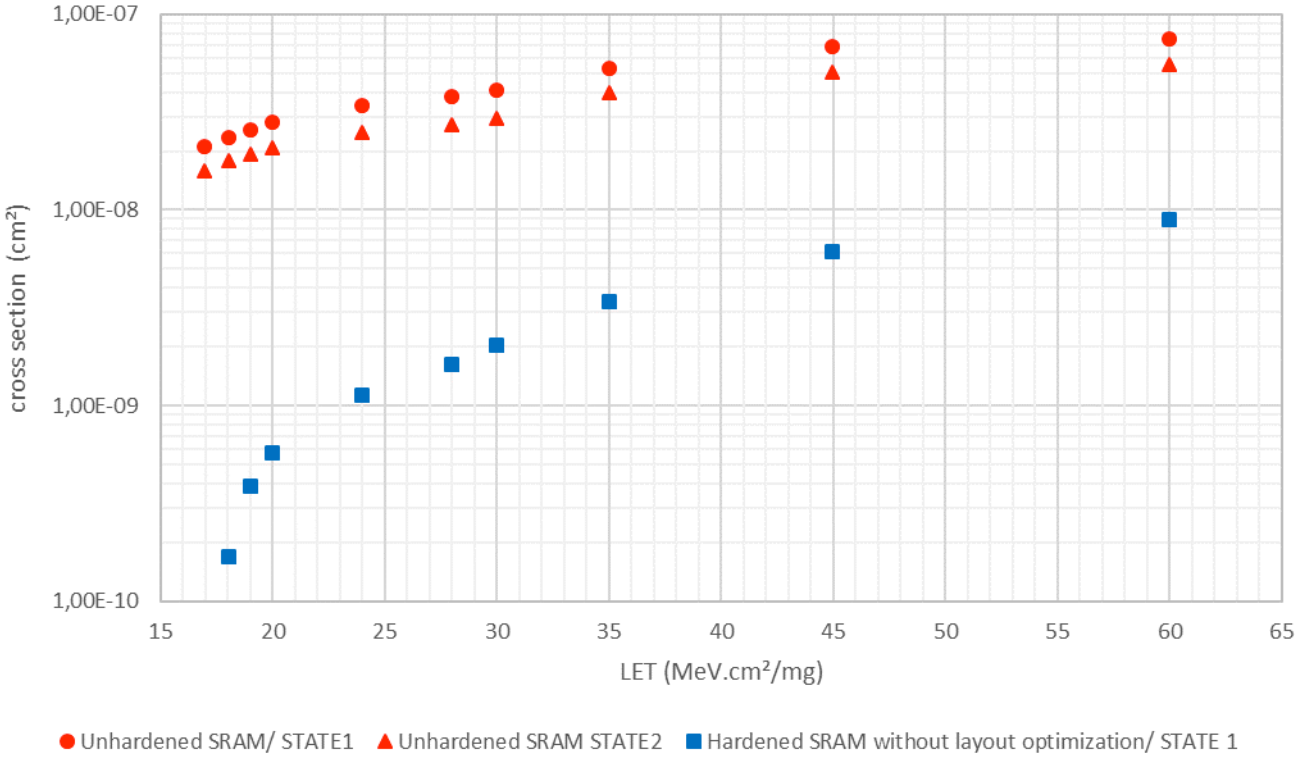


Figure 12: Simulation results of SEU normal cross section

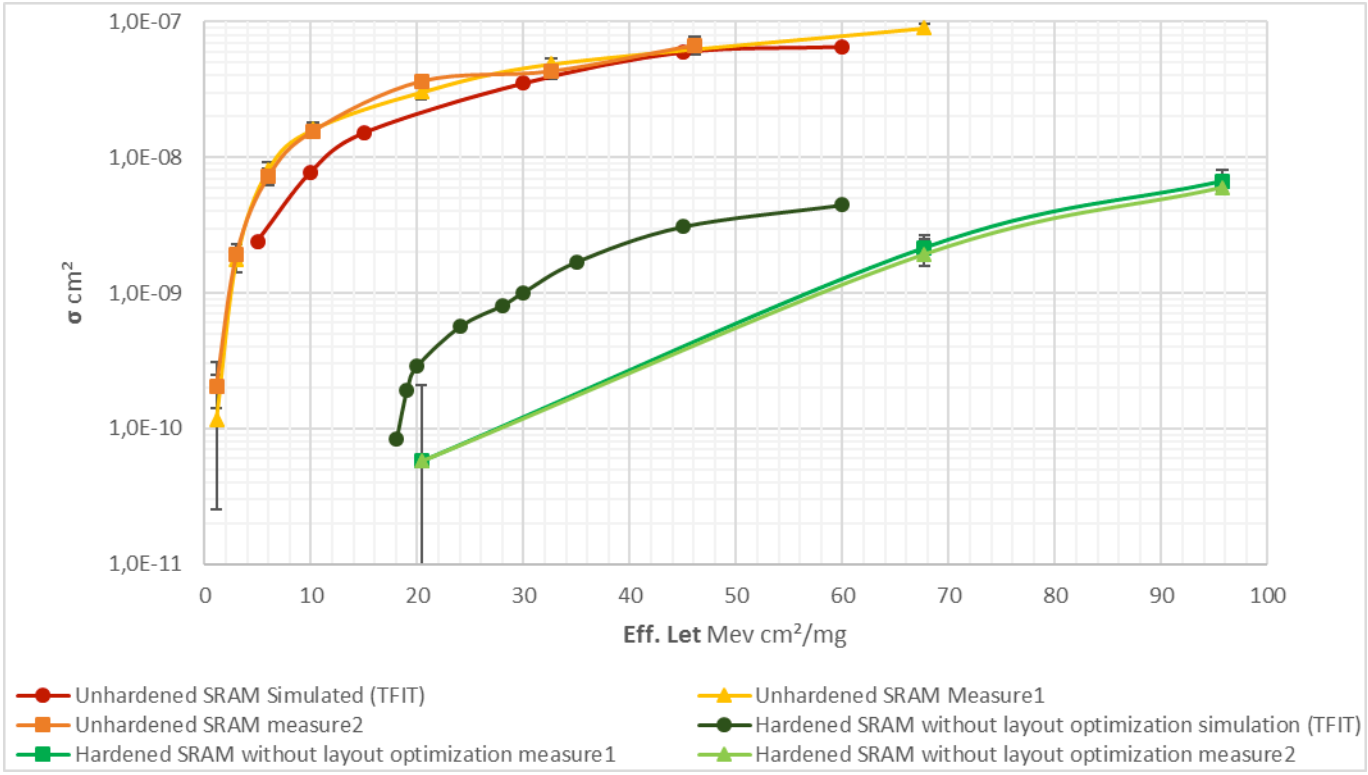


Figure 13: Measure and simulation results of normal cross section (average of the 2 states)

Figure 13 shows a good fitting between measurement and simulation for the 6T unhardened SRAM

At a LET of 60MeV.cm²/mg the two state average simulated cross section is divided by 15 for the hardened structure regarding to the unhardened structure; the reliability improvement is confirmed by the measure that show that the cross-section is divided by 40 for a LET of 67MeV.cm²/mg. The gap between measures is due to dependency with tap distance that can vary in the layout while TFIT considers a tap distance of 2μm for each transistor.

The Hardened SRAM with layout optimization will be measured in the next campaign.

CONCLUSION

In order to improve the reliability of our FPGA in radiative environment, we developed a hardening methodology and applied to one of the configuration SRAM. The first step was on the structure choice. Using the redundant DICE structure, it was measured, during the radiative tests, that the cross section was reduced by more than 40 for LETs between 0 and 60MeV.cm²/mg. An additional improvement is done on the layout by moving the sensitive diffusion couple away from each other and by placing junctions that help retain data, between the sensitive ones. This last improvement will be measured in the next campaign.

REFERENCES

[1] N. Seifert, 16 April 2009, «Radiation-induced clock jitter and race,» *IEEE Reliability physics symposium*.

[2] IROC. [Online]. Available: https://www.iroctech.com/solutions/transistorcell-level-fault-simulation-tools-and-services/.

[3] G. C. Messenger, December 1982, "Collection of charge on junction node from ion tracks," *IEEE Transaction on Nuclear Science, Vol. NS-29, No.6,* p. 2024.

[4] G. C. a. R. K. l. V. Carreno, 1990, «Analog-digital simulation of transient-induced logic errors and upset susceptibility of an advanced control system,» Technical Memo NASA.

[5] F. G. d. Lime, 2000, "Single Event Upset Mitigation techniques for Programmable Devices," Porto Alegre.

[6] L. D. Edmonds, 2011, «Estimates of SEU Rates from Heavy Ions in Devices Exhibiting Dual-Node Susceptibility,» National Aeronautics and Space Administration, Pasadena, California.

AMICSA: Radiation tests of analogue and mixed-signal ICs

ESA Cosmic Vision MF ASICs and IPs Development

E. Pun[a] , F. Serra-Graells[b], J. Madrenas[c], M. García[d], R. Jansen[e], F. Muñoz[f], D. González[a], Michele Dei[b], L. Entrena[d], D. Fernández[c]

[a]ARQUIMEA Ingeniería S.L.U, Madrid, Spain
[b]Instituto de Microelectrónica de Barcelona (IMB-CSIC), Barcelona, Spain
[c]Universitat Politècnica de Catalunya (UPC), Barcelona, Spain
[d]Universidad Carlos III de Madrid (UC3M), Madrid, Spain
[e]ESA, 2200 AG Noordwijk, The Netherlands
[f]Universidad de Sevilla, Seville, Spain

epun@arquimea.com

paco.serra@imb-cnm.csic.es

jordi.madrenas@upc.edu

mgvalder@ing.uc3m.es

richard.jansen@esa.int

fmunoz@gte.esi.us.es

dgonzalez@arquimea.com

michele.dei@imb-cnm.csic.es

entrena@ing.uc3m.es

dfernan@eel.upc.edu

Abstract

In the radiation environment envisaged for the interplanetary mission to Jupiter named Juice, the electronic equipment will require to withstand up to 300krad of Total Ionization Dose. The availability of high performance components that can cope with that requirement is low or non-existent and for that reason ESA funded an activity to create radiation tolerant high-performance mixed-signal IPs.

In the frame of the project two different ASICs where implemented: A rad-hard programmable ∑Δ modulator (CVB-001) which contains four separate ∑Δ modulator and a Rad-hard analogue front-end chip (CVC-001) which contains a Bessel Filter, a Digital to Analogue Converter, a Low Noise Amplifier and a Power amplifier.

Simulation and validation results of those chips and in particular the detailed behaviour of each of the IPs will be presented.

I. Introduction

A set of rad-hard IPs were implemented to provide system designers with the tools needed to build an analogue front-end (from the acquisition of the sensor signal to the data digitalization) for the instruments to be used in Juice missions (i.e. CCD signal conditioner, radiation detector, radiation spectrometer, etc.). These IPs were distributed in two ASICs: CVB001 and CVC001. The former is a rad-hard analogue-to-digital converter (ADC) composed by four ΣΔ modulators (ΣΔM), each of them optimized for a frequency range. The latter includes a filter, a digital-to-analogue converter (DAC), and two kinds of amplifiers: low-noise and power amplifiers. All the IPs were designed to be compatible for interconnection, in order that the signal integrity is maintained all over the possible block chains. Furthermore, all the IPs are configurable, in order to maximize the signal-to-noise and distortion ratio and reduce the power consumption of the overall system. The communications interface to control the ASICs at system level is SPI. Internally, APB protocol is used to read and write the configuration registers.

The considered signal bandwidth is [0.05; 5] MHz and the target resolution is 18 effective bits for the lower frequency limit down to 13 effective bits for the highest.

The IPs design was distributed among a consortium of research groups leaded by a private company:

- ARQUIMEA Engineering (ARQ): in charge of the the coordination, the design of the general purpose IPs, CVB001 and CVC001 system design, system integration, system verification and system validation.
- Microelectronics Institute of Barcelona CSIC (IMB-CSIC): in charge of the mixed signal IPs design.

- Carlos III University of Madrid (UC3M): in charge of the digital design.
- Polytechnic University of Catalonia (UPC): in charge of the amplifiers IPs design.
- University of Seville (USE): in charge of the filter IP design.

CVB001 and CVC001 ASIC were implemented using DARE180 mixed signal library based on UMC180 technology.

A. List of IPs

As mentioned before, the IPs were implemented in two separate ASICS: CVB001 and CVC001. Nevertheless some additional IPs (needed for the basic operation, communication and configuration of the ASICs) were also implemented.

General purpose IPs included in both ASICs are:

- 3.3/1.8V power supply regulator for analogue circuitry (REGA) (designed by ARQ)
- 3.3/1.8V power supply regulator for digital circuitry (REGD) (designed by ARQ)
- SPI/APB communication blocks (SPI) (designed by UC3M)
- High accuracy bandgap voltage reference (BGR) (designed by ARQ)
- Analogue test bus (ATBUS) (designed by ARQ) with 16 channels.
- Digital test bus (DTBUS) (designed by ARQ) with 16 channels.

The Main IPs included in CVB001 are listed below:

- Low-speed single-bit (LSSB) ΣΔ modulator (designed by IMB-CSIC), designed for the [50; 150] kHz signal frequency range.
- High-speed single-bit (HSSB) ΣΔ modulator (designed by IMB-CSIC) designed for the [150; 500] kHz signal frequency range.
- Low-speed multi-bit (LSMB) ΣΔ modulator (designed by IMB-CSIC), designed for the [0.5; 2] MHz signal frequency range.
- High-speed multi-bit (HSMB) ΣΔ modulator (designed by IMB-CSIC), designed for the [2; 5] MHz frequency range.

The Main IPs included in CVC001 are listed below:

- Bessel filter (BF) (designed by USE) with configurable bandwidth (1 and 5 MHz options)
- Low-speed DAC (LSDAC) (designed by IMB)
- Low-noise amplifier (LNA) (designed by UPC) with voltage and trans-impedance programmable amplification modes.
- Power amplifier (PA) (designed by UPC) with voltage, current, trans-impedance and trans-conductance amplification modes.

This paper will be focused on the verification and electrical validation results of three of the developed IPs and in a few configuration modes, for concision. These are: LSSB ΣΔM, LNA (voltage gain) and PA (voltage gain). It shall be noted that radiation testing was not foreseen in the frame of this project.

B. Main specifications

The requirements specification of the IPs was very ambitious and sometimes even above the state of the art, targeting then high performance blocks. The general requirements of the IPs are collected in Tables 1 to 3. Requirements for the ΣΔM modulators, LNA and PA are collected in tables 4 to 6 respectively.

Table 1: Temperature specifications

Parameter	Value	Unit
Operational range	[-10; 85]	°C
Functional range	[-55; 125]	°C

Table 2: Radiation specifications

Parameter	Value	Unit
TID	300	Krad
SEL	80	MeV·cm2/mg
SER	1e-10	errors/bit/day

Table 3: Supply specifications

Parameter	Value	Unit
Supply voltage	[2; 3.6]	V
Supply current	<27	mA

Table 4: ADC main specifications

Parameter	Value	Unit
Signal bandwidth	[0,05; 5]	MHz
Effective resolution	[13; 19]	bits
Consumption	[1; 20]	mA

Table 5: LNA main specifications

Parameter	Value	Unit
Signal bandwidth	[0,05; 5]	MHz
Analogue inputs	[0; 4] / [-0.7; 0.7]	V / mA
THD	[80; 114]	dB
Consumption	4	mA

Table 6: PA main specifications

Parameter	Value	Unit
Signal bandwidth	[0,05; 5]	MHz
Analogue outputs	[0; 4] / [0; 80]	V / mA
Consumption	45	mA

II. ASICs Architecture

A. CVB001 block diagram

The simplified block diagram of the CVB001 ASIC is depicted in figure 1.

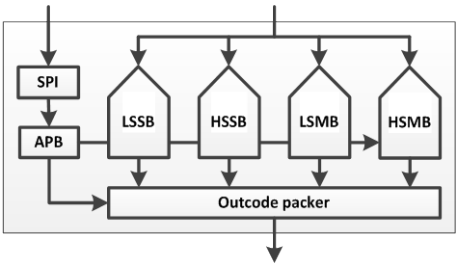


Figure 1: CVB001 block diagram

CVB001 ASIC is composed by four ΣΔ modulators: LSSB, HSSB, LSMB and HSMB. Each one is designed to operate in a non-overlapped signal frequency range: LSSB for [50; 150] kHz, HSSB for [150; 500] kHz, LSMB for [0.5; 2] MHz and HSMB for [2; 5] MHz. Modulators for the two lowest frequency ranges have single-bit output whereas modulators for the highest frequency ranges have a 5-bit multi-bit output. Only one modulator can operate at a time since the output interface is shared and to reduce power consumption. A digital circuitry called 'out-code packer' packages 20 consecutive conversions for the single-bit modulators or 4 consecutive conversions for the multi-bit modulators, in a 20-bit out-code to reduce the frequency of the digital output. CVB001 is controlled and configured through SPI. A 16-channel analogue test bus allows the monitoring of internal critical nets as the output of the regulators and the bandgap reference.

B. CVC001 block diagram

The simplified block diagram of CVC001 ASIC is depicted in figure 2.

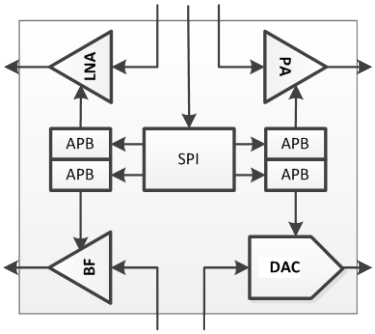


Figure 2: CVC001 block diagram

CVC001 is composed by a Bessel filter a digital-to-analogue converter, a low-noise programmable amplifier and a power amplifier. All the blocks can operate independently and powered-down if their use is not required. CVC001 is controlled and configured through SPI. A 16-channel analogue test bus allows the monitoring of internal critical nets as the output of the regulators and the bandgap reference. Two 16-channel digital test buses allow the monitoring and comparison of internal digital signals to trim clock signals delays and frequencies.

III. RADIATION HARDENING TECHNIQUES

As commented before, the technology used for the development of these IPs is DARE/UMC180 Mix-mode. The DARE digital library was used to implement the digital configuration logic and the modulator output data packers. This library can handle perfectly the project radiation requirements as stated in [1] and [2].

For the analogue part and a few full custom digital cells directly placed on the ΣΔMs dedicated radiation hardening techniques were followed as the ones detailed in [3]

IV. VERIFICATION

Together with the power consumption, a single key parameter has been selected to represent the performance of each IP for convenience. In the case of the LSSB ΣΔM, the effective resolution calculated from the signal-to-noise and distortion ration (SINAD) has been selected. In the case of the amplifiers, their performances is dominated by distortion over noise, hence the total harmonic distortion was the selected parameter. Tables 7 to 9 collect the comparison between the core and the chip simulated performances for the LSSB ΣΔM, LNA and PA respectively.

Table 7: LSSB ΣΔM verification results

Parameter	Core	Chip	Unit
Effective resolution	18	15.5	bits
Consumption	11	15	mA

Table 8: LNA verification results

Parameter	Core	Chip	Unit
THD	88	80	dB
Consumption	24	25	mA

Table 9: PA verification results

Parameter	Core	Chip	Unit
THD	74	68	dB
Consumption	100	110	mA

Degradation in performances is observed at chip level mainly due to the parasitic effects of the pads and package. It shall be noted that in the frame of the activity standard off the shelf packages were envisaged.

V. VALIDATION

A. Tested silicon and packaging

The CVB and CVC chips were fabricated under the IMEC-Europractice service using a MPW run. The die area of both devices is 5x5 mm^2

In addition to these two dies an additional one fabricated under the same service in a mini-ASIC run and ordered directly by IMB-CSIC was also fabricated. This additional die contains an isolated version of the LLSB ΣΔM and was also packaged in the frame of the project for further analysis and comparison between the isolated version of the LLSB modulator and the one sharing silicon with the rest of the modulators (in the CVB chip).

Regarding packages, the CVB chip was packaged using a plastic QFN64 and the CVC a plastic LQFP120. These packages were selected for having the lowest inductance possible from the list of available ones considering the

number of pins required for each case. Finally the LSSB ASIC was encapsulated on a QFN40 package.

Dice microphotographs are depicted in figures 3 to 5.

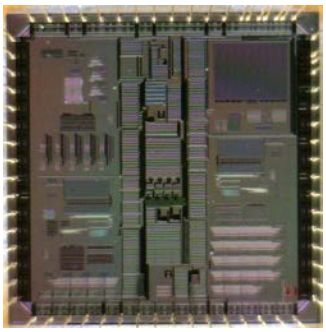


Figure 3: CVB001 die microphotograph

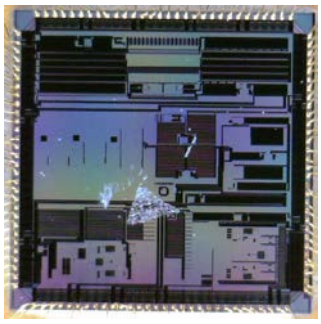


Figure 4: CVC001 die microphotograph

Figure 5: LSSB die microphotograph

B. Measurement boards

A few boards have been designed in the frame of the project to validate the functionality and the performances of the ASICs.

The objective of the CVB&CVC board 1 was to allow functional validation of the ASICs and perform preliminary measurements on each of the IPs. After this stage was completed the design was upgraded evolving in the CVB&CVC board 2. The main objective of the second board was to extend the functional validation capabilities of the setup, to allow the connection of high precision signal sources and to reduce the overall noise floor.

The objective of the LLSB board 1 was to be able to measure the high performance of the modulator. After mounting and debugging, the noise floor measured was around 20dB higher than was required and the distortion 10dB. In any case the measurements performed with this board proved to show the very good behaviour of the LLSB ΣΔM as will be discussed later. The board was upgraded to further improve the overall noise and distortion figures.

Boards are depicted in figures 6 to 9.

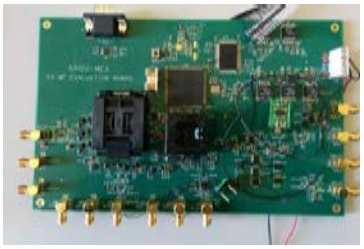


Figure 6: CVB&CVC board 1

Figure 7: CVB&CVC board 2

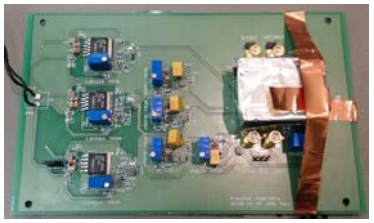


Figure 8: LSSB board 1

Figure 9: LSSB board 2

C. Signal source and measurement equipment

For the [0; 200] kHz range, the analogue input signal was generated with DS360 Standard Research Systems high quality source; for the [0.2; 5] MHz range, BK PRECISION 4064 source was used. The former can achieve 100dB of SNDR but can only go up to 200 kHz; the latter can reach higher frequencies but only achieves 80dB of SNDR. Keysight DSOS204A oscilloscope was used to monitor time domain signal and to perform a quick but moderate accuracy frequency analysis (up to 60dB of SNDR). Analogue Devices EVAL-AD7960FMCZ and EVAL-SDP-CH1Z boards were used to perform high accuracy frequency analysis (up to 90dB of SNDR).

D. Results

A summary of the main features measured on each of the selected IPs is shown in tables 10 to 12.

With regards to the LLSB ΣΔM, as can be seen in the tables, a slight degradation on its performance is observed between the version included in CVB and the standalone one. Additionally, the resolution reached is lower than the one predicted by the core simulations but in line with the chip level verification which indicates that the degradation is probably linked to pad and package limitations. Additional reults of the LLSB modulator can be found in [5].

LNA results indicate a THD lower than expected, which is currently being investigated. The most probable hypothesis is that the degradation is also linked to the influence of pad and package parasitics.

PA results show a very good correlation between verification and validation.

Table 10: LSSB ΣΔM in CVB validation results

Parameter	**Value**	**Unit**
Effective resolution	14	bits
Area	1.325 x 1.485	mm^2
Consumption	16	mA

Table 11: LSSB ΣΔM alone validation results

Parameter	**Value**	**Unit**
Effective resolution	15.5	Bits
Area	1.325 x 1.485	mm^2
Consumption	15	mA

Table 12: LNA validation results

Parameter	**Value**	**Unit**
THD	63	dB
Area	0.995 x 1.07	mm^2
Consumption	25	mA

Table 13: PA validation results

Parameter	**Value**	**Unit**
THD	73	dB
Area	0.61 x 1520	mm^2
Consumption	110	mA

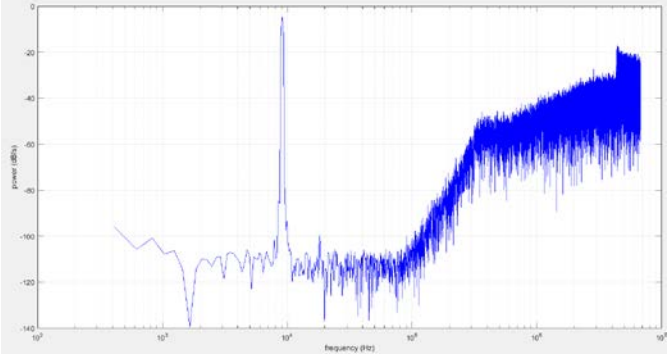


Figure 10: FFT of the LSSB ΣΔM in LSSB board 2

VI. CONCLUSIONS

A set of high performance and highly configurable IPs have been designed, verified and electrically validated in the frame of ESA's Cosmic Vision MF activity showing promising results. A single silicon run was used to implement the designs showing a very good correlation between verification and validation.

Further work on the IPs could tune or adapt performances for particular applications and further testing of the ASICs would allow additional data on all possible configuration modes.

VII. REFERENCES

[1] S.Redant, M. Hollriser (2002). A radiation-tolerant standard-cell library for a commercial deep sub-micron technology. RADECS 2002 procedings.

[2] S.Redant, R. Marec, L. Baguena, E. Liegeon, J. Soucarre, B. Van Thielen, G. Beeckman, P. Ribeiro, A. Fernandez-Leon. B. Glass. (2004). The design against radiation effects (DARE) library. RADECS 2004 procedings.

[3] ESA-ESTEC Data Systems Division/Microelectronics Sextion (2011, December). Space engineering product assurance-Techniques for Radiation Effects Mitigation in ASICs and FPGAs.

[4] Stepan Sutula (2015, November). Low Power High Resolution CMOS Switched Capacitor Delta Sigma Analog to Digital Converters for Sensor Applications. PhD Thesis.

Si and CdTe Detector Readout ASIC in 0.35µm CMOS for Energetic Electron Spectroscopy for Space Application.

I. Introduction

TARANIS (Tool for the Analysis of RAdiation from lightNIng and Sprites) is a microsatellite aimed to atmospheric storms study. It embarks among other instruments IDEE (Instrument Détecteur d'Electron Energétique) which is dedicated to energetic electron characterization in the range from 70keV to 4Mev. To cover such a wide range, two types of detectors are required: Silicon (Si) and Cadmium Telluride (CdTe) based detector for the 70keV to 700keV and for the 300keV to 4MeV respectively. Si detectors are placed in front of CdTe detectors for angle measurement. Although the readout architecture of both detectors are similar, the time constants involved in collection of the charges for Si and CdTe are differents by almost 21 decades (60ns for Si and 3µs for CdTe). Two different readout circuits are thus required. CdTe type channels need to make use of Pole Zero Cancellation (PZC) technique in order not to impede the frequency of operation. Performance of the design has been characterized on a test board as well as interfaced with detectors. Finally, results of its characterized Single Event Latchup (SEL) performance is given.

II. ASIC design

Both type of channel are based on a charge sensitive amplifier (CSA), a CR-RC pulse shaper followed by a peak detector and a 8-bit ADC (analog to digital converter). The ADC design is the same for both channels [1].

A. Si and CdTe Analog Front ends

Si and CdTe channels both make use of a RC CSA for integration of the input charge. The CSA is based on a transconductance amplifier (OTA) with a feedback capacitor Cf to perform the charge integration and a resistor feedback Rf to discharge Cf and to provide a DC path for the detector leakage current. Such a differential approach improves the rejection of common mode external noise. In addition, based on the methodology extensively described in [1], sizing as well as biasing of the transistors are optimized for internal noise and bandwidth performance. The feedback R_f and C_f values depend on the required time constant. Then, in order to improve the Signal-to-Noise Ratio (SNR) and improve the signal amplitude, the CSA output voltage is filtered by a pulse shaper (PS). A first order semi-Gaussian PS (RC-CR bandpass filter) is used as PS for its high-speed response and its active bandpass filtering characteristics.

The relaxation time of the circuit defines the frequency performance of the readout channel. While 1-µs conversion time of the ADC is the limiting criteria for Si channel, time constants of CdTe analog circuit set the limit for CdTe channel. It becomes necessary to eliminate the undershoot created by the 2nd pole of the CSA-PS chain. A PZC circuit is thus implemented by adding an extra resistor Rz in parallel to the pulse shaper derivation circuit (Cd, Rd) as shown in Fig 1.

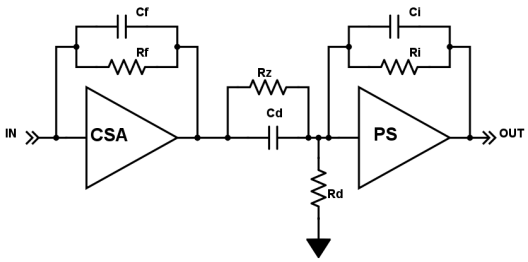


Figure 1: CdTe channel analog Front End simplified schematic

B. Peak detector and 8-bit ADC

At the output of the pulse shaper, the signal amplitude is proportional to the incoming particle energy, a peak detector searches the maximum value of the signal in a track and hold manner. The final value is digitized by an 8-bit SAR ADC.

C. Layout considerations

The circuit has been implemented in AMS 0.35µm HV CMOS technology. This technology has a triple well option allowing isolation of transistors from the bulk. This is an advantage in terms of noise and crosstalk reduction. To further reduce crosstalk, power supply of the analog part of the channel is isolated from the peak detection and ADC. A microphotograph of the chip is shown in Figure 2.

8 CdTe channels and 5 Si channels are integrated in the chip.

III. ASIC characterization

The ASIC (Fig. 2) has been characterized on a test board. A 1-nF injection capacitance driven by a signal generator has been used to generate the input charge. The ASIC input is loaded by a 40-pF capacitance representing the detector.

Noise measurement has been performed by sending 1000 events and standard deviation is computed. ENC of Si is of 3120e- while CdTe ENC is 2335e-, time constant of CdTe PS provides a better filtering of the noise.

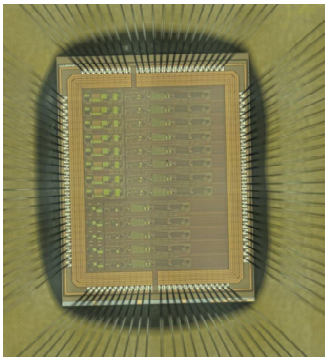


Figure 2: Si and CdTe readout ASIC microphotograph

IV. Interface Test with Si and CdTe detectors

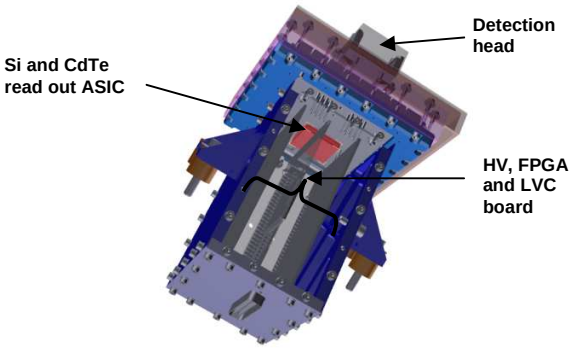


Figure 3: 3D model of the IDEE instrument

The ASIC is mounted in the instrument electronic box (Fig. 3). The electronic box is composed of a High Voltage, a FPGA and a Low Voltage board. The HV board generates the 100 and 300V necessary for Si and CdTe detectors biasing. The FPGA encapsulates the detected energy in the appropriate data frame and the low voltage board takes care of the supply voltage for each electronic board.

The detector head is made of 8 CdTe detectors placed behind a strip of 5 Silicon pixels. The centered Silicon pixel is about 40 times smaller than the others. It will be used alone for the South Atlantic Anomaly crossing that might saturate the instrument otherwise.

The detector head is exposed to a 207Bi source for final characterization of the instrument. The specified resolution of the instrument being 6 bits, only the first 6 bits of ASICs output are being collected by the FPGA. The spectrum of the 207Bi is given below. The source being centered in the middle of the Si detector strip, Si1 and Si3 receive the highest density of particles. Si2 being the smallest detector pixel the probability of having a count is small (Fig. 4).

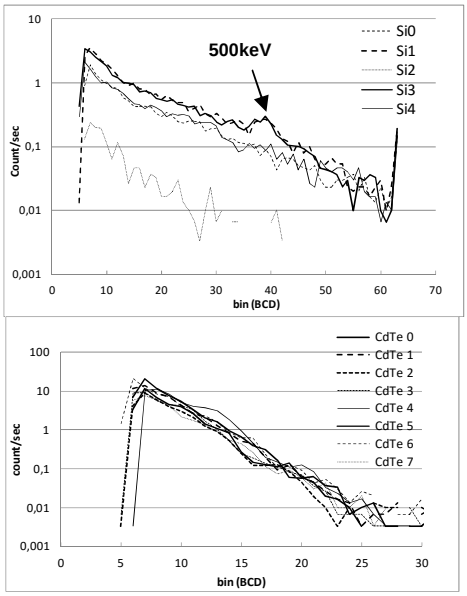


Figure 4: Si and CdTe 207Bi source spectrum

The electron emission around 500keV can be clearly seen on the Si spectrum while in the CdTe spectrum no obvious electron energy can be seen mainly due to obstacles between the source and CdTe detectors in the detection head.

V. Radiation Test

Heavy ion test has been performed at RADEF at University of Jyvaskyla (Finland) using their cyclotron accelerator test facility. Two samples were exposed to krypton ion at a tilt angle of 37°deg and showed a Single Event Latchup (SEL) occurring at a Linear Energy Transfer (LET) level of 40MeV(mg/cm²). An analog de latching circuit on the test board detected the current surge on the chip supply voltage and powered it off. Functionality of the chip has been verified after occurrence of latch up event.

VI. Conclusion

A Si and CdTe detector readout ASIC for Energetic Electron Spectroscopy has been presented, it features a detection range from 70keV to 4MeV. The ENC Si is of 3120e- for Si channel and CdTe ENC is 2335e-. Both are loaded at the input by a 40pF capacitance. It has been tested both on a test board and in the electronic box of the instrument. SEL occurs at a LET of 40Mev(mg/cm²).

VII. References

[1] F. Bouyjou, O. D. Bernal, H. Tap, J.A. Sauvaud and P. Jean, " Low Noise CMOS Analog Front-End Circuit With an 8-bit 1-MS/s ADC for Silicon Sensors for Space Applications," *IEEE Sensors Journal.*, vol. 14, no. 5, pp. 1617-1624, May. 2014.

[2] P. Grybos, R. Szczygiel, " Pole-Zero Cancellation Circuit With Pulse Pile-Up Tracking System for Low Noise Charge-Sensitive Amplifiers " , *IEEE Transaction on Nuclear Science*, vol. 55, no. 1, February 2008.

LVDS: A RAD-HARD Octal 500 Mbps Bus LVDS Repeater for Space

J. Lopez[a] , E. Cordero[b], M. Cirillo[c], R. Dittrich[d] , A. Frouin[a], R. Jansen[d] , D. López[b]

[a]Arquimea Ingenieria S.L.U, Spain
[b]ALTER, Spain
[c]IHP microelectronics, Germany
[d]ESA, Noordwijk, The Netherlands

jlopez@arquimea.com

enrique.cordero@altertechnology.com

cirillo@ihp-microelectronics.com

rok.dittrich@esa.int

afrouin@arquimea.com

richard.jansen@esa.int

demetrio.lopez@altertechnology.com

Abstract

Transmission of large amount of data is extensively used in communication among spacecraft and satellite onboard systems during a mission. LVDS (Low-Voltage Differential Signaling) Drivers and Receivers are key devices to provide means of sending/receiving data along twisted pair cable at very high data-rates with low power and excellent EMI performance. Rad-tolerant and Rad-hard ANSI EIA/TIA 644A complaint LVDS Drivers and Receivers products are essential in an extensive range of space applications. Typical applications with such needs are Space-Wire and clock distribution networks.

The purpose of the paper is to present the characterization results performed on the LVDS Octal repeater developed by ARQUIMEA in the frame of ESA's and ECI's European LVDS Driver Development intended to be used in space applications and built in IHP's 0.25-um BiCMOS process technology.

The key features of the octal LVDS repeater include cold sparing, fail safe, more than 250MHz signaling rate per channel allowing above 500Mbps transfer rates over SpiceWire, 3.3V single power supply, low channel to channel skew, TRI-state output control, extended common mode on LVDS receivers.

I. Electrical Results

A. General

The Electrical Characterization performed by ALTER on the first manufacturing run of the LVDS octal repeater has mostly fulfilled the specific requirements of the project and the generic Requirements of ANSI/TIA/EIA-644-A-2001 which states Electrical Characteristics for LVDS Interface Circuits.

B. Test Set-up

The set-up includes several channels of high precision power sources that allow high stability supply and precision measurement of all DC parameters of the different inputs and outputs. The test bench includes an LVDS generator and a high bandwidth oscilloscope to measure all AC switching characteristics (See Figure 1).

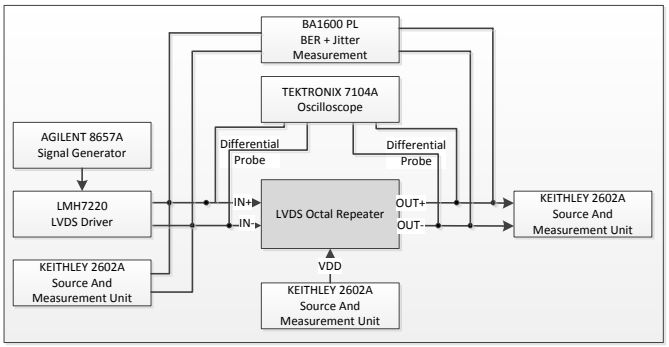


Figure 1: Electrical Characterization Test Set-up

C. Test Board

The Test board uses matched impedance connectors (SMAs) to connect to external test equipment. The signal paths to the connectors are matched in length.

Circuit board layout and stack-up is designed to provide noise-free signals. Ground planes, decoupling, separated high frequency with high level IOs are implemented to minimize unwanted stray noise pickup, feedback and interferences (See Figure 2).

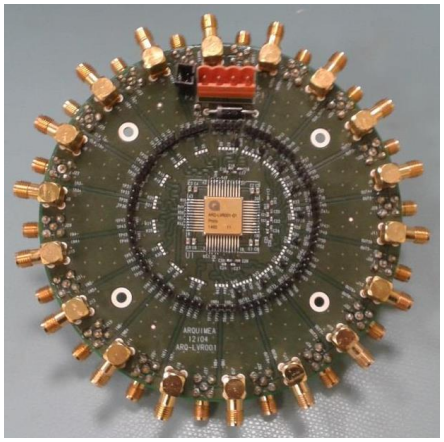


Figure 2: LVDS Octal Repeater Test Board

D. Electrical Parameter deviation

A Non-Compliance-Report has been raised due to the minor deviation on some parameters. This NCR serves as a basis for further improvement of the electrical parameters (See Table1).

Table 1: Electrical Parameter Deviations

Parameters	Description	Measured Value	Spec. Limit
V_{TH}	LVDS Input Voltage Threshold	135mV	<100mV
t_P	Propagation time	5,5ns	<3,5ns
V_{OD}	Differential Output Voltage	565mV @-55ºC only	<453mV
I_{CS} I_{CSOUT} I_{CSIN}	Cold Spare Leakage currents	30uA @25ºC 50uA @125ºC	<20uA
I_{OZ}	Output Tristate Current	15uA	<10uA
J_{RMS}	Jitter rms	20ps	<15ps

II. Radiation Results

A. Total Ionising Dose

1) General

The TID Test was performed by ALTER at RADLAB Facility with a Low Dose Rate of 220 rad(Si)/h up to 300Krad on biased and unbiased samples according to ESCC22900 Standard.

The Octal LVDS repeater did not show relevant degradation of its tested parameters up to 300Krad.

2) Set-up

The samples are located at a calculated distance from the Co60 gamma source to reach the required dose rate in RADLAB Facility as per Figure 3.

Figure 3: TID Set-up

Pre, intermediate and post-radiation electrical measurements are performed on the components with Electrical Characterization set-up in order to detect eventual drifts.

B. Single Event Effects

1) General

The SEE campaign was performed by ALTER at HIF UCL Facility with Bit Error Rate Calculator and Latch-up protection equipment's according to ESCC25100 Standards.

The LVDS octal repeater did not show sensitivity to Latch-up at 25ºC and 65ºC up to 62.5MeV.cm2/mg (higher LET applied with Xe ion). The Component is either not sensitive to SET or SEU up to 20MeV.cm2/mg. At higher LET of 62.5MeV.cm2/mg, 15 bit errors were detected after 1E12 transmitted bits.

2) Set-up

The samples are collocated on the Facility frame for Heavy Ion irradiation as per Figure 4. The frame associated with Peltier Modules allows temperature control in order to apply the worst case conditions for the different type of SEE.

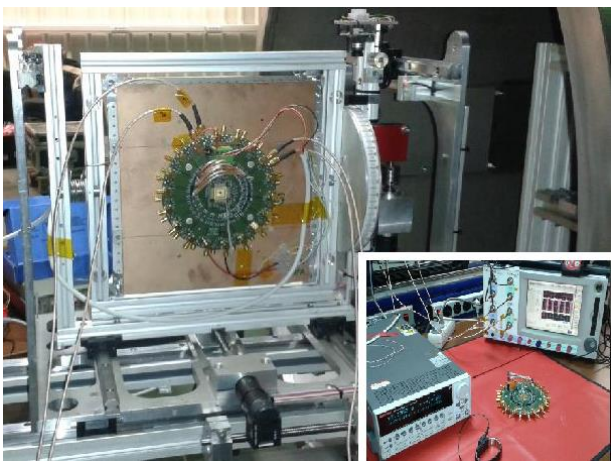


Figure 4: SEE Set-up

During the irradiation, the LVDS Octal Repeater is operating at 200Mbps with all its channels connected in series in order to increase the equivalent number of transmitted Bits.

III. ESD RESULTS

1) General

The ESD Tests were performed by ALTER in-House with their dedicated Test System according to JEDEC Standard (JS-001-2010, JESD22-A115-A and JESD22-C101-C).

The LVDS Octal repeater withstands correctly the applied ESD pulses:

- HBM ESD model up to ±8KV
- MM ESD model up to ±250V.
- CDM ESD model ±500V

After each pulses levels and combination of pins the protection circuits were tested and BER analysis at 500MHz was performed. No relevant degradation was detected.

2) TLP Results on Wafer

Confidence on ESD robustness of the LVDS Octal Repeater was assumed forehand thanks to TLP ESD characterization performed on wafers by IHP on some ESD test structures developed in collaboration with SOFICS. In fact the LVDS ESD test structure did not show degradation up to 7kV (Highest tested Voltage).

IV. FURTHER STEPS

A few design modifications were required in order to improve the deviated electrical parameters. Specific care was necessary for the selection of a qualified CQFP48 package suitable for space.

The Test Board design is also improved in order to ease the test with removable resistors and increase measurement precision with active probes.

The new LVDS Octal Repeater will now follow evaluation testing according to ESCC2269000 at ALTER in order to give sufficient confidence to reach TLR8.

The pros and cons of *in situ* testing – going beyond the test standards

R.E. Sharp[a], J. Hofman[a, b] and J. Haze[b]

[a]Cobham RAD Solutions, 168 Maxwell Avenue, Harwell, Oxfordshire, OX11 0QT, United Kingdom
[b]Brno University of Technology, Technicka 8, Brno, Czech Republic

richard.sharp1@cobham.com

Abstract

This paper discusses the benefits of *in situ* measurement during radiation testing, compared with the common practice of remote measurement at each of a number of total dose steps. An example is drawn from real test data.

I. INTRODUCTION

THE total dose radiation testing of electronic components for use in space environments is frequently carried out according to one of two test standards: either ESCC 22900 [1] published by the European Space Agency or the US Department of Defence Mil-Std-883, method 1019 [2]. Both of these standards are written around the basic concept of alternately making electrical measurements on the components and then irradiating them. Numerous instances have subsequently been noted where this procedure could lead to an erroneous understanding of the response to radiation exhibited by the components being tested. This paper highlights the issues associated with some of those instances and proposes *in situ* testing as an alternative test strategy that, in certain circumstances, can lead to much greater fidelity of the results and higher confidence in the validity of the data gathered.

II. EXISTING TEST STANDARDS

ESCC 22900 describes the basic requirements applicable to the total dose radiation testing of integrated circuits and discrete semiconductors suitable for space environments. It distinguishes between *in situ* testing, where electrical measurements are made on the devices under test ("DUTs") which are physically located in the irradiation chamber, and remote testing, where the DUTs are removed from the chamber for the measurements to be made. *In situ* testing is permitted either during or after irradiation. However, the majority of the document assumes that remote testing will be carried out with multiple, discrete radiation exposures and, hence, will yield data points at only a few values of total dose.

Mil-Std-883, method 1019 (and Mil-Std-750, method 1019 is very similar) uses the term 'in-flux' testing in place of '*in situ*'. The standard states that not-in-flux testing allows for more comprehensive electrical testing but may give misleading results if significant post-irradiation time dependent effects occur. *In situ* testing is permitted but, again, the remainder of the standard is written assuming that remote testing will be carried out.

In practice, the majority of tests are carried out using remote testing and just a few total dose steps. Both standards define time limits that should be observed so as to minimise post-irradiation, time dependent effects that may cause parameter values to shift significantly from their immediate, post-irradiation values. However, the guidance given in both standards regarding the number of dose steps and their spacing is sparse and different.

ESCC 22900 specifies that measurements shall be made at a minimum of three dose steps and that these shall be set at "1/3, 1 and 3 times the radiation level of interest".

Mil-Std-883 method 1019 provides no guidance at all on the number of dose steps and requires irradiation above the radiation level of interest only for certain technologies and in low dose rate conditions. One dose point would be sufficient to meet these requirements although, in practice, up to six dose steps are frequently applied.

Having considered these provisions of the two standards, it is worth noting that many tests deviate from one or more aspects of the standards. This may be because the end use or application has some features that justify a variation from the standard or because previous test data have influenced the test plan. The impact of this deviation for the measurement technique should be assessed.

III. A DESCRIPTION OF THE *IN SITU* METHOD

In situ (or in-flux) testing requires the measurement system to be included in the signal chain during exposure of the DUTs to irradiation. This may require the switching in and out of multiple test instruments and more than one bias condition to be applied to the DUTs.

A. Disadvantages of the in situ method

There are several disadvantages to the *in situ* method, including complexity of the electrical circuit, relatively long lead lengths, restrictions on how close instrumentation may be placed to the DUTs, radiation effects on the measuring system and potential issues with processing large amounts of measurement data.

The primary issue is ensuring that the fidelity of the measurement process is maintained throughout the test by avoiding any influence of radiation on the measuring instrumentation. This may be achieved by placing the instrumentation outside the radiation area. However, leads of more than 10m in length may be required, complicating the measurement of very low voltages and currents and making high speed measurements very difficult indeed. Alternatively, instrumentation may be located close to the DUTs and protected by shielding. The amounts of shielding required can be cumbersome and installing it may present a physical risk to the test equipment and personnel.

Some electrical tests simply cannot be carried out *in situ*. These include parameters for which a large or complex measurement system is required, especially for sophisticated

digital parts, such as microprocessors. Nevertheless, in these cases, *in situ* measurement of a parameter even as simple as the supply current can yield valuable information about the radiation response of the device.

A secondary issue relates to how the measurement system is set up. It is possible to generate large quantities of data, most of which, for slowly changing parameters, may be of little value. Some planning of the data collection strategy can significantly reduce the post-irradiation analysis effort.

One further issue to consider is the impact of frequent measurements using bias conditions different from those applied between measurements. If the radiation response of the DUT is strongly bias dependent then this approach can lead to a difference in the measured effects compared to a test carried out using remote testing. In this case, making less frequent *in situ* measurements so as to reduce the duty cycle at the different bias conditions, can help, while still yielding many times more data than remote testing.

B. *Advantages of the in situ method*

The main advantage of *in situ* testing is that the greater quantity of data gives much finer resolution of the effects of the radiation exposure, as measured on the total dose scale. Subtle and non-linear effects are more readily identified with *in situ* testing. An example of this phenomenon is shown in section III below.

In situ testing also helps to avoid errors due to time dependent effects occurring after irradiation and before measurement. The measurement system can continue running after the radiation source has been withdrawn, providing data from the point in time immediately after irradiation has ceased. This gives a detailed picture of the magnitude and rate of annealing effects.

In any real application, the circuit in which the DUT would be deployed would experience the impact of radiation exposure during and immediately after the exposure. *In situ* testing more closely mimics this situation than remote testing.

In order to benefit fully from these advantages of *in situ* testing, and especially for long duration tests, it is important to remember the value of measurements on a control device for validating the stability of the test set-up. Periodic measurement of an unirradiated device helps ensure that the measurement system has not drifted. If any drift is observed then this can be compensated for, either during the test or during the post-irradiation analysis.

IV. CASE STUDY

An example is given here for the total dose testing of a voltage reference device. The test was instrumented *in situ* to measure the output voltage of three DUTs of the same type of device. The DUTs were irradiated with static bias and at a dose rate of 447 rad[Si]/hr in Cobham's cobalt-60 gamma irradiation facility, located at Harwell, UK. The irradiation lasted for a duration of approximately four weeks.

Figure 1 shows the test board, with two sets of three samples in a horizontal row across the centre of the board. Data are presented here for only one of the two types of sample. A number of relays can also be seen on the board; these were used to switch the measurement system between the individual test samples. Measurements were made on each test sample at an interval of one minute. The board was housed in a lead/aluminium container to screen out low energy particles, as recommended in both standards.

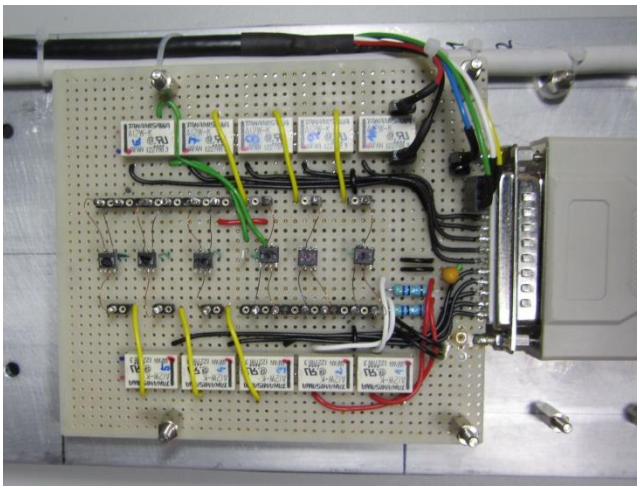


Figure 1: the test board housing the samples.

Figure 2 shows a graph of the change in output voltage when the measurements taken at each point in a series of dose steps of 50, 200, 250 and 300krad are plotted. It can be seen that the primary trend is for the measured value to decrease with increasing total dose. Based upon these data, a circuit designer may allow for a reduction of a certain percentage in the output voltage when designing a circuit using this type of device. For example, if a dose of 100krad were to be considered then a change of no more than 1%, compared with the initial value, might be expected from these data.

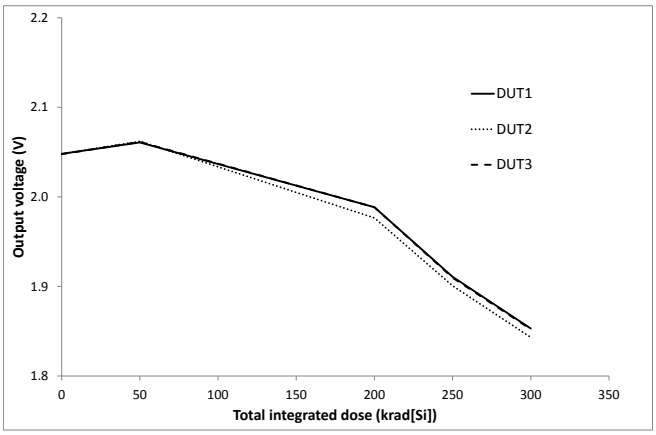


Figure 2: Output voltage against total dose with measurements at four dose steps.

Figure 3 shows the same data measured *in situ* at one minute intervals. Several features are visible. Firstly, the traces are much smoother, simply due to the finer dose resolution. Secondly, a significant rise in the output voltage is visible between 50 and 100krad, followed by an even larger reduction between 125 and 200krad. This feature is not visible in the first set of data because of the dose steps that happened to be chosen. With this additional information, the circuit designer would make a completely different allowance for shifts in the output voltage or might reject the device altogether.

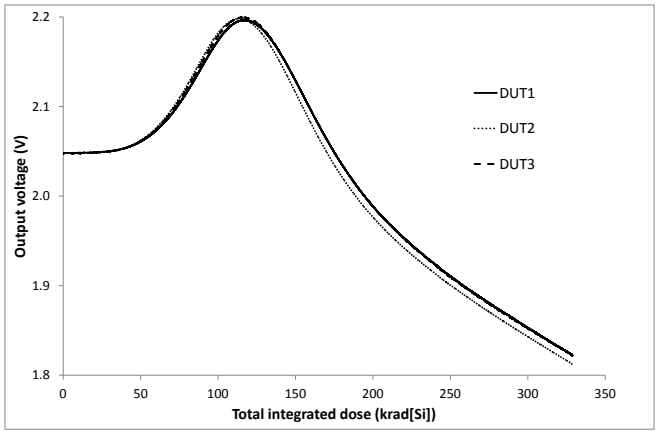


Figure 3: Output voltage against total dose with the full, *in situ* measurement data.

V. DISCUSSION

The experimental data show that, in the case of a nonlinear response to radiation exhibited by a given parameter, a data acquisition system based upon *in situ* measurements can reveal unexpected behaviour and yield valuable insights to the induced changes. The sometimes complex nature of this response may be missed by remote testing based upon a test regime using a small number of dose steps. Where remote testing is used, care is required in selecting the dose steps and the interval between them to reduce the probability of such a response being overlooked. An *in situ* test on one or two DUTs may be a useful screening technique to employ before a full test, using the simpler, remote testing technique, is carried out.

VI. CONCLUSIONS

The *in situ* method is not applicable to all types of device or all parameters, especially where high speeds or frequencies or very low voltages or currents are involved. However, DC and low frequency signals lend themselves readily to *in situ* monitoring and the additional data obtained, coupled with the greater total dose resolution, can lead to a much better understanding of the effects of irradiation on the samples.

VII. REFERENCES

[1] ESA ESCC Basic Specification No. 22900, "Total dose steady-state irradiation test method", issue 4, October 2010

[2] Mil-Std-883, method 1019, "Ionizing radiation (total dose) test procedure", issue 1019.9, June 2013

In-Situ Total Ionizing Dose Tests of SSPA Components

R. Uzel[a,b], M. B. Demirköz[a], A. Özyıldırım[b], O. Kalkan[b], H.I. Atasoy[b]

[a] Middle East Technical University, Physics Department, 06800 Ankara, Turkey
[b] Aselsan INC., 06172 Ankara, Turley

ruzel@aselsan.com.tr
demirkoz@metu.edu.tr
ayanartas@aselsan.com.tr
okalkan@aselsan.com.tr
hiatasoy@aselsan.com.tr

Abstract

In-house developed GaAs-based Solid State Power Amplifiers (SSPAs) operating at super high frequencies (SHF) have been tested using a ^{60}Co source to predict the module and its components' response when subjected to its actual space environment. GaAs-based electronic components are considered to be immune against TID. Test results are presented here that quantify residual performance degradations in component specs under various TID and other extreme environmental conditions.

I. Introduction

Electronic components in a working satellite will be exposed to a total ionizing dose (TID) commensurate with its orbit. Solar particles, electrons/protons trapped in the Van Allen belts and galactic cosmic rays (GCRs) are the main sources. TID due to electrons and protons can cause device failures whereas Displacement Damage (DD) and Single Event Effects (SEEs), although problematic, can cause temporary loss of function with lesser possibility of catastrophic failure. Such detrimental events have cumulative effects during the whole mission lifetime of the components and, with well-established techniques it is possible to estimate the time of failure under relevant operating conditions.

SSPA components are chosen as test subjects here as they are key configuration items in any communication satellite. Power Amplifiers (PA) boosts downlink signals in order to compensate for atmospheric path losses. The two primary types of PAs in the market today are: Solid-State Power Amplifiers (SSPAs) and Travelling Wave Tube Amplifiers (TWTAs) [1]. These amplifiers are also critical for space-borne phased-array applications. GaAs-based SSPAs are widely used in aforementioned systems today with GaN-based solutions fast catching up as attractive alternatives due to their inherently even higher power density capabilities [2].

The efforts of manufacturing domestic satellite payload components must be matched by capabilities to carry out standard radiation tests to qualify the resulting equipment for space. Reliability of these components within the space environment can only be guaranteed through ground-based qualification in terms of radiation tests and other widely used environmental tests under varying thermal, vacuum, vibration and shock conditions. Although, the latter set of tests can currently be performed in-house, there is an urgent need to develop the capabilities to carry out the radiation tests locally so as to expedite the qualification of satellite subsystems or components.

II. Total Ionizing Dose Test Plan

A. Test Techniques and Setup

At a short driving distance from ASELSAN, there is a radiation testing facility in Ankara; Sarayköy Nuclear Research and Training Center (SANAEM), operated by the Turkish Atomic Energy Agency (TAEK). As dictated by a tight schedule, the construction of the test setup at SANAEM, and the design and manufacturing of the modules were carried out simultaneously to reduce scheduling risks. TID tests are being performed using the ^{60}Co source located at the TAEK SANAEM Gamma Irradiation facility. The source has an activity level of 300 kCi and can deliver a dose rate higher than 30 kRad(Si)/h, which is in compliance with the ESA 22900 standard high dose rate recommendation. A new chamber was designed and built in order to attenuate and deliver the necessary dose rates [3].

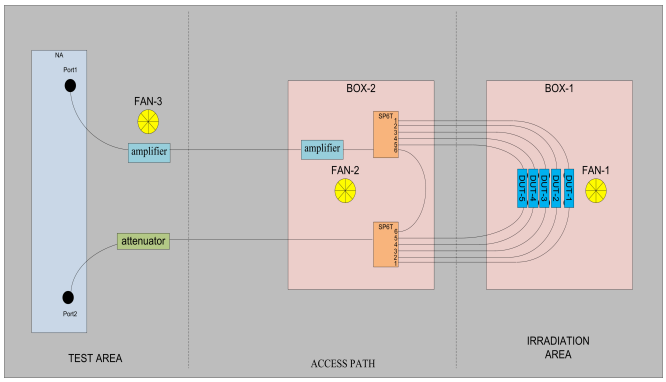


Figure 1: Bird's-eye view of the test facility at SANAEM. The irradiation area and the access path are under strict control for the safety of the personnel.

After careful consideration of the irradiation chamber dimensions, a decision was made to place the measurement

devices about 13 meters away from the DUTs. Inevitably, this leads to losses on the RF cables. Thus, amplifiers are used just before the network analyzer and also the RF selection switch. The amplifier before the RF switch is isolated against radiation using thick shielding boxes. Temperature variations during irradiation are also monitored.

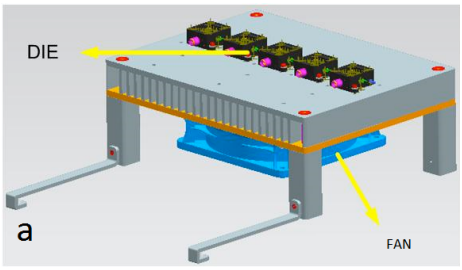


Figure 2. TID test setup for dice

DUTs are placed on an Aluminum slab that is raised off the floor and is cooled by a vertical blowing fan as seen in Error! Reference source not found. **Vertical Al bars acting as legs for the slab are secured on the floor. A picture of the actual setup is given in**
Figure 3.

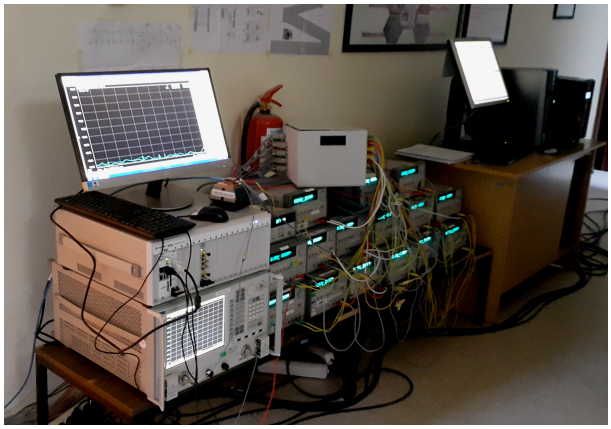


Figure 3. Test Equipment placed outside of the irradiation area.

B. Experimental Conditions

The Aluminum-Lead box attenuates the absorbed dose to the desired levels. The absorbed dose on the DUTs is calibrated using Alanine dosimeters to guarantee dose uniformity. Each one of Alanine dosimeters was placed on the edges of the test board to measure dose uniformity to accuracies better than 1%. The readout mechanism of the dosimeters was based on the procedure of electron spin resonance (ESR) that is capable of measuring dose levels up to 200 kGy.

We also controlled the ambient temperature of the irradiation area to be around 20 ^{0}C during exposure.

Depending on mission specifications, DUTs are expected to absorb around 100 kRad(Si) of total dose during their orbital lifetimes. Here, we use ESA 22900 recommended high level windows to administer a uniform 30 kRad(Si)/h radiation dose rate to reach a total dose of 300 kRad(Si) [4]. This is consistent with a safety factor 3 for the simulated radiation environment that the DUTs are exposed to.

III. Results and Discussion

As an oxide layer is not present, GaAs MMIC circuits are relatively immune to total ionizing dose effects in contrast to Si-based circuits. In addition, GaAs is a direct bandgap material while Si is an in-direct bandgap material. Thus, minority carrier lifetimes in GaAs are much less than those in Si that means increased immunity against radiation. Finally, due to very high surface state densities of GaAs, Fermi levels are pinned to what is dictated by the surface and hence prevent radiation-induced surface inversion and associated leakage currents [5]. Other studies of the effects of gamma irradiation on GaAS MMIC devices have also shown total dose hardness level near MRad(Si) [6][7][8][9].

Total Ionizing Dose effects were measured through a cascade of a high power amplifier, an attenuator, a power amplifier and a phase shifter within an in-house developed SSPA.

The gamma-ray measurements were performed using ^{60}Co sources providing 30 kRad(Si)/h to achieve 300 kRad(Si) total deposited dose. The DUTs were irradiated under operational bias conditions. Thanks to the fully automated in-situ test setup, all of the components were controlled/monitored and sampled for data, remotely.

Reference output powers for both High Power Amplifiers and Power Amplifiers, reference attenuation levels for attenuators and reference insertion loss levels for phase shifter are derived from components datasheets and pre-irradiation measurements with in-situ test setup.

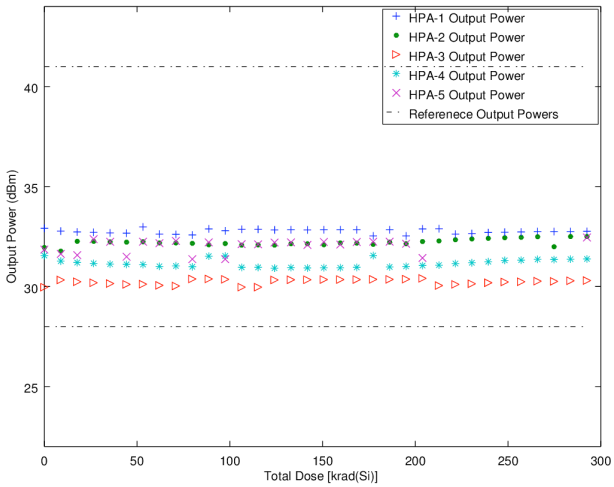


Figure 4. Effects of irradiation on output power characteristics of GaAs High Power Amplifier MMICs.

Figure 4 shows results of the total ionizing dose effects in each GaAs High Power Amplifier MMIC sample irradiated with ^{60}Co under operational bias conditions. The output power remains same levels with increasing radiation dose up to 300 kRad(Si). Similarly, Figure 5 shows output power characteristics of each GaAs Power Amplifier MMIC. Output power remains same levels as in High Power Amplifiers.

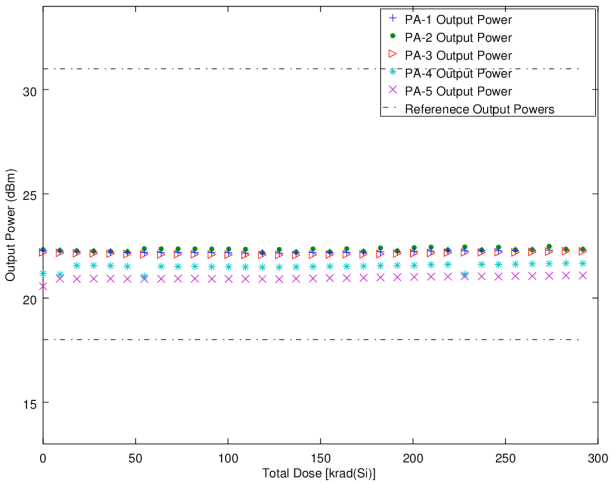


Figure 5. Effects of irradiation on Output Power characteristics of Power Amplifier.

Figure 6 shows the total ionizing dose effects in a GaAs Analog Attenuator MMIC irradiated with ^{60}Co under operational RF bias conditions. Here we focused on first attenuation result. First attenuation exhibits fluctuations around its initial attenuation values with increasing radiation dose.

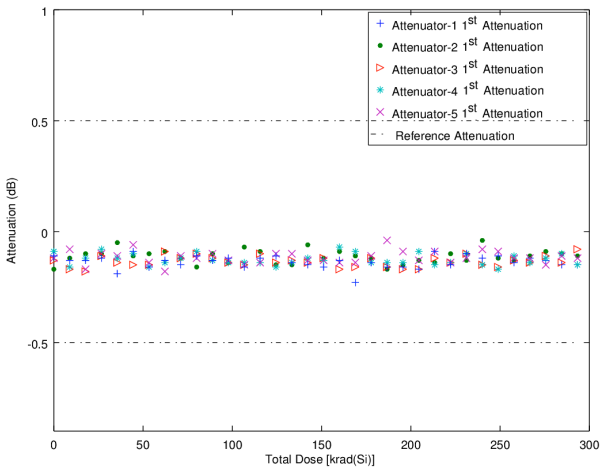


Figure 6. Effects of irradiation on Attenuation characteristic of Analog Attenuator.

Figure 7 shows the total ionizing dose effects in a GaAs Phase Shifter MMIC irradiated with ^{60}Co under operational bias conditions. As seen in Figure 7, insertion loss levels of each phase shifter exhibits monotonic decrease up to 300 kRad(Si) radiation doses.

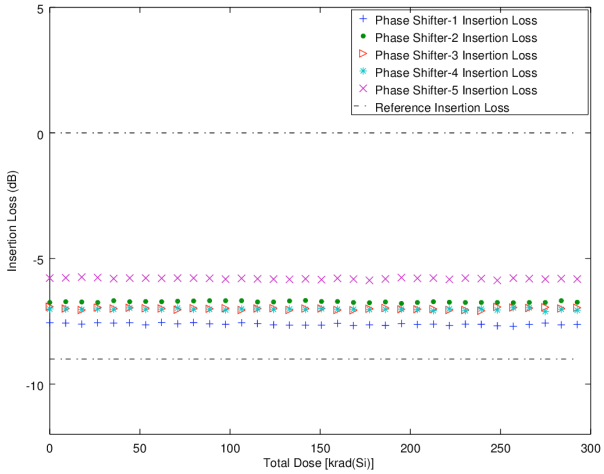


Figure 6 Effects of irradiation on Insertion Loss characteristic of Phase Shifter

IV. CONCLUSION

Radiation hardness of GaAs based components of SSPA under operational bias conditions were investigated. The test results exhibit excellent hardness characteristics under irradiation. The only significant change in the output power of the High Power Amplifier is around 1% below from expected values while it is similar for Power Amplifier. No degradation observed in attenuation characteristics of attenuator. Insertion loss of the Phase Shifter also observed within the expected values with 1% below its characteristics.

These results suggest that components of SSPA will operate successfully against gamma ray irradiation in the space environment.

Although, GaAs MMICs that are components of in-house developed SSPA modules are immune to total ionizing dose effects according to test results, radiation effect studies and tests of SSPA module itself will be investigated to insure its performance in the space environment.

V. ACKNOWLEDGEMENTS

The authors are grateful to Ö. Gündüz, and Z. Ünal from TAEK SANAEM Gamma Irradiation facility for their contributions during tests and M. Eray from Aselsan for his fruitful discussions and suggestions on test results.

This work was supported in part by the Republic of Turkey Ministry of Science, Industry and Technology under Grant 0616-STZ-2014.

VI. REFERENCES

[1] R. Strauss (1993, September). Orbital Performance of Communication Satellite Microwave Power Amplifiers (MPAs). International Journal of Satellite Communications. volume 11, 279-285.

[2] M. Kalinski. (2009, April). Evaluation of the Net Steps in Satellite High Power Amplifier Technology: Flexible TWTAs

and GaN SSPAs. Presented at IEEE International Vacuum Electronics Conference.
[3] R. Uzel et. al., (2015, November). Cost Effective Total Ionizing Dose Tests of Solid State Power Amplifiers. Presented at Reinventing Space Conference, UK, BIS-2015-24.
[4] ESA/SCC. (2010, October) Total-Dose Steady State Irradiation Test Method. Basic Specification No.22900.1-17.
[5] S. Kayali, G. Ponchak, R. Shaw. (December, 1996). GaAs MMIC Reliability Assurance Guideline for Space Applications, JPL Publication, 96-25.
[6] A. Meulenberg et. al., (December, 1988). Total Dose and transient radiation effects on GaAs MMICs, IEEE Transactions on Electron Devices, volume 35 (Issue 12), 2125-2132
[7] W. T. Anderson, M. Simons, A. Christou, J. Beall, (December 1985), GaAs MMIC Technology Radiation Effects, IEEE Transactions on Nuclear Science, volume 32 (issue 6), 4040-4045.
[8] K. Matsuzaki et al., (September 1997), Radiation Hardness pf Pseudomorphic HEMPT and Dual-Gate GaAs MES-FET MMICs, RADECS 1997 Conference, 114-119.
[9] Zuleeg, (March, 1989) , Radiation Effects In GaAs FET Devices, Proceedings of the IEEE, volume 77 (issue 3), 389-407

AMICSA: Evaluation and qualification of full custom ICs for space applications

Approval Process of an ESCC Qualified ASIC Supply Chain based on a Mixed-Signal IP Library

J. Steinkamp[a], F. Henkel[a] , V. Lück[b] , H.-D. Herrmann[c]

[a] IMST GmbH, Carl-Friedrich-Gauss-Str.2-4, 47475 Kamp-Lintfort, Germany
[b] TESAT SPACECOM GmbH & Co. KG, Gerberstraße 49, 71522 Backnang, Germany
[c] DLR (German Aerospace Center), Linder Höhe, 51147 Köln, Germany
jan.steinkamp@imst.de

Abstract

A fast and reliable development of a RadHard Space product benefits from a dynamic and efficient way of an ASIC design and supply chain. Design and qualification of a new ASIC is associated with a long development phase. Using an ESCC qualified supply chain with an IP library can reduce the development time to a space qualified product significantly and lowers the costs and risks of the product. This supply chain resolves the trade-off between a full custom design with all associated qualification steps and a semi optimized product based on standard ICs.
IMST and TESAT Spacecom are currently working in a DLR funded R&D project to built up such an ASIC supply chain that will be offered by IMST after approval by ESCC consortium. Completion of this project is planned for Q1 2017.
A first publication of this ASIC supply chain establishment has been given on the AMICSA 2014 in CERN [1].
In this paper an update will be given on the current status of this project with measurement results including TID and SEE evaluation. The designed library elements will be presented and an overview of the supply chain will be given with all supported technology features, package choices and the design flow information.

I. Preface

Prior to this funded project a technology evaluation phase has been initiated by TESAT Spacecom to validate the suitability of the XFAB's XH018 process for the intended RadHard ASIC supply chain. TID tests and SEE tests have been performed on digital cells and single transistors to prove it. In the current project two ICs have been designed: "spac2_eval" as the initial chip to test the principle suitability of the semiconductor process and the designed IP blocks and a second IC with additional IPs and redesigned IPs as the test device for the evaluation test program, called spac3_eval. The evaluation test program is currently running according to the ESCC specification 2269000 and first results are available. After this evaluation test a third IC will be designed as a MS-ASIC for the qualification according to the capability domain and manufactured as described in the process identification document (PID) IMST proposed for the ASIC supply chain. This supply chain begins with a certain specification of the ASIC, which will be commonly agreed between customer and IMST and finishes with the delivery of a space qualified ASIC with its accompanying documents. The involved steps of the supply chain are further described in chapter V.

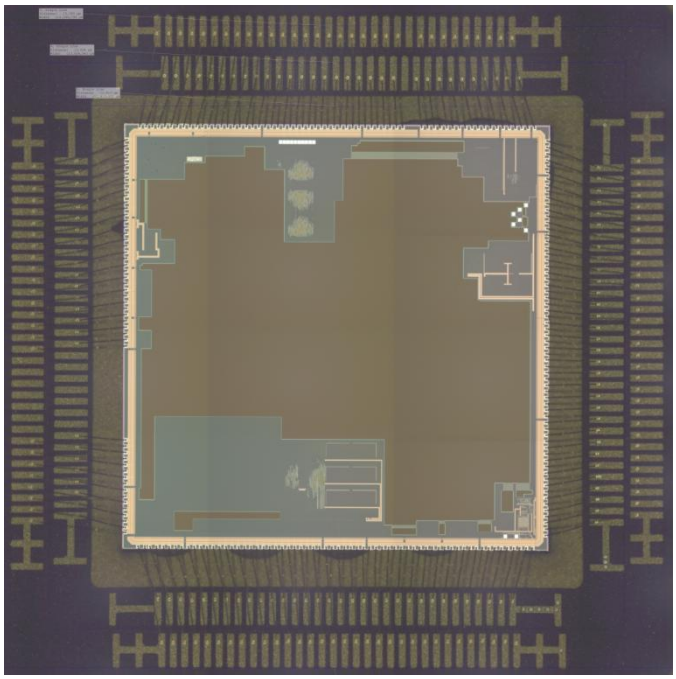


Figure 1: Photo of the bonded test chip "spac3_eval"

II. HARD Library Elements

The radiation hardened library designed by IMST, called HARD Library (HARD= Hard Against Radiation Design) supports I/O cells for 3.3 V and 5 V supply as well as level shifter I/Os for a negative supply voltage of -5 V on the ASIC. The other IPs are specified with the intention to cover a wide range of applications. The IP library contains data converters, biasing cells, memory modules, a reconfigurable opamp, LVDS driver and receiver, a SPI interface, OTP cells, a clk PLL, oscillators and special I/Os with cold spare functionality.
Different radiation hardening techniques have been implemented in the IP circuits to mitigate SEE and TID effects.

The following list gives an overview of the library elements with their key features:

IP Block	Main Characteristics
4-Wire SPI Interface	1.8V, extendible register bank with 8 register and 16 bit, each. Refresh logic for SEE mitigation implemented
I/O Cells	3.3V & 5.0V digital + Analog I/O, TMR In/Out
LVDS Driver	1.8V, Fmax=622 MHz
LVDS Receiver	1.8V and 3.3V, Fmax=622 MHz
Reconfigurable Multifunctional Operational Amplifier	•Inverting OpAmp with variable gain: -10 dB … +30 dB; 1dB step size •Non inverting OpAmp with variable gain: -10 dB … +30 dB; 1dB step size •LPF; 3 different cut off frequencies •I/U Converter with different input ranges •Schmitt Trigger with adjustable hysteresis •Voltage buffer •Open Loop configuration
Bandgaps	1.8V & 3.3V trimable
Reference Bias Generators	1.8V & 3.3V with PtoPR and constant currents & adjustable voltage references
Temperature sensor	1.8V, temperature range from -40°C…+150°C
POR Generator	POR delay: 5µs
LDO	Input voltage: 3.3V Output Voltage: 1.8V with adjustable short protection, 150mA I max
Level shifter High-Low	input signals with 0V…1.8V output signals with -5V…-3.2V
Level shifter Low-High	input signals with -5V…-3.2V output signals with 0V…1.8V
Digital Level shifter High-Low	3.3V-1.8V
Digital Level shifter Low- High	1.8V - 3.3V
16bit MUX	Max. signal frequency: 800 MHz
12 bit ADC	charge-scaling SAR ADC fast mode: 200 KS/s
Memory cell	2k x32 bit RAM module Clock frequency: 50 MHz.
12 bit DAC	segmented current steering DAC
Memory cell	64 bit OTP
Serializer / Deserializer	Data Rates: 600 Mbps with a reference clock Power: <500 mW
Clock PLL	16 bit 2nd order SDM fractional-N divider period jitter: 50ps (PK-PK)
DCXO	Supports 5 MHz … 50 MHz crystals
VCO with frequency divider bank	VCO frequency from 80 MHz – 600 MHz Divider bank ration from 1 to 128
CQFP package family	•Pin count: 256, 208, 132, 64 and 32 •100 Ω differential ports for LVDS interfaces •Die size from 2.2 mm^2 up to 100 mm^2

Table 1: Summary of the HARD library elements

III. Evaluation Tests

A. Test Chip & Electrical Measurements

A test chip spac3_eval containing all IPs as single blocks with their own individual supply pads has been designed and packaged in a 256 pin CQFP package. It is the largest defined package within the capability domain. The largest specified die size of 10 x 10 mm^2 has been chosen in order to have the worst case combination in terms of mechanical reliability like shock and vibration tests as specified in the evaluation test program. The picture of the bonded die is presented in Figure 1.

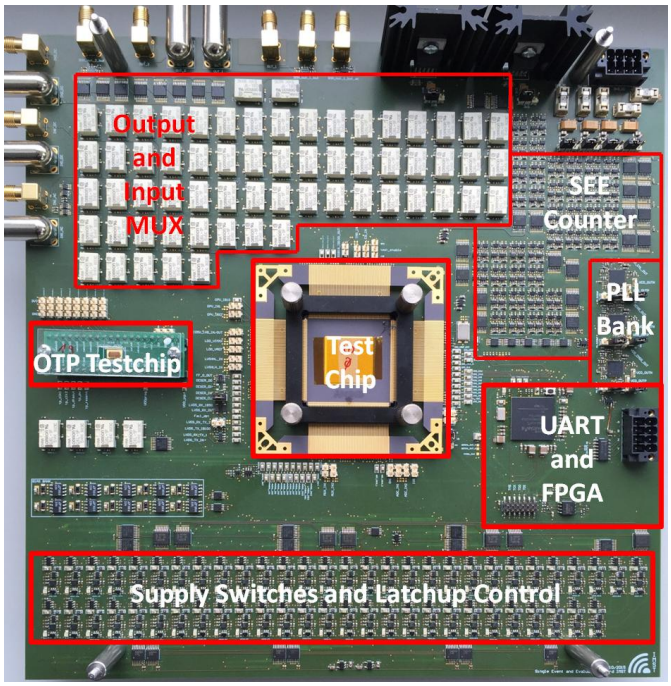


Figure 2: Evaluation board and SEE test board for the "spac3_eval" chip

Figure 2 shows the PCB used for electrical verification and SEE tests. It consists of different sections: the test chip mounted with a socket in the middle of the board and a further test chip containing the OTP test structure left of it. All signal input and output ports of the test chip are routed via relays to the SMA and BNC test connectors. The individual supply pins of the IPs are monitored against over current and latchup effects in the lower part of the PCB. For the single event transient tests a bank of comparators and counters with shift registers are used. SEE tested clock signals like DCXO, VCO or PLL are routed to external PLLs as reference clocks. The tuning voltage of the VCO from the external PLL and the lock detect signal is monitored during irradiation with heavy ions to detect any phase or frequency shift affected by the hits. A FPGA is the interface between the PCB and the PC. The evaluation board can be controlled by a programmed GUI.

B. SEE test

The SEE test for the shown test chip in Figure 2 will be performed in July 2016. Nevertheless the previous chip spac2_eval has been tested for SET, SEL and SEU at the CYCLONE110 facility in the Cyclon Resource Centre Louvain-la-Neuve. The test was performed based on the ESCC 25100 Specification (AD1), Single Event Effects Test Method and Guidelines.

The test PCB and test strategy is comparable to the current board shown in Figure 2. All IP blocks are enabled during the Single Event Effect test and were tested in the same way. All analogue circuit outputs are monitored by comparators to count all events over and under a specified and controlled threshold voltage. The counters have two comparators, one for -Vref and one for +Vref. Each time the signal passes over ±Vref a SET event is counted. Additionally all outputs are routed sequentially one after another to the oscilloscope for a specified time. If during this time a Single Event takes place,

Test	Ion M/Q=5	Energ. (MeV)	∢	Range (µm)	LET(MeV/ mg/cm^2)	Temp [°C]
1	^{20}Ne $^{4+}$	78	0	45	6.4	20
2	^{40}Ar $^{8+}$	151	0	40	15.9	20
3	^{84}Kr $^{17+}$	305	0	39	40.4	20
4	^{124}Xe $^{25+}$	420	0	37	67.7	20
5	^{125}Xe $^{25+}$	420	40	28.34	88.4	20
6	^{125}Xe $^{25+}$	420	40	28.34	88.4	125

Table 1: SEE Test conditions

the oscilloscope is triggered in single shot mode and a screenshot is stored in order to verify the SET amplitude and frequency of the ringing. At the end of the test every analogue output pin has been monitored by the oscilloscope for a certain time.

The Latch-up protection circuitry was designed for each power supply and test device. The Latch-up current limits were tuned individually for each circuit block to trigger for a supply current larger than 1.5 times the typical current.

Digital circuits like the RAM module and SPI controller are tested for SEU and SEL, only.

Table 1 shows the test conditions for the SEE test.

Representative results are shown for the 1.8 V bandgap circuit exemplarily in Figure 3 and Figure 4. Figure 3 shows the cross section of the counted hits while Figure 4 shows a screen shot of the transient plot for a hit with an Argon ion. Noticeable is the falling cross section between 67.7 MeV and 88.41 MeV. The reason is a detected SEU problem in the digital input pad of the chip control block leading to unintended interruptions of the SET measurement. Consequently the counter values are not reliable for the higher energy ions. The SEU problem has been resolved in a redesign and its effectiveness need to be proven in the upcoming SEE test. In a redesign of the bandgap, a topology has been implemented for a faster recovery of SETs and RC filters on sensitive nodes are added to further reduce the SET sensitivity. These modifications will be verified in the upcoming SEE test.

No SELs were detected in the measurement campaign.

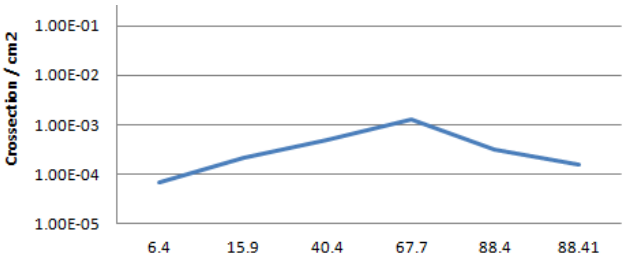


Figure 3: Cross section of the 1.8 V Bandgap vs. LETs at 25°C and 88.41 MeV*cm^2/mg at 125°C (last point)

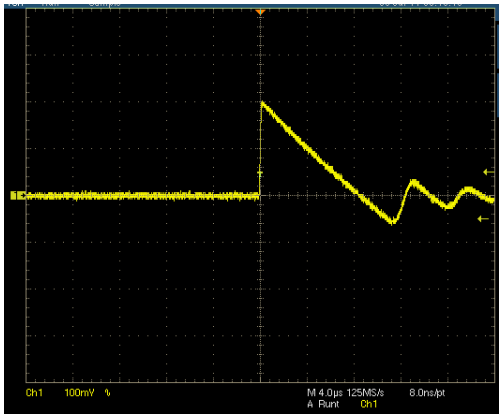


Figure 4: SET measured on the Bandgap output for a hit with an Argon ion

C. *TID test*

The TID test has been done according to the ESCC Basic Specification No. 22900 in the facility of ESTEC in Noordwijk. Figure 5 shows the irradiation board in front of the Co60 Gamma ray source. In Table 3 the radiation test plan is listed with the irradiation steps for the electrical measurements. Two initial measurements are done before irradiation has been started: 0_1 and 0_2.

LET (MeV/mg/cm^2)	hits
6.4	9
15.9	17
40.4	61
67.7	76
88.4	31
88.41	10

Table 2: Detected SET events

Total Dose [krad] (Si)	Dose Rate [krad/hrs] (Si)
0_1	0
0_2	0
9	0.275
33	0.275
104	0.275
200	3.3
300	3.3
24h annealing	0
192 h annealing	0

Table 3: Tested TID steps

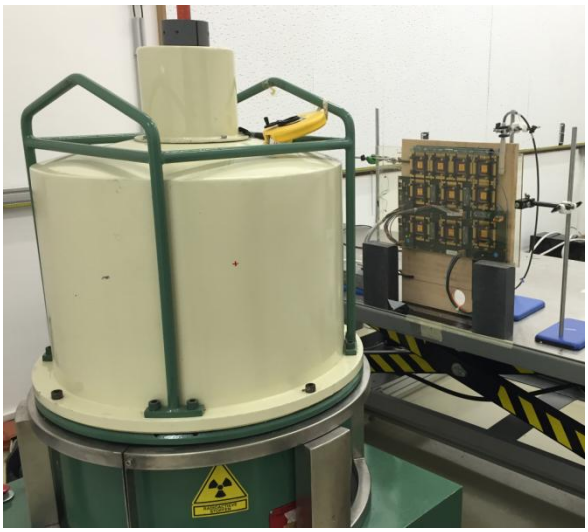


Figure 5: TID test board in the facility of ESTEC

First results with representative effects are shown here. A detailed documentation and evaluation of all results is ongoing at this time. The full documentation will be available after finishing the project.

The 1.8 V bandgap design show no significant effect on the irradiation neither on the output voltage, nor on the current consumption as shown in Figure 6. The variation of ± 0.25 mV is not correlated to the irradiation steps and can be explained with the measurement inaccuracy. According to the specified ± 2 mV variation over PVT, the TID variation is negligible. However, the 3.3 V bandgap shows a voltage drop versus total dose with a simultaneous current enhancement (Figure 7). Both parameters are falling back to the initial value after annealing. The variation vs. TID is with 8 mV larger as the specified ± 2 mV. A comparison of both designs show the advantage of the thinner gate oxide for the 1.8 V transistors compared to the 3.3 V transistors [2].

Another measured parameter is the resistance of a 3.3 V transmission gate. Shown is the resistance at a drain-source bias of 700 mV, where the NMOS and PMOS transistors are both contributing to the on-resistance. The resistance value drops versus total dose and goes back to the initial value after annealing (Figure 8).

In the previous test chip the ADC shows a drop of the output values for higher input voltages at higher TID levels (Figure 9, old version). The reason was supposed to be a leak of the small charge that is kept on the capacitors during the data conversion. In a redesign the leakage current effects have been improved and the new results showing the elimination of this effect.

The forecast of the final TID test summary is that the performance degradation due to ionising dose is very low for 1.8 V designs and has some effects on the 3.3 V designs. Circuits with low power consumptions can still suffer on the low remaining leakage of the 1.8 V transistors vs. TID as shown on the initial version of the ADC (Figure 9). But these effects can be handled by suitable mitigation techniques.

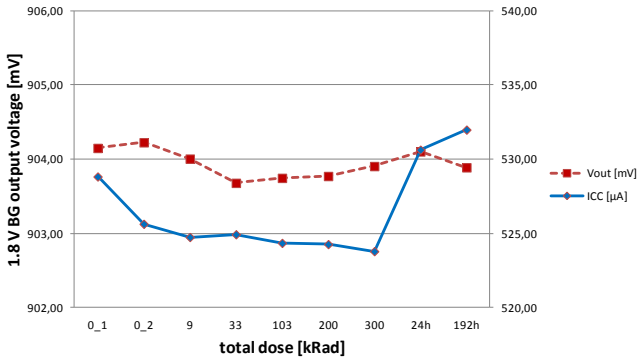


Figure 6: 1.8V Bandgap output voltage (dotted) and current (solid)

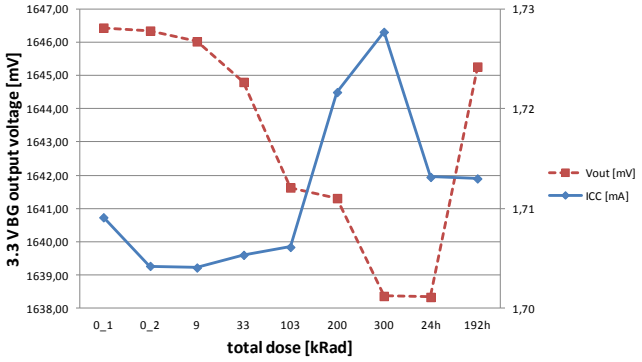


Figure 7: 3.3 V Bandgap output voltage (dotted) and current (solid)

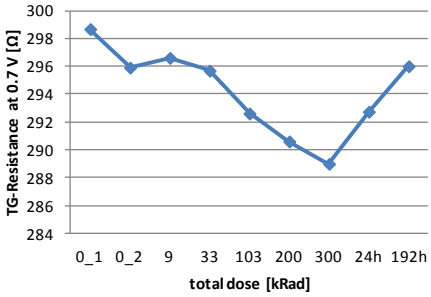


Figure 8: Transmission gate resistance

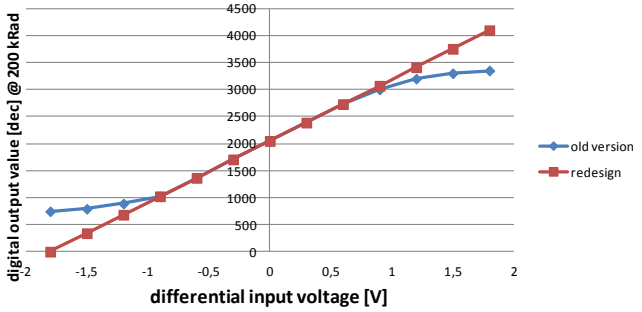


Figure 9: ADC old version vs. improved version

D. Mechanical tests

Aside from the electrical and radiation tests a set of mechanical tests are described in the ESCC 2269000 for the evaluation test program. Currently the assembly of the defined number of devices is ongoing together with the dimension, die shear and bond pull checks. Next steps are sealing the devices and continue with mechanical tests within this year. Since the test campaign is ongoing, no results can be reported up to now.

IV. ASIC SUPPLY CHAIN AND DESIGN FLOW

Two main design flows are targeted: One is a turn-key design by IMST based on customer requirements, while the other flow assists a co-design with the customer where the customer is allowed to provide encrypted VHDL codes. In the latter case IMST is creating the netlist with selected digital standard cells and implements TMR structures and scan chains in order to guarantee a RadHard design with test functionality. Analog features are handled by IMST using the IP library. On either case IMST delivers a tested, qualified and assembled RadHard ASIC.

A ceramic quad lead frame package family has been developed for the supply chain with different pin counts from 32 up to 256, supporting die sizes from 1.5 X 1.5 mm^2 for the smallest package up to 10 X 10 mm^2 for the largest package.

Figure 10 shows the involved steps for the ASIC supply chain, starting with ASIC specification, followed by the design and layout. After the layout, the production steps and test steps are shown.

For the quality assurance, the design and test phase will be followed by the "Space product assurance - ASIC and FPGA development" described in the ECSS-Q-ST-60-02C.

V. CONCLUSION

In this paper the current status and results are given on the DLR funded project 50 PS 1401 that has the aim to get the approval on an ESCC qualified ASIC supply chain. For this supply chain an IP library has been designed and first test results are presented. With this supply chain IMST will become a provider for qualified RadHard ASICs.

VI. REFERENCES

[1] ESA Requirements and Standards Division. Space engineering, product assurance. Techniques for Radiation effects. Mitigation in ASICs and FPGAs. 2009 © ESA for the members of ECSS

[2] J. Steinkamp, F. Henkel, V. Lück. 180nm CMOS Mixed-Signal Radiation Hard Library as base for a full ASIC supply chain. AMICSA 2014

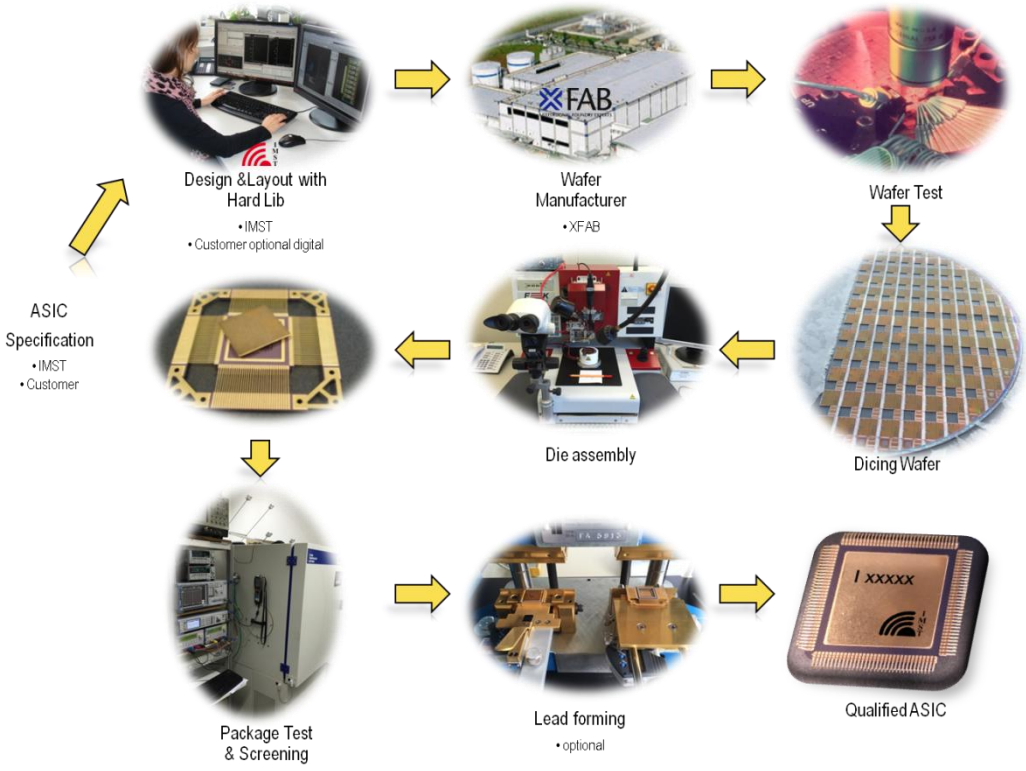


Figure 10: ASIC supply chain

AMICSA: In-orbit Experiences and flight heritage of analogue and mixed-signal ICs

An Update on Medipix in Space and Future Plans (Medipix2, 3 & 4)

L. Pinsky[a] , T. Campbell-Ricketts[a], A. Empl[a], S. George[a], L. Tlustos[a], D. Turecek[a], D. Fry[b], M. Kroupa[b], R. Rios[b], E. Semones[b], N. Stoffle[b], S. Wheeler[b], C. Zeitlin[b]
H. Kitamura[c], & S. Kodaira[c]

[a]University of Houston, 77204 Houston, TX, USA
[b]NASA, 77058 Houston, TX, USA
[c]HIMAC, QST-NIRS, 4-9-1 Anagawa, Inage-Ku, Chiba-Shi 263-8555, Japan

pinsky@uh.edu

Abstract

Medipix technology in the form of Timepix chips from the Medipix2 Collaboration have been in continuous operation in LEO (Low Earth Orbit) externally (in vacuum) on satellites and internally within the ISS for over three and half years. To date no failures of the Timepix chips themselves have occurred during any of the more than 30 combined exposure-years, although there have been a few minor failures in the supporting electronics. These exposures include numerous single devices powered and readout via ISS onboard laptops, self-contained battery-powered units on the first test of NASA's new Orion MPCV during the EFT-1 flight, as well is dedicated satellite based devices including the 5-chip LUCID (Langton Ultimate Cosmic-ray Intensity Detector) device on the UK's TechDemoSat mission. A summary of the functional information and the data gathered from these missions are presented along with the recent evaluation of n-in-p Si sensors on both Timepix and Timepix3 chips in comparison with the baseline results using the nominal p-in-n Si sensors.

Future plans include flying additional single units as radiation monitors inside the ISS and the upcoming test of the inflatable Bigelow Expandable Activity Module (BEAM) module as well as deploying a multiple Timepix stack to evaluate its potential to improve incident particle ID capability. In the longer term the primary charged particle radiation monitors to be flown on the next few flights of the Orion, called the HERA (Hybrid Electronic Radiation Assessor), is undergoing the final verification process. Evaluation of the Data-Driven Timepix3 from the Medipix3 Collaboration is underway as well, and it will be used in the verification process for the frame based Timepix and Timepix2-based devices from the Medipix2 Collaboration. The Timepix2 is in the final design process at CERN, and will be evaluated for replacement in the HERA hardware for eventual operational Orion missions. The Medipix4 Collaboration has just formed and is in the process of developing the design concept for the Timepix4 chip. The University of Houston, with support from NASA and the University, is one of the founding members of the Medipix4 Collaboration, which will hopefully ultimately provide the basis for future long term radiation monitoring and active personal dosimeter devices.

Table 1: Medipix Chips, Past, Present and Future. (P.C. =(Photon Counting, and * = Not yet available). Note only the final versions in the development of each chip line are listed.

Name	**# & Pixel size/ CMOS Tech.**	**Modes**	**Read-Out**
Medipix1			
Medipix1	64 x 64 170μm/ ~1μm IBM	P.C.	Frame
Medipix2			
Medipix2	256x256 55μm/ 250nm IBM	2 Threshold P.C.	Frame
Timepix	256x256 55μm/ 250nm IBM	TOT, TOA or P.C.	Frame
Timepix2*	256x256 55μm/ 13nm TSMC	TOT+TOA or P.C.	Frame
Medipix3			
Medipix3RX	256x256 55μm 128x128 110μm/ 130nm IBM	2 Threshold P.C. 4 Threshold P.C.	Frame 2 Regis
Timepix3	256x256 55μm/ 130nm IBM	TOT+TOA or Continuous PC	Frame or Data Driven
Medipix4			
Medipix4*	TBD/ (65nm TSMC)*	TBD	Frame or Data Driven
Timepix4*	TBD (65nm TSMC)*	TBD	Frame or Data Driven

I. The Medipix Collaborations

The sequence of CERN-based Medipix Collaborations had their start with the initial efforts of Michael Campbell, Eric Heijne, Walter Snoeys and others in the in the early 1990's using the experience from the RD19 Collaboration and earlier

efforts in the development of radiation sensing pixel detectors[1], [2], [3] [4]. The constant design characteristic of all of the Medipix Collaborations has been the employment of the hybrid design whereby the readout chip and the overlaying sensor volume were separate, typically connected using the Flip-Chip® "solder-bump bonding technology [5]. The Medipix2 Collaboration formed in the late 1990's, and set the tone for the subsequent incarnations in the sequence. Each Medipix Collaboration is an aggregation of member institutions that each pay an initially set collaboration fee to join, with that initial infusion of funding sustaining the collaborations activities until supplemented by royalties from the licensing of their products. The membership is only partially overlapping, as are the associated access rights to the products of each collaboration. Medipix3 formed in 2006 and Medipix4 has just formed in late 2015. The three latter Collaborations are all still active. Table 1 lists the chips produced by each collaboration and their essential design characteristics. All of the past and present space flight units have been based on the Timepix chip from the Medipix2 collaboration. Bare Timepix assemblies and various control and readout interfaces have been licensed to a number of vendors for sale to the public along with licenses to sell the Medipix2 chip by the Medipix2 collaboration. The Medipix3 collaboration have licensed distribution Medipix3RX chips and at some point in the not too distant future, they will likely license the distribution of the Timepix3.

II. The Medipix2 Timepix Chip

The Timepix chips contain 256 x 256 pixels, each 55 μm on a side, providing an effective area of the chip that is 1.982 cm2 [6]. The full chip is 16.120 x 14.111 mm, which includes a service area on one side of the chip that contains 127 input/output wire-bond pads for control, readout and power. Each pixel contains the circuitry within its footprint to digitize the output. As such, only digital data is transferred out of the pixels, unlike CCDs and monolithic CMOS detectors. The input to each pixel is through a conducting solder pad on the upper surface of the chip.

To fabricate a charged particle detector employing a Timepix, one must attach a semiconductor sensor to the top surface of the pixels as shown in Figure 1. Different sensor materials may be used for various applications, but for charged particle detection, silicon is the semiconductor of choice. Sensors with thicknesses from 50 μm to 1.0 mm have been fabricated; with 300 and 500 μm thick sensors used on the ISS REM units, and exclusively 500 μm thick sensors employed on all additional NASA projects to date. The sensors are fabricated so that the bulk volume is doped as either p-type or n-type, with opposite doping implants on the lower surface. The REM units employ bulk n-type sensors. The implants are in contact with conducting solder pads on the lower surface of the sensor, which allows the bulk sensor volume to be reverse-biased to deplete it of free charge carriers. As noted previously, the sensor is attached to the Timepix chip using the FlipChip® solder-bump technology. The bias voltage also serves to collect any free electron-hole pairs created by the passage of charged particles in the sensor volume. The presence of free charges in the sensor volume causes images charges to appear on the sensor's solder pad. The return path for the bias voltage runs through the solder-bump and the pixel's analog front-end circuitry. Thus the current induced in the solder bumps by the formation of the image charges is amplified and shaped by the analog front-end circuitry in each pixel. The current flow created in the front-end electronics is generally proportional to the energy deposited in the sensor volume, and the digital portion of each pixel digitizes that value for readout. The digital section of each pixel can be set to function as a charge-summing Wilkinson-type Analog-to-Digital-Convertor (ADC) using the Time-Over-Threshold (TOT) technique where the time is referenced to an external clock signal with a maximum frequency of 100 MHz.

In operation, the Timepix is controlled by providing discrete inputs to the internal Digital-to-Analog-Convertors (DACs) to set various working parameters such as the threshold to suppress noise. In addition, data-taking is activated by providing an external gate or "shutter" signal. This shutter can be set to a very wide range of time values from microseconds to minutes or more. As a practical matter for measuring the energy deposited by charged particles, the minimum shutter time should be an order of magnitude or two longer than the longest anticipated digitization time using the TOT method, which for space radiation situations is on the order of a millisecond. The Timepix and related devices produced by the Medipix2 Collaboration are also capable of being configured to measure the properties of the incident neutron flux[7],[8],[9], but this paper will focus solely on the detection and measurements of incident charged particles. Each detector in use has been individually calibrated pixel-by-pixel to yield an accurate correlation between the TOT counts recorded and the energy deposited in the sensor volume that was responsible for that pixel's response [10].

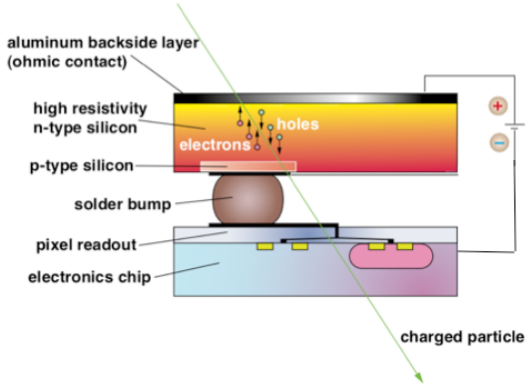


Figure 1: Timepix Hybrid Assembly. Each pixel in the underlying chip is connected to a bulk semiconductor sensor through a solder-bump as shown. The bulk sensor volume is separated from the sensor's ohmic contact with an opposite polarity doped implant to allow the formation of a p-n junction in the sensor for each pixel. (Courtesy of the Medipix2 Collaboration)

Generally speaking, the cluster of pixels produced by a penetrating charged particle has a clearly defined core of contiguous pixels that can be geometrically identified [11], [12], [13]. For slower particles (e.g. protons, He and heavier

ions with kinetic energies below a few hundred MeV/u) there are rarely any disconnected pixels. However, for higher velocity particles, the production of δ-rays can lead to geometrically discontiguous pixels. With low occupancy frames, the association of these separated pixels can be recovered, but in busier frames such correlations can become ambiguous.

II. The Medipix3 Timepix3 Chip

The Timepix3 chip[14] is still in the evaluation phase of its development, and has not yet been deployed in space. It differs from the Timepix in a number of important characteristics. Although it has the same pixel size and number as the Timepix, and can be operated in a "Frame" mode with summing TOT measurements in each pixel for the duration of the frame's live time, one of its primary distinguishing capabilities is to be operated in a "Data-Driven" mode. For readout purposes, the individual pixels are ganged into super-pixels of 4 by 4 pixels in adjacent columns. The readout path runs down to the output buss between every other column of pixels with a token passing along the super-pixel interface every 40ns. If data are present in a super-pixel, the token shifts out the contents of that super-pixel, which are added to the serial stream being continuously readout from the chip. With an appropriately fast interface, this mechanism will support the recovery of all data without significant loss for random hits on the pixel matrix up to ~81 MHz. Compact USB 3.0 based interfaces have been demonstrated to function at rates of up to half that value.

Another major difference between the Timepix and Timepix3 is the addition of a "Time-Of-Arrival" (TOA) recording by each pixel of the time of threshold crossing to an accuracy of ~1.6 ns. This is accomplished by giving each pixel access to a global 40 MHz clock and a local 4-bit high-speed divider in each pixel to enable recording of the TOA to the stated accuracy. This data is included with the TOT in the output stream.

This Data-Driven output capability comes at the cost of increased power consumption with respect to the Timepix when the interface electronics power consumption is included. Currently, the available Timepix3 USB interfaces power requirements slightly exceed the capability of typical laptop USB powering ability and require external power supplies. One can, of course operate the Timepix3 in the Frame mode to reduce the power consumption and still take advantage of first-hit TOA information. Plans by the Medipix2 Collaboration to produce a Timepix2 replacement for the current Timepix will be close to a "plug-&-play" replacement from the control standpoint, but it include the addition of the TOA capability in several operating modes. Full details of this addition to the Medipix2 family will be forthcoming from the Medipix2 Collaboration.

III. Present and Planned Timepix Deployments In Space

Table 2 lists the present and future planned deployment in space[15], [16], [17] [18]. It is important to note that while some of the COTS ("Commercial Off The Shelf") interfaces that were employed in the first uses in space did suffer some long term parts failures, post failure analysis has determined that none of these failures were due to the Timepix chip itself. In all cases where the Timepix chips have been recovered after up to 3 years in space (in LEO), no measurable degradation of performance has been observed. This level of robustness has encouraged NASA to proceed to plan future on-board active radiation monitoring based on the continuing Medipix technology. To date, Timepix devices have been deployed in vacuum in polar orbits (LUCID and SATRAM) as well as internally in manned spacecraft (ISS and Orion/MPCV) in various orbits, with the EFT-1 mission penetrating the more intense regions of the Earth's trapped radiation [15]. Further, multiple exposures of Timepix devices for hours in intense heavy ion accelerator beams over several years has continually built confidence in the ability of these chips to operate successfully in the harshest of radiation environments. One recent test of a Timepix3 detector was demonstrated in a sustained proton beam flux of $> 4 \times 10^5$ /cm^2 s without loss of data or any perceived damage.

IV. Acknowledgments

The support of the Medipix2 and Medipix3 collaborations is gratefully acknowledged, along with specific acknowledgment of the essential contributions over the years of the director and members of the Institute for Pure and Applied Physics at the Czech Technical University in Prague. Clearly, the support of the Space Radiation Analysis Group at the Johnson Space Center in Houston, Texas, has been essential as well. The University of Houston has provided significant support, as has NASA via pass-through contracts (T72203 & T73015) from Wyle Laboratories in Houston, Texas.

V. References

All bibliographical references should be numbered and listed at the end of the paper in a section called "REFERENCES". When referring to a reference in the text, place the corresponding reference number in square brackets [1], [2], [3], etc...

Example:

[1] M. Campbell et al., 1990, "A 10 MHz CMOS front-end for direct readout of pixel detectors," Nucl. Instr. and Meth. A 290, 149.

[2] M. Campbell et al., 1994, "Development of a pixel readout chip compatible with large area coverage," Nucl. Instr. and Meth. A 342, 52.

[3] E. H. M. Heijne et al., 1996, "LHC1: a semiconductor pixel detector readout chip with internal, tunable delay providing a binary pattern of selected events, " Nucl. Instr. and Meth. A 383 55.

[4] M. Campbell et al., 1998, "A Readout Chip for a 64 x 64 Pixel Matrix with15-bit Single Photon Counting." IEEE Trans. On Nucl. Sci., 45 (3), 751.

[5] Riley, G., 2000. Solder bump flip chip – tutorial #2. http://flipchips.com/tutorial/ bump-technology/solder-bump-flip-chip/. Viewed Nov. 23 2014.

[6] X. Llopart, et al., 2007, "Timepix, a 65k programmable pixel readout chip for arrival time, energy and/or photon counting measurements. Nucl. Instrum. Methods Phys. Res., Sect. A,

Accel. Spectrom. Detect. Assoc. Equip. 581, 485–494. Nucl. Instrum. Methods Phys. Res., Sect. A, Accel. Spectrom. Detect. Assoc. Equip. 585 (2008) 106 (erratum).
[7] J. Jakubek, et al., 2006 "Neutron imaging with Medipix2 chip and a coated sensor. Nucl. Instrum. Methods Phys. Res., Sect. A, Accel. Spectrom. Detect. Assoc. Equip. 560, 143–147.
[8] J. Jakubek, et al., 2009, "Position-sensitive spectroscopy of ultra-cold neutrons with Timepix pixel detector." Nucl. Instrum. Methods Phys. Res., Sect. A, Accel. Spectrom. Detect. Assoc. Equip. 607, 45–47.
[9] D. Greiffenberg, et al., 2009, "Detec- tion efficiency of ATLAS-MPX detectors with respect to neutrons," Nucl. Instrum. Methods Phys. Res., Sect. A, Accel. Spectrom. Detect. Assoc. Equip. 607, 38–40.
[10] M. Fiederle, et al., 2008, "Energy calibration measurements of MediPix2," Nucl. Instrum. Methods Phys. Res., Sect. A, Accel. Spectrom. Detect. Assoc. Equip. 591, 75–79.
[11] T. Holy, et al., 2008, "Pattern recognition of tracks induced by individual quanta of ionizing radiation in Medipix2 silicon detector," Nucl. Instrum. Methods Phys. Res., Sect. A, Accel. Spectrom. De- tect. Assoc. Equip. 591, 287–290.
[12] S. Hoang, S., 2014, " Data analysis of tracks of heavy ion particles in timepix detectors. J. Phys. Conf. Ser. 523, 12026–12034.
[13] L. Pinsky, et al., 2011, "Penetrating heavy ion charge and velocity discrimination with a TimePix-based Si detector (for space radiation applications," Nucl. Instrum. Methods Phys. Res., Sect. A, Accel. Spectrom. Detect. Assoc. Equip. 633 (Supp. 1), S190–S193.
[14] M. De Gaspari, et al., 2014, "Design of the analog front-end for the Timepix3 and Smallpix hybrid pixel detectors in 130 nm CMOS technology," J. Instrum. 9, C01037.
[15] N. Stoffle, et al., 2015, "Timepix-based radiation environment monitor measurements aboard the International Space Station. Nucl. Instrum. Methods Phys. Res., Sect. A, Accel. Spectrom. Detect. Assoc. Equip. 782, 143–148.
[16] A. Bahadori, et al., 2015, "Battery-operated independent radiation detector data report from Exploration Flight Test 1. NASA/TP-2015-218575, http://ston.jsc.nasa.gov/collections/TRS/_techrep/TP-2015-218575.pdf.
[17] L. Pinsky, et al., 2011, "Application of the Medipix2 technology to space radiation dosimetry and hadron therapy beam monitoring," Radiat. Meas. 46 (12), 1610–1614.
[18] M. Kroupa, et al., 2015, "A semiconductor radiation imaging pixel detector for space radiation dosimetry," Life Sciences in Space Research Volume 6, 69–78.

Table 2: Summary Past, Present and Planned Medipix deployments in Space

Mission/Project Launch Date	Agency (Country)	Number of Timepix Detectors	Exposure Time In Space to Date	Timepix Failures to Date	Orbital Parameters (altitude/Inclination)
ISS/REM Aug. 2012	NASA	7 total	Max time chip 3 yre 10 months	0	~400 km/ 51°
ProbaV-SATRAM May, 2013	ESA	1	3 yrs 1 month	0	820 km/96° Sun Sync.
TechDemoSat/LUCID July 2014	(UK)	5	1 yr 11 months	0	500 km/98° Sun Sync.
MPCV-EFT-1/BIRD Dec. 2014	NASA	2	~4 hours	0	400-5910 km/28.6°
RISESat/Timepix (2016)	JAXA (Japan)	1	TBD	TBD	~700 km/Sun Sync.
ISS/JSC X-Project (2017)	NASA	2	TBD	TBD	~400 km/ 51°
Biosentinel/HERA (EM-1)	NASA	1	TBD	TBD	Parasitic EM-1 Payload
MPCV-EM-1/HERA (2020)	NASA	3-5	TBD (2-3 Weeks)	TBD	Trans-Lunar
MPCV-EM-2/HERA (2022)	NASA	3-5 (Timepix2 or Timepix4?)	(2-3 Weeks)	TBD	Trams-Lunar

AMICSA: Needs and Requirements for analogue and mixed-signal ICs in future space missions

Serial I/O ADCs/DACs : The Next Giant Leap in Mixed-Signal for Space

R. Bedi

Spacechips Ltd, Harpenden, U.K.

rajan@spacechips.co.uk

Abstract

Today, the cost and effort to develop satellite payloads, platforms and space instruments have to be repeated for each new mission, introducing unnecessary re-design, re-test, performance, re-qualification, schedule and budget risks to key programs.

Operators are constantly complaining to OEMs that the cost to develop satellites is prohibitively expensive, delivery takes too long and never right-first-time, while satellite manufacturers are handicapped by the reusability limitations of current mixed-signal electronics.

Today, 3 billion people around the world do not have internet access and new, Silicon-Valley entrepreneurs intend to build thousands of low-cost, satellites to address this market. The traditional approach to developing space electronics is simply too bespoke, too expensive, too inflexible and too power consuming to deliver tomorrow's, space-enabled world for everyone.

Serial-I/O ADCs/DACs offer manufacturers of satellite sub-systems the potential to deliver spacecraft operators bespoke levels of performance without having to continually re-engineer the avionics. Individual customer needs can be accommodated by simply swapping pin-to-pin compatible ADCs/DACs each with different resolutions (SNRs), because for the first time, the digital interfaces will remain the same. This novel advance means that only mission-specific, on-board processing algorithms will have to be re-coded, completely eliminating non-recurring, hardware design effort and cost. Recurrent test and manufacturing costs will also be reduced, allowing future satellites to be delivered right-first-time, within budget and to schedule.

Introduction

The digital payloads used on the Sentinel-1 and NovaSAR, Earth-observation satellites performed very similar functions but each had its own architecture, hardware design, fabrication, assembly, test and qualification. Effort and cost had to be duplicated and in terms of performance, the only difference between both was one effective bit.

Similarly, the digital payloads used on Alphasat and that being developed for the Inmarsat 6 telecommunication satellite perform very similar channelizing functions, but each has its own architecture, hardware design, fabrication, assembly, test and qualification. Effort and cost was duplicated and in terms of performance, the only difference between both payloads was 2 dB and extra information bandwidth.

The traditional approach to developing mixed-signal, payload electronics is simply too bespoke, too expensive and too inflexible.

The JESD204 Standard

Parallel-I/O devices have reached their limits in terms of pin count, package size, parasitics and managing skew between digital signals and their clocks. High-speed serial links embed clocking information within the bitstream which is extracted by the receiving device.

Initially semiconductor vendors developed their own proprietary serial-I/O ADCs/DACs with little or no interoperability between these or companion logic devices. To standardise devices, JEDEC formed a working group and published the first industry-wide standard for serial-I/O ADCs/DACs in 2006. This defined a high-speed serial link for a single lane with a maximum data rate of 3.125 Gbps as illustrated below:

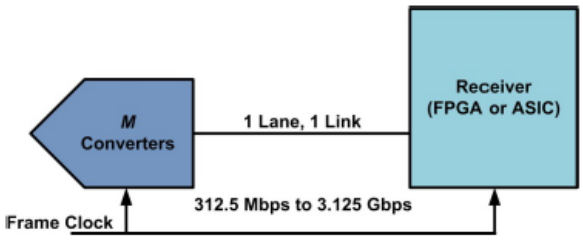


Figure 1: Serial ADC connected to a FPGA

In 2008, JEDEC formally released revision A of the standard which supported multiple-aligned serial lanes with data rates up to 3.125 Gbps as shown below:

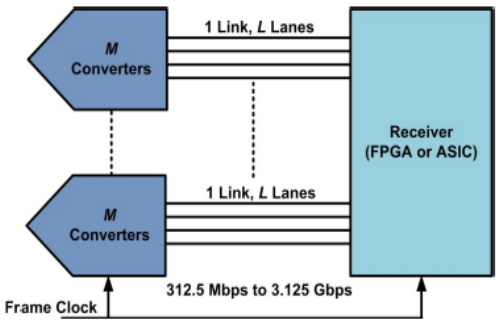


Figure 2: Serial ADCs connected to a FPGA

To accommodate the increasing performance needs of cellular base-stations, JEDEC released revision B of the standard in 2012 which added deterministic latency and supports data rates up to 12.5 Gbps as illustrated below:

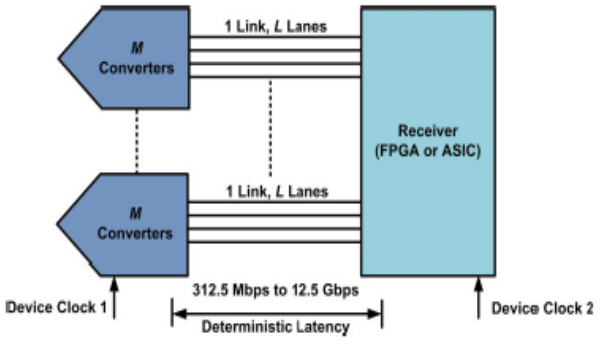


Figure 3: Serial ADCs connected to a FPGA

A serial-output ADC connected to an FPGA is shown below. The ADC is physically small, 10 x 10 mm, occupying significantly less footprint than an equivalent, parallel-output ADC. Only two pins are required for each high-speed serial link, easing PCB layout and routing effort, resulting in simpler and less expensive PCBs as shown below:

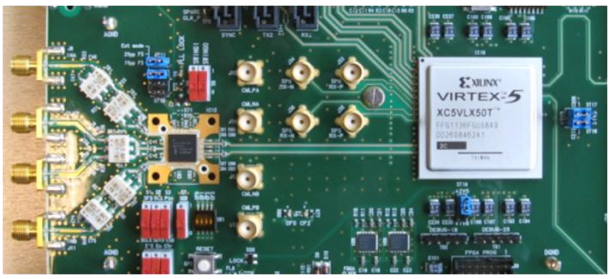


Figure 4: ADC connected to FPGA using high-speed serial links

Due to limits in the number of available I/O, up to four broadband, parallel-I/O ADCs/DACs can be reliably connected to one V5QV FPGA. Achieving timing closure of several hundred high-speed I/O can be very challenging. Conceptually, many more serial-I/O ADCs/DACs can be connected to one FPGA as illustrated below:

Figure 5: Serial ADCs/DACs connected to a space-grade FPGA

Hardware verification of digital interfaces will change from traditional IBIS simulation to IBIS-AMI modelling. This too has been standardised by silicon vendors and the EDA industry to allow interoperability between devices. The analogue and mixed-signal extension to the IBIS specification was developed to simulate a BERT, allow interoperability between models from different semiconductor vendors using commercially available EDA tools, with the ability to simulate ten million bits in minutes.

Compared to traditional IBIS, protected, proprietary, behavioural DSP algorithms have been added in the form of compiled executables to support SERDES emphasis and equalisation functions.

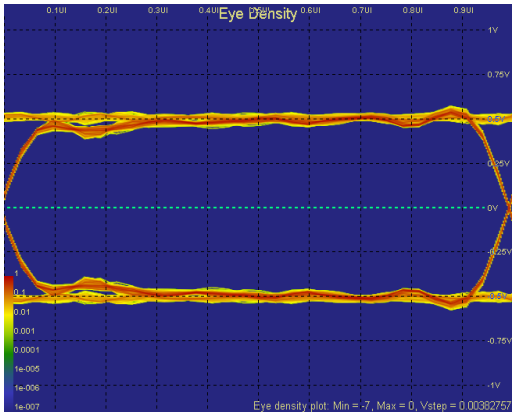


Figure 6 : Serial ADC connected to an FPGA

Serial-I/O ADCs/DACs also offer the potential of locating mixed-signal convertors at the RF receive/transmit antenna, exploiting high-speed serial links connections to the digital payload processor.

Conclusion

JESD204 is a mature and proven standard adopted by the global electronics industry and supported by the major mixed-signal providers.

JESD204B offers deterministic latency capability to support digital beamforming applications and can offer the space industry the same benefits it delivered cellular telecommunications.

AMICSA: Other topics

Radiation Prediction Tool Dedicated to Analyzing and Hardening by Design Readout Circuits of Photonic ICs

L. Artola[a], S. Ducret[b], G. Hubert[a], F. Perrier[b], N. Ricard[b]
A. Author[a] , B. Glass[b], R. Trautner[b]

[a]ONERA, 31055, Toulouse, France
[b]Sofradir, 38113, Veurey-Voroize, France

laurent.artola@onera.fr

Abstract

This work presents a SEE prediction tool called MUSCA SEP3 and its interest in failure investigations and in providing a help for designers with the aim to optimize the SEE sensitivity of Sofradir readout circuit. Estimations and a failure analysis at circuit level were presented. Comparisons between predictions and experimental data obtained under heavy ion are consistent. The analysis of critical areas of the DFF design allows to propose hardening techniques with the aim to reduce the SEE sensitivity of the D Flip-Flop (D- FF) of the readout circuit.

I. INTRODUCTION

Image sensors are widely used in spacecraft for many applications [1][2]. Photonic imager technology has been developed for wavelength responses that range from ultraviolet, through visible, to infrared. Most radiation effects studies have been made on infrared detectors, and visible/near infrared technologies such as charge coupled device (CCD), charge injection devices (CID) and active pixel sensors (APS). Among many optical applications, like earth or space observation, the guidance system in a spacecraft (launcher or satellite) is particularly critical. Then, the reliability of such guidance systems based on image sensors is essential for the space mission.

CMOS (Complementary Metal Oxide Semiconductor) technology is mainly used in the readout circuit of photonic integrated circuits (ICs). However, CMOS technology is known to be sensitive to single event effects (SEE), such as single event transient (SET) [2]. SETs can be induced by various ionizing particles, i.e., heavy ions, protons, electrons the space radiation environment [3]. SETs can become critical for image devices and ICs boarded in flight because of their critical applications. Actually, SETs in D Flip-Flop can change the logic state and disturb the nominal behavior of the readout circuit.

One of the interests of prediction tools, such as MUSCA SEP3 (MUti-SCAle Single Event Phenomena Prediction Platform) [4][5], is to anticipate the sensitivity trends with the aim to help the designers to select the best layout considering of performances and reliability. Moreover, these investigations lead to reduce the number of testing runs during the qualifications of electronics under high energy particles such as heavy ions.

In this work is presented the interest of such approach to understand the failure origins at transistor level with the aim to be able to harden circuits of the readout system of photonic devices. This work presents an optimized design of the reference DFF used in the readout circuit of a infrared (IR) device, designed by Sofradir. The gain in term of SEU sensitivity is shown while the penalties in term of area and power consumption are non-existent, quite the opposite.

II. SEE PREDICTION TOOL

A. Simulation flow of the prediction tool

MUSCA SEP3 is a SEE prediction tool based on a Monte-Carlo approach which allows a complete simulation from the interaction of the radiation particles with the matter to the occurrence of the soft error in the IC [4][5] as shown in the figure 1. These simulations use nuclear databases (issued from GEANT-4 calculations) in order to describe in 3D the interactions (nuclear and Colombian) of radiation particles, such as, heavy ions, protons, neutrons, or muons, with the materials of the Back-End Of Line (BEOL). The modeling of transport and collection mechanisms is based on dynamic ambipolar diffusion, multi dynamic collection, and bipolar amplification. Details of analytical models of transport and collection mechanisms are presented in details in previous works [6][7]. The effects of bias voltage, the layout, and the fabrication processes are taken into account with the aim to build a realistic SET currents database. The modeling of the Front-End Of Line (FEOL) is based on the description (dimensions and locations) of active implants, i.e., drain and source of each n-MOS and p-MOS transistor directly extracted from GDS files. The process of the extraction of collection areas from the layout file has been presented in a previous work [8]. All required layout files and electrical models were provided by Sofradir. Next, this SET currents database is injected on each corresponding node at transistor level for an electrical simulation with Spectre simulator with the aim to estimate the soft error response of the circuit. The electrical transient simulations of the parasitic circuit were performed by the Spice simulations [9]. As previously, the schematic of the cells and the model cards of n-MOS and p-MOS transistors are provided by Sofradir.

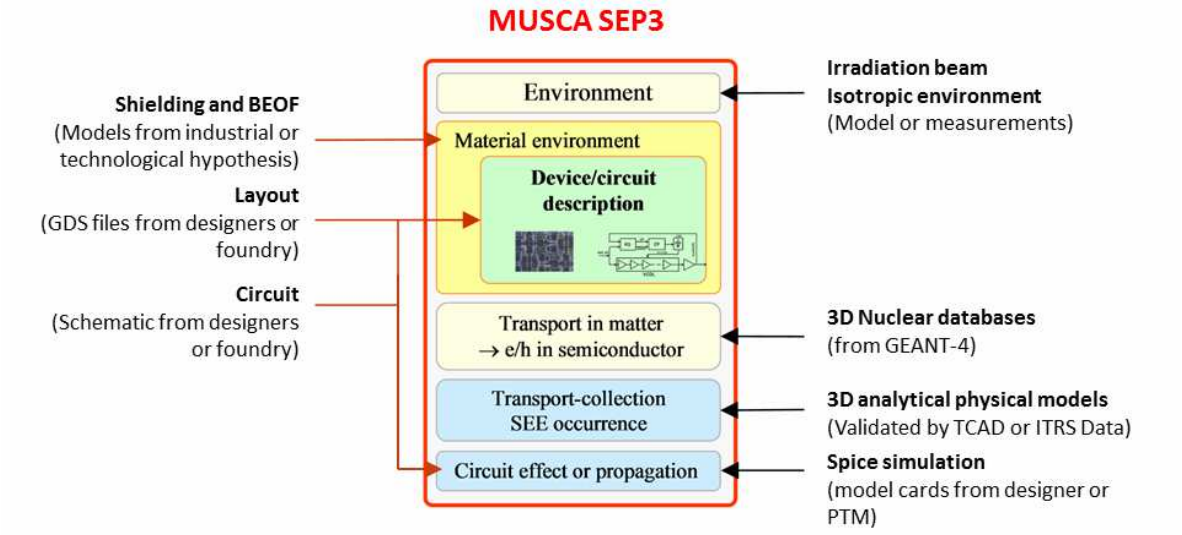
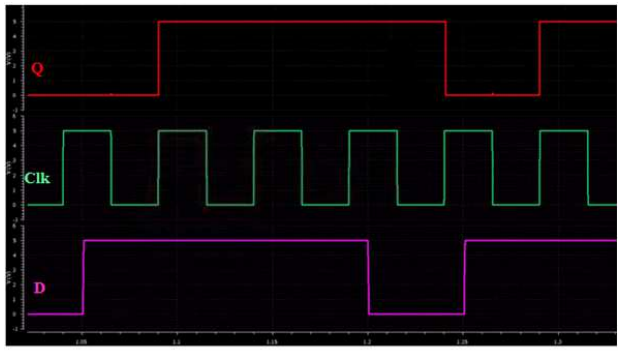
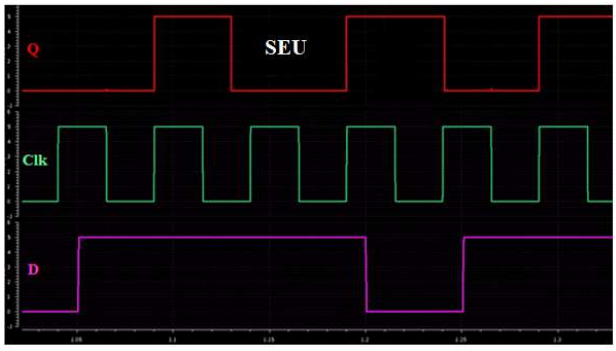


Figure 1: Simulation flow of the SEE prediction tool, MUSCA SEP3

An upset event is considered during the electrical simulation if the output signal Q changes of logic state ("1" to "0" or "0" to "1") while it should not. The chronograms of input, output and clock signals illustrate the SEU detection based on the electrical simulations, and are shown in the figure 2(a). It presents the nominal behavior of the DFF cell synchronized by the clock signal (i.e. Clk) of 20 MHz. On the other hand, the figure (b) reveals a SEU occurrence on the output signal (Q) induced by an incident heavy ion on the DFF cell. The output signal decreases from 5V (state "1") down to 0V (state "0") until the next rising edge of the clock signal.



(a)



(b)

Figure 2: Chronograms of input, D (in pink), output Q (in red), and clock Clk (in green) signal of the DFF in (a) nominal behavior and (b) impacted by a SEU.

Based on this simulation framework, MUSCA SEP3 is able to propose an estimation of the SEU sensitivity (SEU cross section, but also event mapping) of the DFF cells designed by Sofradir.

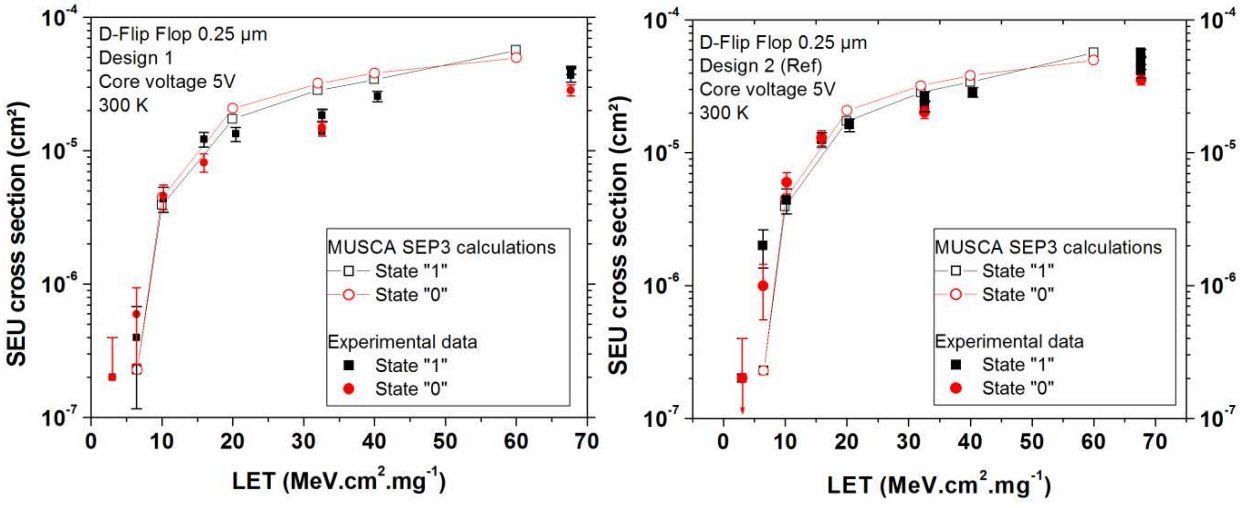
B. Comparison with experimental data under heavy ions

The experimental SEU test vehicle was developed by Sofradir and contains 2 main blocks. First a sequential block with 6 designs of shift registers are sharing Clock, Reset, Data input and Enable signals. Each shift register is composed by 200 cells of one design of flop and has its own clock gate and related clock tree. This leads to minimize the impact of the SEU over a unique and global clock tree. The second main block contains 2 x 350 arrays of memory point in shift configuration. In this work, only the sensitivity of sequential blocks is investigated. Even if all the designs were tested, in this work only two designs will be investigated because of their main uses in CMOS functions in Sofradir infrared image sensors.

The SEU test measurements have been performed during two campaigns in June 2014 and May 2015 in UCL (Université Catholique de Louvain) heavy ion test facility in Belgium. The CYClotron of Louvain la NEuve (CYCLONE) is a multi-particle, variable energy. Available heavy ions species are split in two "Ion cocktails", named M/Q= 5 and M/Q 3.3 for a range of LET from 1.1 MeV.cm^2.mg^{-1} up to 67.7 MeV.cm^2.mg^{-1}

The comparisons of experimental data and MUSCA SEP3 calculations at 300 K have been performed for 2 designs of DFF used in the readout circuit.

Good correlations in terms of LET threshold and SEE saturation of cross section are proposed, as presented in the figure 3(a) and the figure 3 (b) for the two design of DFF respectively, i.e., design 1 and design 2 (the reference design). Error bars represent the standard deviation.



(a) (b)

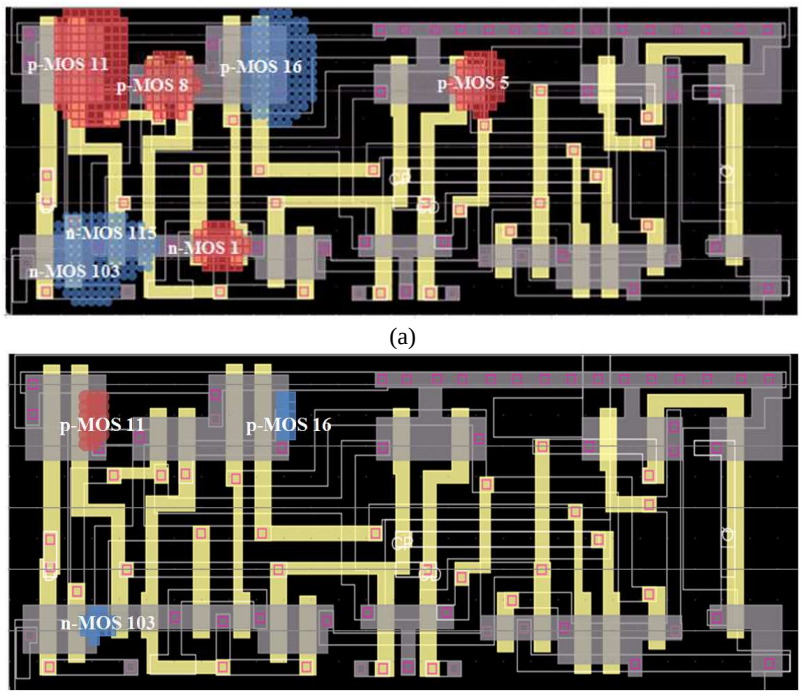
Figure 3: Comparison of experimental data with MUSCA SEP simulations f the SEU cross section of DFF for the design 1 (a) and design 2 (b), as a function and logic state, under heavy ion irradiation at UCL facility at 300 K.

After this presentation of the relevance of the prediction tool, the next section will show the failure analysis performed on the DFF cells. Actually, the other main interest of prediction tools is to allow a failure analysis at layout level with the aim to identity critical areas of the circuit.

III. Failure Analysis Dedicated for SEU Hardening

These failure analyses based on sensitivity mappings can be really useful for designers in order to determine which transistors of the cell are critical and to anticipate design optimizations. But, the kind of analysis can be also interesting to improve test plan of irradiation campaign in order to reduce the cost of space qualification of embedded devices. In previous works, MUSCA SEP3 had already shown the relevance of the estimated critical areas of SEU [10] but also for SEL (Single Event latchup) [11].

In this work, the simulation results highlight that the transistors of the input of the cell are more sensitive than the transistors of the output of the flip-flop cell as shown in figure 4. It is interesting to note that even if the global SEE cross sections are quite equivalent (Cf. Fig. 3) for the two stored logic states in the DFF, i.e., state “1” and state “0”, the locations of critical areas are strongly different.

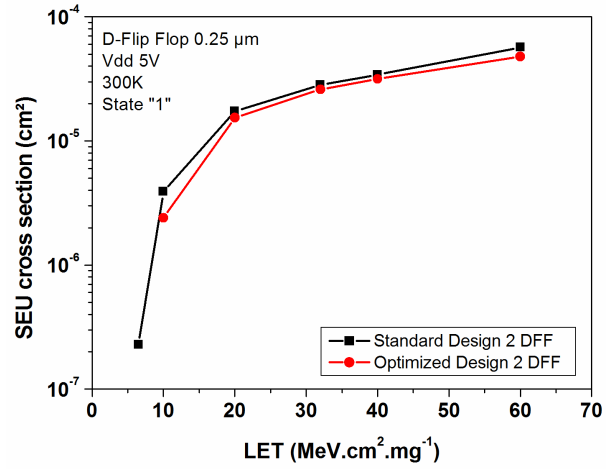


(a)

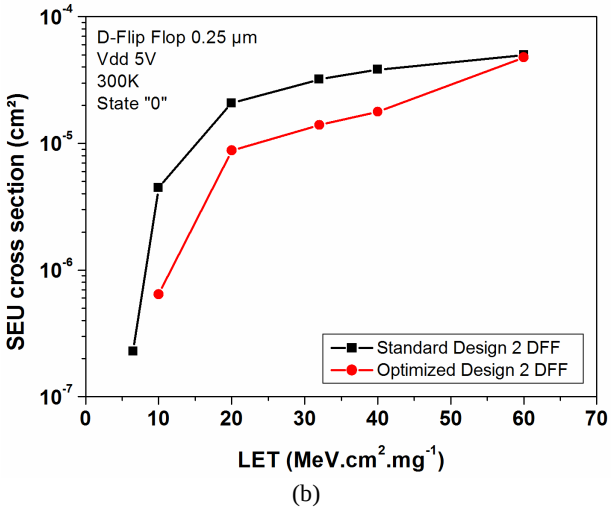
(b)

Figure 4: SEU sensitivity mappings obtained by MUSCA SEP3 calculations for the standard design of the DFF (design 2) for an ion with a LET of 58 MeV.cm^2.mg^{-1} (a) and with a LET of 10 MeV.cm^2.mg^{-1} (b), as a function of stored data: “1” (red squares) “0” (blue dots) at 300 K.

The analysis of this failure mapping at transistor level combined with the monitoring of SET on different internal nodes of the DFF cell allows for proposing design optimization. This optimization of the design cell is focus on the wider sensitive transistors, i.e., p-MOS 11 p-MOS 16, n-MOS 103, and the physical associated transistors (because of design rules). The initial cell area is kept, while the width of 6 transistors (4 p-MOS and 2 n-MOS) is decreased. This optimization allows for reducing the global power consumption of the DFF cell. Actually a decrease in width of these transistors induces a decrease in the drive current and so a decrease in the power consumption of the DFF cell during the transient states.



(a)



(b)

Figure 5: Comparisons of SEU cross sections between standard DFF design (black squares) and optimized design (red dots) at "state “1” (a) and state "0" (b) obtained by MUSCA SEP3 calculations for heavy ions for a range of LETs from 6.6MeV.cm^2.mg^{-1} up to 58.8MeVcm^2.mg^{-1}.

The figure 5 presents the comparison of the SEU cross section between standard design (black squares) and optimized design obtained by MUSCA SEP3 calculations for an ions with a range of LETs from 6.6 MeV.cm^2.mg^{-1} up to 58 MeV.cm^2.mg^{-1} at state "1" (a) and state "0" (b). The proposed design allows to reduce the SEU sensitivity of the DFF cell at all the LETs of the heavy ions. The figure 6 shows the percentage of the improvements of the SEU cross section obtained for the optimized design for the state "1" and state "0" stored as a function of the LETs. The LET threshold of the optimized DFF is increased by a factor of 1.5X, corresponding to an increase from 6.6 to 10 MeV.cm^2.mg^{-1}. It is interesting to note that the improvement in the robustness of the optimized DFF is more significant at state "0" than state "1". The difference is mainly due to the complete immunity of p-MOS 16 at state "0" for low LETs while n-MOS 1 is still sensitive at state "1". Actually, the higher sensitivity of n-MOS 1 at state "1" in the optimized DFF design is induced by the lower drive current provided by the adjacent p-MOS transistor of p-MOS 16.

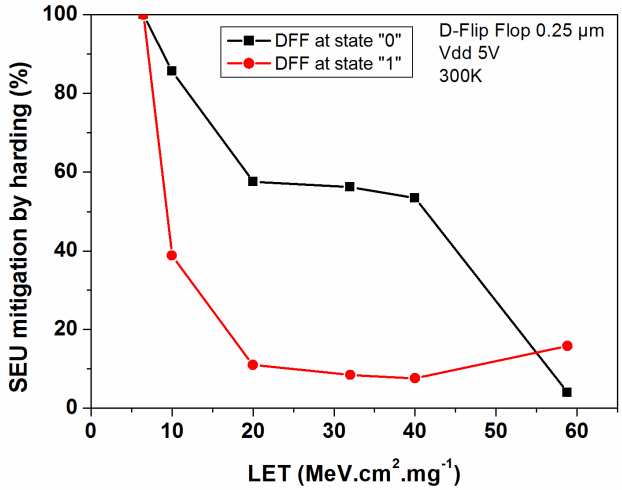


Figure 6: Percentage of SEU mitigation obtained for the optimized design of the DFF obtained at state "0" (black squares) and at state "1" (red dots) by MUSCA SEP3 simulation for heavy ions for a range of LETs from 6.6MeV.cm^2.mg^{-1} up to 58.8MeVcm^2.mg^{-1}.

IV. Conclusions

This work presents an SEE prediction tool and its interest in failure investigations and in providing a help for designers with the aim to optimize the SEE sensitivity of DFF cells used in the readout circuit developed by Sofradir. Estimations and a failure analysis at circuit level are presented considering the stored data configuration. Comparisons between predictions and experimental data obtained under heavy ion at UCL facility are consistent. The failure analysis allows for determining the critical transistors of the DFF cell with the aim to help designers to mitigate SEU by design optimization. Finally, an optimized design of the DFF cell is proposed and evaluated. The interest in term of SEU robustness is presented while the power consumption is also decreased and none area penalty is induced. The LET threshold of the new design is increased by a factor of 1.5X, while the mitigation of the SEUs varies from 85% to 10% depending on LETs and stored state. Actually, because of electrical feedback effects, the optimized design is more relevant when the state "0" is stored in the DFF.

In future works other DFF designs will be investigated and hardened with the aim to improve the global reliability

of the readout circuit of the new generation of IR device developed by Sofradir.

V. REFERENCES

[1] G. R. Hopkinson, (2000, Dec.) "Radiation effects in CMOS active pixel sensor", IEEE Trans. Nucl. Sci., vol. 47, no, 6, pp. 2480 - 2484.

[2] C. Virmontois, A. Toulemont, G. Rolland, A. Materne, V. Lalucaa, V. Goiffon, C. Codreanu, C. Durnez, A. Bardoux, (2014, Dec.) " Radiation-Induced Dose and Single Event Effects in Digital CMOS Image Sensors" IEEE Trans. Nucl. Sci., vol. 61, no. 6, pp. 3331-3340.

[3] D. Falguere, D. Boscher, T. Nuns, S. Duzellier, S. Bourdarie, R. Ecoffet, S. Barde, J. Cueto, C. Alonzo and C. Hoffman , (2002, Dec.) "In-flight observations of the radiation environment and its effects on devices in the SAC-C polar orbit", IEEE Trans. Nucl. Sci., vol. 49, no. 6, pp.2782 -2887.

[4] G. Hubert, S. Duzellier, C. Inguimbert, C. Boatella-Polo, F. Bezerra, R. Ecoffet, (2009, Dec.) "Operational SER Calculations on the SAC-C Orbit Using the Multi-Scales Single Event Phenomena Predictive Platform (MUSCA SEP3)" IEEE Trans. Nucl. Sci., nol. 56, no. 6, pp. 3032-3042.

[5] G. Hubert, L. Artola, (2013, Dec.) "Single-Event Transient Modeling in a 65-nm Bulk CMOS Technology Based on Multi-Physical Approach and Electrical Simulations", IEEE Trans. Nucl. Sci., vol. 60, no.6, pp. 4421-4429.

[6] L. Artola, G. Hubert, S. Duzellier and F. Bezerra (2010, Aug.) "Collected charge analysis for a new transient model by TCAD simulations in 90-nm technology", IEEE Trans. Nucl. Sci., vol. 57, no. 4, pp.1869 -1875.

[7] L. Artola, G. Hubert, K. M. Warren, M. Gaillardin, R. D. Schrimpf, R. A. Reed, R. A. Weller, J. R. Ahlbin, P. Paillet, M. Raine, S. Girard, S. Duzellier, L. W. Massengill and F. Bezerra, (2011, June) "SEU prediction from SET modeling using multi-node collection in bulk transistors and SRAMs down to the 65-nm technology ode", IEEE Trans. Nucl. Sci., vol. 58, no. 3, pp. 1338 -1346..

[8] L. Artola, M. Gaillardin, G. Hubert, M. Raine, and P. Paillet, (2015, Aug.) "Modeling single event transients in advanced devices and Ics", IEEE Trans. Nucl. Sci, vol. 62, no. 04. p.. 1528-1539.

[9] "Spice simulator," [Online]. Available: http://embedded.eecs.berkeley. edu/pubs/downloads/spice/index.htm.

[10] G. Hubert, D. Truyen, L. Artola, M. Briet, C.H. Heng, Y. L. Lakys, E. Leduc, (2014, Dec.) "SET and SEU Analyses Based on Experiments and Multi-Physics Modeling Applied to the ATMEL CMOS Library in 180 and 90-nm Technological Node", IEEE Trans. Nucl. Sci., vol. 61, no. 6, pp. 3178-3186.

[11] L. Artola, G. Hubert, and T. Rousselin, (2014, Dec.) "Single-Event Latchup Modeling Based on Coupled Physical and Electrical Transient Simulations in CMOS Technology' IEEE Trans. Nucl. Sci., vol. 61, no. 6, pp. 3543-3549.

DSP Day: Trends in space based Digital Signal Processing

DSP Day: DSP IP cores and related IP including NoC

DSP Day: DSP software, tools and libraries

DSP Day: Rad-hard DSP chips and boards

DSP Day: COTS DSP chips and boards

DSP Day: Test, Verification and Qualification of DSP chips

DSP Day: Requirements and Needs for future space DSPs

DSP Day: Other topics

DSP Day: Poster Session

DSP Day: DSP and FPGA

DSP Day: DSP applications