Title: **Development of a Digital Temperature Transducer ASIC in a 28 nm FD-SOI CMOS Process for a Spaceborne Low Power Sensor Bus**

Abstract Content

A large geostationary satellite typically employs several hundred resistive temperature sensors for housekeeping tasks. These sensors are point-to-point wired to an acquisition unit, which is often a single central interrogator system. This poses a need to develop solutions that can reduce harness complexity and mass, while maintaining high reliability and keeping low cost and power consumption of the solution in mind. Digital temperature sensors fabricated as integrated circuits (IC) have become a popular choice for use in thermal management systems. The temperature sensor and the digital interface circuitry for bus-type interfaces are integrated on a single chip; thus, enabling modularity and simplicity in the system design. Implementing a sensor network, in which the point-to-point connected resistive sensors are replaced with serially connected digital temperature sensors, can result in a significant reduction in the amount of wiring. The selection of a suitable semiconductor process technology for designing such sensors is very crucial. The 28 nm Fully-Depleted Silicon on Insulator (FD-SOI) CMOS process of STMicroelectronics offers many attractive features, namely, fast switching, poly biasing and back-gate biasing for power regulation, and expected latch-up immunity. Additionally, some indications suggest a sufficiently high total ionizing dose (TID) radiation tolerance, which makes this technology suitable for the development of circuits for space applications.

In this paper, we discuss the system-level requirements of a low-power digital temperature transducer application-specific integrated circuit (ASIC); it is currently under development in the said CMOS process. We also present the ongoing design activities to meet the challenges of the space application. The ASIC will become a part of such a low power sensor bus system of a future spacecraft, where all the serially connected transducer ICs will communicate with a central interrogator module. The targeted temperature range, to be measured with an effective resolution of 0.1 °C, is from -40 °C to +125 °C. A worst case measurement inaccuracy of ±1 °C is specified for the spacecraft's operational temperature range of -20 °C to +20 °C. For the measurement of temperatures outside this range, a maximum inaccuracy of ±3 °C is required. Different system-level and circuit-level techniques will be exploited to achieve low power operation of the ASIC. Design-level mitigation strategies for non-destructive single event effects (SEE), such as triplicated combinatorial logic and triplicated registers, will be also employed.

Among the various temperature sensing elements proposed in the literature, most of the state-of-the-art digital temperature sensors employ parasitic bipolar transistors. With a single-point thermal calibration, inaccuracies less than ±0.2 °C have been reported for such sensors. The speed of temperature sensors is limited by the thermal time constants of their packages; which are typically in the order of a few seconds. Therefore, sigma-delta analog-to-digital converters (ADC) are popularly used in such sensors because of their ability to trade low speed for high resolution. On the system-level, the temperature transducer ASIC discussed in this paper, consists of three major design blocks: a bipolar transistor-based temperature sensor, a sigma-delta ADC, and a digital serial communication interface. Additionally, circuit blocks for the generation of the internal bias currents and low power digital calibration are included. A resolution of 14 effective number of bits (ENOB) is specified for the sigma-delta ADC. This ADC is being developed in the scope of "Thin but Great Silicon to Design Objects" (THINGS2DO) – under the ENIAC framework.

In line with the development of this temperature transducer ASIC, a 1st order sigma-delta modulator and its constituent operational transconductance amplifier (OTA) have been integrated as test structures on an IC called "AMBER1". The IC is realized to explore the low power features of the 28 nm FD-SOI technology. Most of the analog and mixed signal blocks are powered by a 1.0 V nominal supply. For digital input/output (IO) signals a supply voltage between 1.5 V and 1.8 V is required for the IO ring. It was taped-out in November 2015 and its silicon validation is planned for the mid of 2016.

Summary

We discuss the system-level requirements of a low-power digital temperature transducer application specific integrated circuit (ASIC); it is currently under development in the 28 nm FD-SOI CMOS process of STMicroelectronics. We also present the ongoing design activities to meet the challenges of the space application. The targeted temperature range, to be measured with an effective resolution of 0.1 °C, is from -40 °C to +125 °C. A worst case measurement inaccuracy of ±1 °C is specified for the spacecraft's operational temperature range of -20 °C to +20 °C. For the measurement of temperatures outside this range, a maximum inaccuracy of ±3 °C is required. On the system-level, this temperature transducer ASIC consists of three major design blocks: a bipolar transistor-based temperature sensor, a 14 bit sigma-delta analog-to-digital converter (ADC), and a digital serial communication interface. Additionally, circuit blocks for the generation of the internal bias currents and low power digital calibration are included. In line with the development of this temperature transducer ASIC, a 1st order sigma-delta modulator and its constituent operational transconductance amplifier (OTA) have been integrated as test structures on an integrated circuit (IC) called "AMBER1". It was taped-out in November 2015 and its silicon validation is planned for the mid of 2016.