Development of a Digital Temperature Transducer ASIC in a 28 nm FD-SOI CMOS Process for a Spaceborne Low Power Sensor Bus

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THINGS2DO

eniac JOINT UNDERTAKING

Bundesministerium für Bildung und Forschung

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Agenda

- Background
- 28 nm FD-SOI Technology
- System Requirements
- System Description
- Demonstrator
- Conclusion

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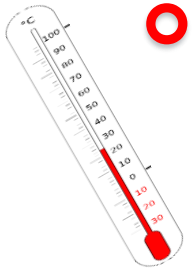
Background

Housekeeping in Geostationary Satellites

Housekeeping Data tells:

- where the satellite is pointing
- which parts are working properly
- what its **temperature** is



°C

Source: spac0255, NOAA In Space Collection

Image Courtesy: NASA

Importance of temperature sensing

- Large temperature difference
- To support the onboard Thermal Control System
- Temperature requirements of equipments for reliable operation

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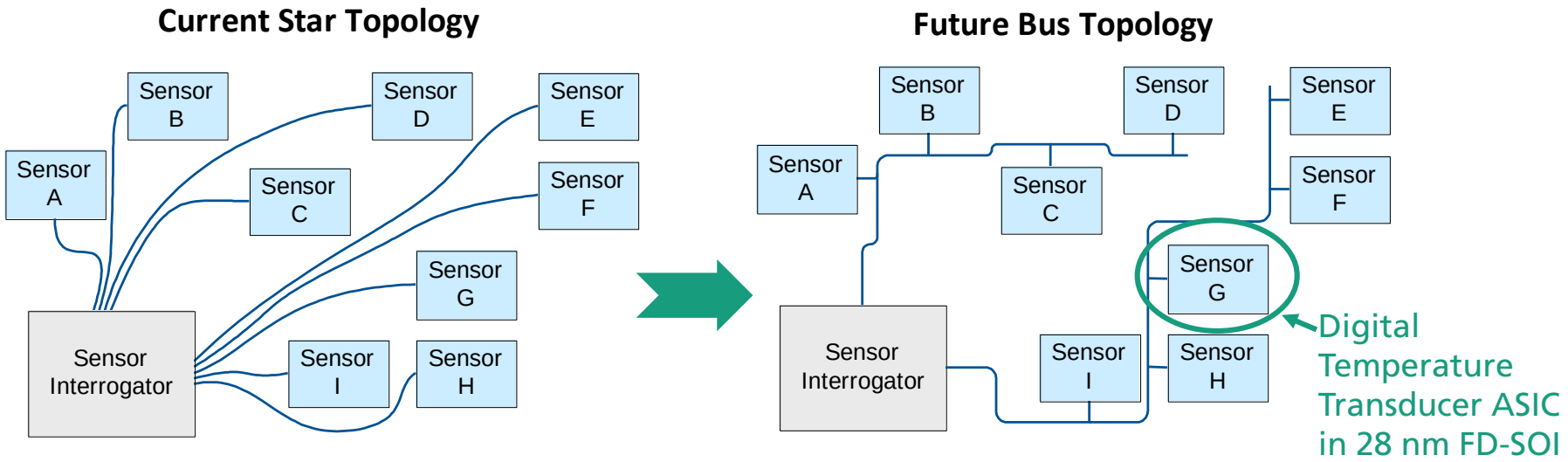
Background
Conventional vs Serial Sensor Network



Conventional Sensor Network

- Star topology
- Lot of cables
- Extra weight
- Inflexible for future

Future Sensor Bus System

- Hybrid Bus topology
- Serial Bus line: reduction in wiring
- Electrical and fiber optical sensor network

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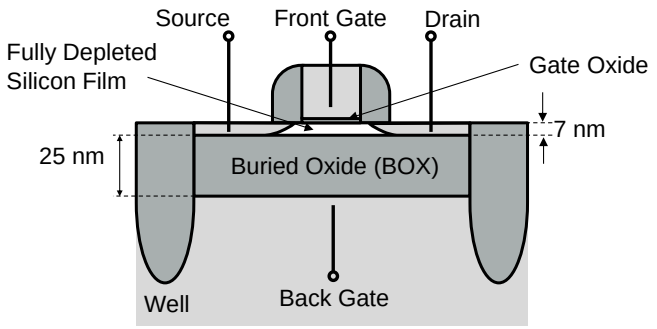
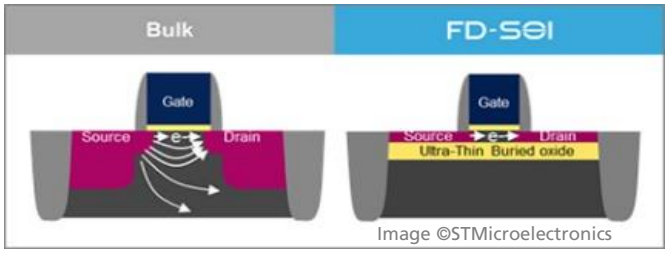
28 nm FD-SOI Technology
Process Features

- Characteristics [1]
  - Low C_{ds} and $I_{leakage}$
  - High Speed (LVT, Forward BB)
  - Low leakage (RVT, Reverse BB)
  - High Body-biasing tuning range and sensitivity [3]
  - Robust against latch-up

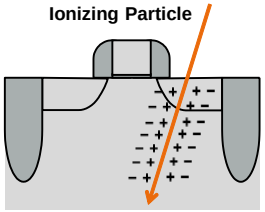




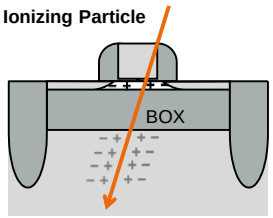
[2]

Bulk CMOS versus FD-SOI CMOS

- Radiation tolerance
  - Thin front oxide
  - Reduced sensitive volume
  - Robust against SEL
  - High TID tolerance due to 25 nm BOX



Bulk transistor



FD-SOI transistor

[1] S. Shopov, S.P. Voinigescu, "Characterization of the High Frequency Performance of 28-nm UTBB FDSOI MOSFETs as a Function of Backgate Bias", Compound Semiconductor Integrated Circuit Symposium (CSICs), 2014 IEEE
[2] http://cmp.imag.fr/documents/doc/UTBB-FDSOI%20Design%20and%20Migration%20Methodology_.pdf
[3] S. Le Tual et al, "A 20GHz-BW 6b 10GS/s 32mW Time-Interleaved SAR ADC with Master T&H in 28nm UTBB FDSOI Technology", ISSCC2014

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System Requirements

Temperature Range	-40 °C to +125 °C
Accuracy	±1 °C in [-20 °C, +20 °C] and ±3 °C outside
Measurement Resolution	0.1 °C
ADC Resolution	≥ 11 bits
SEU LET threshold	≥ 20 MeV·cm²/mg
TID tolerance	≥ 300 krad
Interface type	Serial (I^2C)
Lifetime	15 years in-orbit operation

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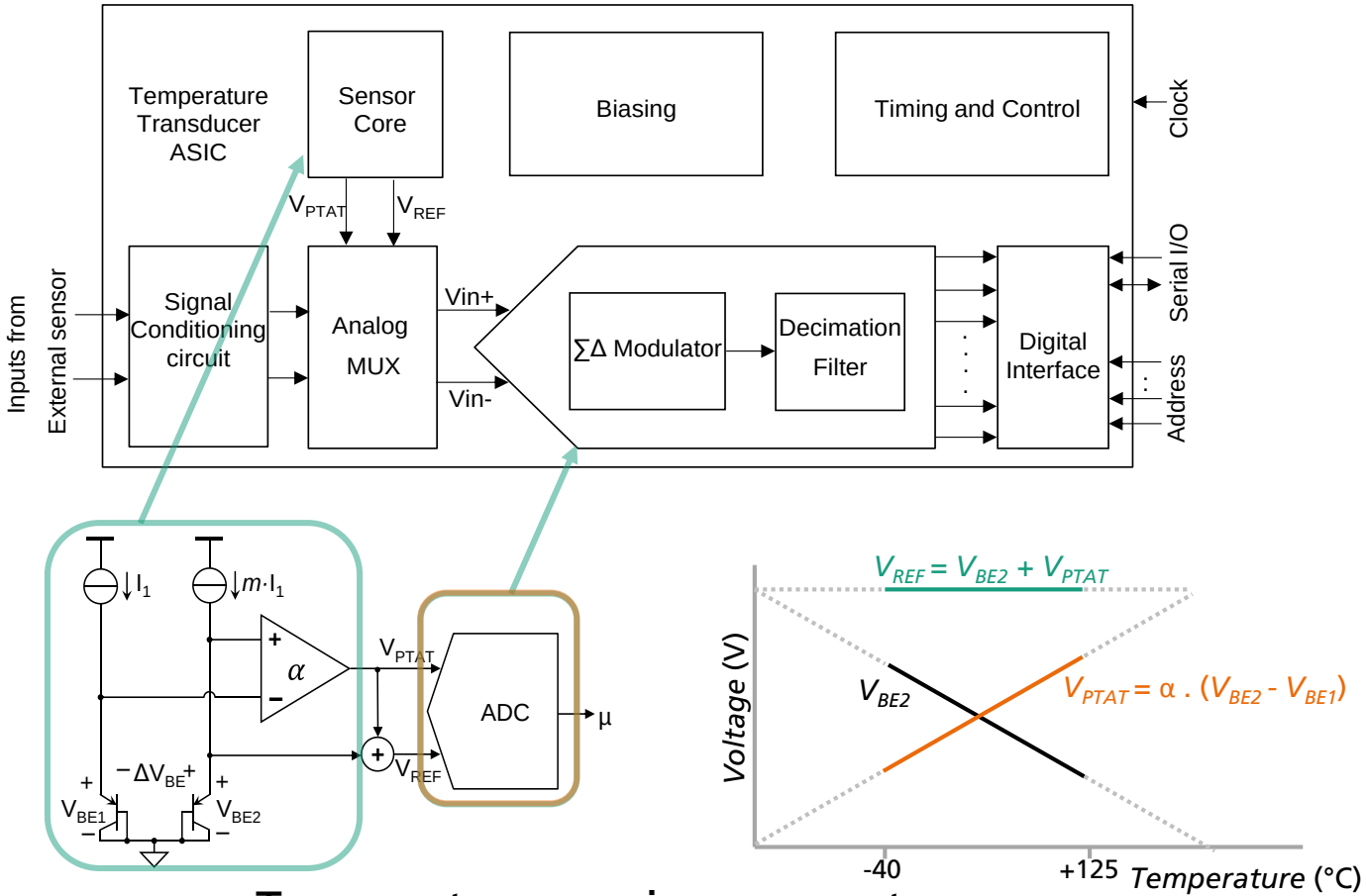
System Description
Block Diagram

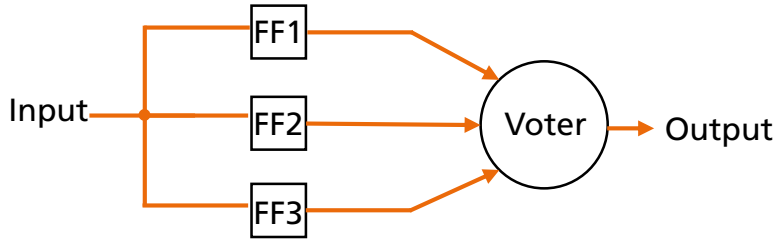


Temperature sensing concept

System Description
Radiation Hardening

System-level

- Redundancy techniques



Circuit-level

- Optimal transistor sizing
- Offset-compensation
- Back gate biasing

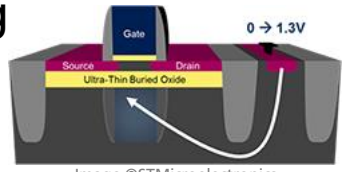
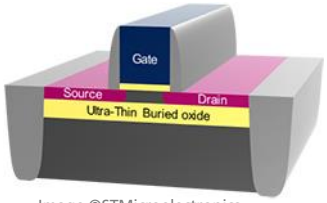


Image ©STMicroelectronics

Device-level

- FD-SOI CMOS technology



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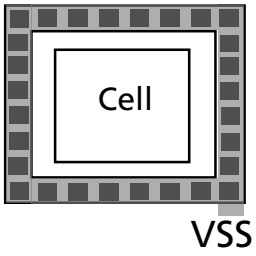
Layout-level

- Placement of guard-rings



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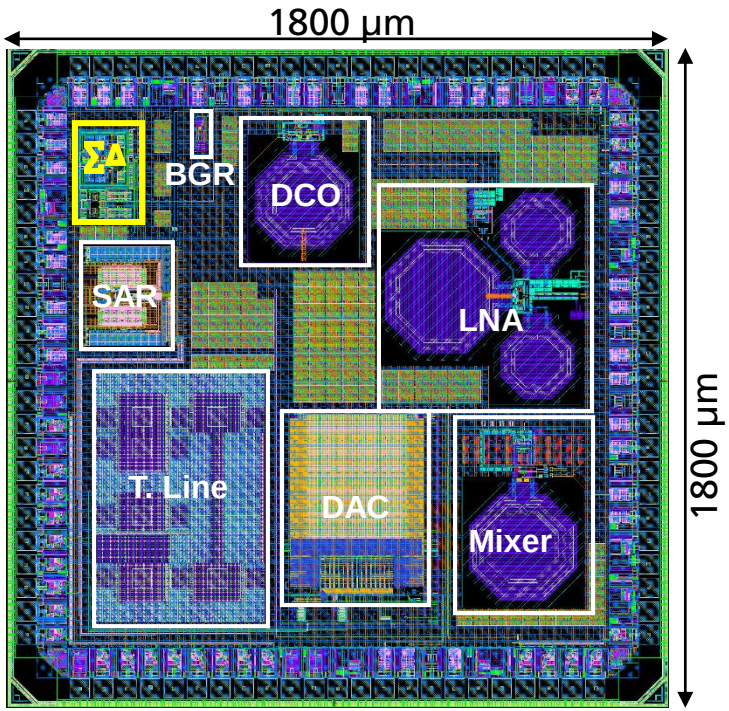
Demonstrator
AMBER1: Top Level

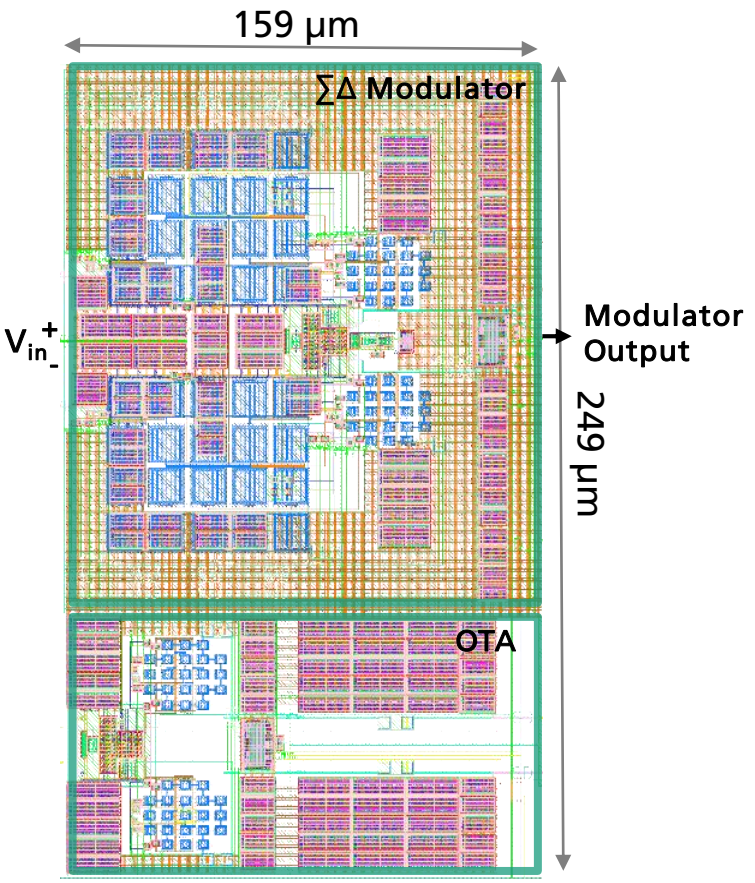
- Developed under THINGS2DO project
- Aim:
  - Validate core design components
  - Validate process features (Body-biasing, Passive devices)
- 92 pins, QFN 100 package
- 1.0 V (Core) and 1.8 V (I/O) Supplies
- Features design blocks for:
  - **∑Δ Modulator,** SAR ADC, DAC, LNA, DCO, Mixer, Transmission line, Band Gap Reference.



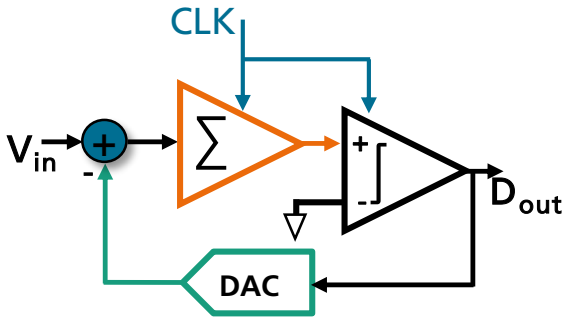
Demonstrator
Sigma-Delta Modulator

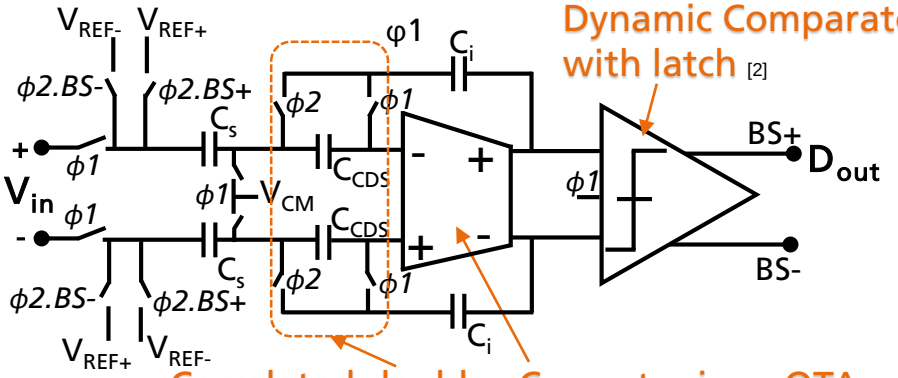
- Modulator:
  - Operation voltage 1.0 V (nominal)
  - Fully-differential
  - 1st order, discrete time
  - 1-bit quantization
  - Bandwidth = 500 Hz
  - $f_{sampling}$ = 200 kHz
  - Symmetrical Layout

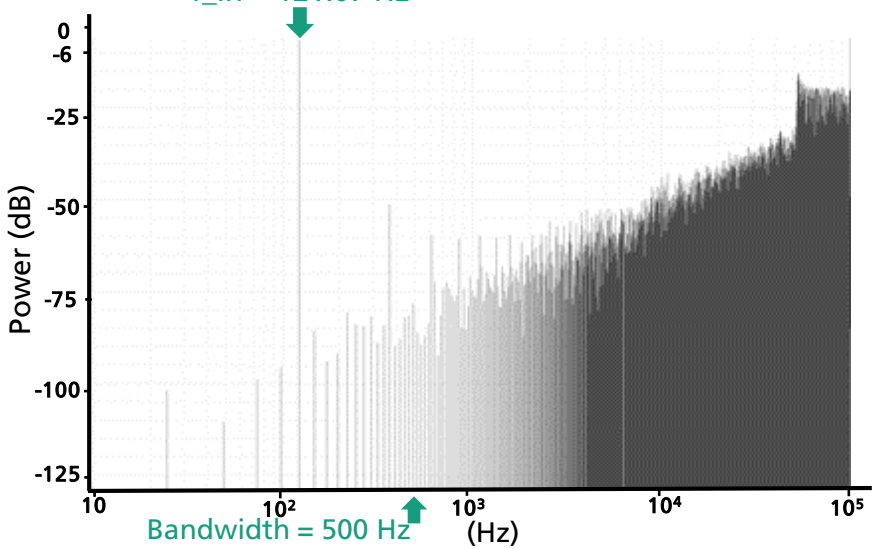
- Operational Transconductance Amplifier
  - DC Gain = 65 dB
  - Gain Bandwidth = 20 MHz



Demonstrator
Sigma-Delta Modulator







Input Amplitude	1.0 V_{PP} (½ Full Scale)
ENOB	7.14 bits
SINAD	44.78 dB
SNR	64.94 dB
SFDR	44.82 dB
Power	64 µW (1.0 V Supply)

[1] Enz, Christian C., and Gabor C. Temes. "Circuit techniques for reducing the effects of op-amp imperfections: autozeroing, correlated double sampling, and chopper stabilization." *Proceedings of the IEEE* 84.11 (1996): 1584-1614.

[2]Roh, Jeongjin, et al. "A 0.9-V 60-µW 1-bit fourth-order delta-sigma modulator with 83-dB dynamic range." Solid-State Circuits, *IEEE Journal of* 43.2 (2008): 361-370.

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Conclusion

- Digital Temperature Transducer ASIC:
  - Sensing, data-conversion and communication
- 28 nm FDSOI CMOS Process:
  - Reduced parasitics, back-gate biasing, good radiation tolerance
- System Requirements:
  - Up to ±1 °C accuracy in [-20 °C, +20 °C] with 0.1 °C resolution
- Demonstrator: AMBER1 IC
  - ∑Δ Modulator:1st order, discrete-time, correlated double sampling
- Next Steps:
  - Validate 1st order ∑Δ Modulator on AMBER1 IC
  - Integrate sensor core and digital circuitry
- Outlook:
  - Digital intensive design: exploit low-power features of 28 nm FD-SOI CMOS process
  - Further integration of components for space applications based on FD-SOI

THANK YOU