Development of a Digital Temperature Transducer ASIC in a 28 nm FD-SOI CMOS Process for a Spaceborne Low Power Sensor Bus

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13.06.2016

This work is funded through project THINGS2DO under the ENIAC grant agreement number 621221 and the national grant agreement number 16ES0240.
Agenda

- Background
- 28 nm FD-SOI Technology
- System Requirements
- System Description
- Demonstrator
- Conclusion
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Background
Housekeeping in Geostationary Satellites

Housekeeping Data tells:
- where the satellite is pointing
- which parts are working properly
- what its temperature is

Importance of temperature sensing
- Large temperature difference
- To support the onboard Thermal Control System
- Temperature requirements of equipments for reliable operation
Background
Conventional vs Serial Sensor Network

Conventional Sensor Network
- Star topology
- Lot of cables
- Extra weight
- Inflexible for future

Future Sensor Bus System
- Hybrid Bus topology
- Serial Bus line: reduction in wiring
- Electrical and fiber optical sensor network

Current Star Topology

Future Bus Topology

Digital Temperature Transducer ASIC in 28 nm FD-SOI
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28 nm FD-SOI Technology

Process Features

- Characteristics [1]
  - Low $C_{ds}$ and $I_{leakage}$
  - High Speed (LVT, Forward BB)
  - Low leakage (RVT, Reverse BB)
  - High Body-biasing tuning range and sensitivity [3]
  - Robust against latch-up

- Radiation tolerance
  - Thin front oxide
  - Reduced sensitive volume
  - Robust against SEL
  - High TID tolerance due to 25 nm BOX

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## System Requirements

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Range</td>
<td>-40 °C to +125 °C</td>
</tr>
<tr>
<td>Accuracy</td>
<td>±1 °C in [-20 °C, +20 °C] and ±3 °C outside</td>
</tr>
<tr>
<td>Measurement Resolution</td>
<td>0.1 °C</td>
</tr>
<tr>
<td>ADC Resolution</td>
<td>≥ 11 bits</td>
</tr>
<tr>
<td>SEU LET threshold</td>
<td>≥ 20 MeV·cm²/mg</td>
</tr>
<tr>
<td>TID tolerance</td>
<td>≥ 300 krad</td>
</tr>
<tr>
<td>Interface type</td>
<td>Serial (I²C)</td>
</tr>
<tr>
<td>Lifetime</td>
<td>15 years in-orbit operation</td>
</tr>
</tbody>
</table>
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System Description
Block Diagram

Temperature sensing concept

\[ V_{REF} = V_{BE2} + V_{PTAT} \]

\[ V_{PTAT} = \alpha \cdot (V_{BE2} - V_{BE1}) \]

\[ V_{BE2} \]

\[ -40 \quad +125 \quad \text{Temperature (°C)} \]
System Description

Radiation Hardening

System-level
- Redundancy techniques

![Diagram of FF1, FF2, FF3 connected to a Voter and Output]

Circuit-level
- Optimal transistor sizing
- Offset-compensation
- Back gate biasing

Device-level
- FD-SOI CMOS technology

![Image of FD-SOI CMOS technology]

Layout-level
- Placement of guard-rings

![Image of guard-rings]
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Demonstrator
AMBER1: Top Level

- Developed under THINGS2DO project
- Aim:
  - Validate core design components
  - Validate process features (Body-biasing, Passive devices)
- 92 pins, QFN 100 package
- 1.0 V (Core) and 1.8 V (I/O) Supplies
- Features design blocks for:
  - $\Sigma \Delta$ Modulator, SAR ADC, DAC, LNA, DCO, Mixer, Transmission line, Band Gap Reference.
Demonstrator
Sigma-Delta Modulator

- **Modulator:**
  - Operation voltage 1.0 V (nominal)
  - Fully-differential
  - 1\textsuperscript{st} order, discrete time
  - 1-bit quantization
  - Bandwidth = 500 Hz
  - \( f_{\text{sampling}} = 200 \text{ kHz} \)
  - Symmetrical Layout

- **Operational Transconductance Amplifier**
  - DC Gain = 65 dB
  - Gain Bandwidth = 20 MHz
Demonstrator Sigma-Delta Modulator

CLK

\[ V_{\text{in}} \] \[ + \] \[ \sum \] \[ - \] \[ D_{\text{out}} \]

Dynamic Comparator with latch

Current-mirror OTA

Correlated-double Sampling (CDS)

\[ f_{\text{in}} = 121.07 \text{ Hz} \]

\[ \text{Input Amplitude} \ | \ 1.0 \text{ V}_{\text{pp}} \ (\frac{1}{2} \text{ Full Scale}) \]

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>ENOB</td>
<td>7.14 bits</td>
</tr>
<tr>
<td>SINAD</td>
<td>44.78 dB</td>
</tr>
<tr>
<td>SNR</td>
<td>64.94 dB</td>
</tr>
<tr>
<td>SFDR</td>
<td>44.82 dB</td>
</tr>
<tr>
<td>Power</td>
<td>64 µW (1.0 V Supply)</td>
</tr>
</tbody>
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Conclusion

- **Digital Temperature Transducer ASIC:**
  - Sensing, data-conversion and communication

- **28 nm FDSOI CMOS Process:**
  - Reduced parasitics, back-gate biasing, good radiation tolerance

- **System Requirements:**
  - Up to ±1 °C accuracy in [-20 °C, +20 °C] with 0.1 °C resolution

- **Demonstrator: AMBER1 IC**
  - ∑Δ Modulator: 1st order, discrete-time, correlated double sampling

- **Next Steps:**
  - Validate 1st order ∑Δ Modulator on AMBER1 IC
  - Integrate sensor core and digital circuitry

- **Outlook:**
  - Digital intensive design: exploit low-power features of 28 nm FD-SOI CMOS process
  - Further integration of components for space applications based on FD-SOI
THANK YOU