65nm Technology Development
for electronics in the LHC at CERN

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ATLAS

CMS
High Luminosity at the LHC

- TDR: OCT 2015; TDR_v2 : 2017
- Cryo, SC links, Collimators, Diagnostics, etc. starts in LS2 (2018)
- Proof of main hardware by 2016; Prototypes by 2017 (IT, CC)
- Start construction 2018 for IT, CC & other main hardware
- IT String test (integration) in 2019-20; Main Installation 2023-25
- Though but – based on LHC experience – feasible
Radiation Environment

PIONS

Charged pion spectrum, Strip barrel 1, inner

NEUTRONS

Neutron spectrum, Strip barrel 1, inner

10 MeV

10 MeV
Radiation Environment
Radiation Environment

charged particle fluence

\( R \text{ (cm)} \)

\( Z \text{ (cm)} \)

particles/cm\(^2\)

\( 1 \times 10^{14} \)

\( 1 \times 10^{15} \)

\( 1 \times 10^{16} \)

\( 1 \times 10^{17} \)
Radiation Environment

- The radiation field is mainly photons, "light" charged particles, and neutrons.
- "No" heavy ions.
- Protons and neutrons, in their energy range, can interact with silicon and produce ions by spallation. The highest LET of these ions is less than 15 MeV/cm².
- The spallation rate is such that the (protons induced) SEU cross section per bit is in the range $10^{-13}$ to $10^{-14}$ cm².
- With appropriate TRM/redundancy, the SEU cross section per bit is reduced by a factor ~100.
- Also, latchup risk is reduced.
- The main issue is ionising dose effects in the oxides.
65nm technology

Provides capability for:

- High density pixel detectors:
  50umx50um with internal buffer and data processing per pixel

- High speed links:
  The trigger rates (that extracts data out of the detector) may increase by a factor 10, plus more detector channels
Technology roadmap in HEP

- Radiation hard processes
- Hardness By Design (HBD) in commercial-grade processes

- Production for LHC: 0.25um CMOS
- Upgrades: 130nm CMOS
- (some) tracker upgrades: 65nm CMOS

- ca. 1998-2000
- ca. 2006
- ca. 2011

- TID up to 10Mrad
- TID: 100Mrad
- TID: 400Mrad

- Main transistor
  - $V_{th}$, $g_m$, ...
  - Leakage in parasitics
- Leakage in parasitics RINCE
- Leakage in parasitics RISC
130nm technology

- Radiation tests

Enclosed Layout Transistor exhibits no degradation

Standard layout exhibits parasitic leakage with a “shape”
The leakage current is the sum of different mechanisms involving:

- the creation/trapping of charge (by radiation)
- its passivation/de-trapping (by thermal excitation)

These phenomena are Dose Rate and Temperature dependent!

Is there still the need for ELTs and guard rings?

130nm technology

- Oxide and interface charges
130nm technology

- Radiation tests

"Radiation Induced Narrow Channel" effect

65 nm technology

- Radiation tests

“No ”bump” effect

Vt shift limited to 20mV

Std NMOS device
65 nm technology

- Radiation tests

Vt shift increases

The PMOS drive capability degrades
65 nm technology

Radial damage is severe in short and narrow channel transistors, where it depends on the bias and temperature applied both during and after irradiation.

PMOS W array  PMOS L array  NMOS L array  NMOS W array

Bias: |Vgs|=|Vds|=1.2V

Radial-Induced Narrow Channel Effect (RINCE)
Radial-Induced Short Channel Effect (RISCE)

1 Mrads  1 Mrads

Std PMOS device  Std NMOS device
65 nm technology

Transistors’ size: W=1um, L=60nm
Irradiation conditions:
T = 25C
Bias: |Vgs|=|Vds|=1.2V
65 nm technology

- Bias during irradiation is bad!

Annealing at high T is neutral or good (for the most damaged devices)!

Std NMOS device

Transistors' size: W=0.6μm, L=60nm
Irradiation conditions:

- Bias:
  - "Vgs" => |Vgs| = 1.2V, Vds=0V
  - "Diode" => |Vgs| = |Vds| >1.2V
  - "Gnd" => |Vgs|=Vds=0V

Sub-zero T during irradiation is good
65 nm technology

Bias during irradiation is mildly influential

Thermal energy during irradiation is bad!

Annealing at high T is very bad if performed under bias!!

Std PMOS device

Transistors’ size: W=0.6um, L=60nm
Irradiation conditions:
* Bias:
  "Vgs" => |Vgs| = 1.2V, Vds=0V
  "Diode" => |Vgs| = |Vds|=1.2V
  "Gnd" => |Vgs| = Vds=0V
Circuits in 65nm technology

Digital Libraries

Reg nmos : 1u/60n: IDS=f(VGS) for VDS=1p20V

Drain Current (A)

Gate Source Voltage (V)

Pre Irrad-Meas
500 Mrad-Meas
Pre Irrad-Sim
500 Mrad-Sim

Measured versus Model
Pre-Rad and at 500 Mrads

9 libraries:
Different $V_T$ flavours, transistor size and shape

DRAD Chip: evaluation of variants of digital libraries

Models build at 200 and 500 Mrads
Circuits in 65nm technology

Bandgap reference

Bandgap with Diodes

Bandgap with DTNMOS

Date

June 14, 2016

AMICSA 2016
Circuits in 65nm technology

I/O cells

SLVS Receiver, 640Mb/s

SLVS Driver cell, 1.2GB/s
Circuits in 65nm technology

RAM Generator

Clock synchronous, pseudo dual-port memory

Write/Read operation @ same clock cycle

Operating speed: 80 MHz @ 1.2 V

Memory Compiler specifications:

- Minimum size: 128 words of 8 bit
- Max size: 1k words of 256 bits
- Generates: complete OA database, timing library, datasheets
- RadTol design techniques for TID and SET robustness

(Development by IMEC)
Circuits in 65nm technology

Other cells in preparation

PLL, DLL

Front-Ends (Amplifiers, filters, discriminators)

ADC : 12 bits dual ramp (monitoring)

DACs : 10 bits (biasing)

LDO
65 nm technology SEU cross section

![Graph showing cross-section vs LET for different digital blocks.](image)

The cross-section per bit of the SRAM and shift-register blocks are presented in Fig. 19. The shift-register, therefore, has a lower cross-section, though not strictly proportional to the area.

The I/O pad current has a negligible change in the explored TID range.

The ring oscillator frequency and current decrease constantly with TID, as visible in Fig. 20. The shift-register static current changes very little with respect to the SRAM, increasing within a factor 3.3 for both the SRAM and the shift-register, which have similar results. In a typical application, the reduction in power supply can give great savings in power and the worst case, as shown in Fig. 21, is about 40% in power and 70% in cross-section in the shift-register. The SRAM cell has an area about 13 times larger than the shift-register, which explains the higher cross-section.

The dependence on the power supply is slightly bigger compared to data acquired in a 90 nm technology (different foundry) [2], previously tested in the same facility [3]. The shift-register showed an evidence of particle hits on the clock-tree, which caused throughput to reduce from a high of 19.4 MHz down to 6.5 MHz (a factor 3.0) and the shift-register static current to increase by a factor 300 for a 1BU upset (for 1.2 V @0.9V)

The SRAM static current increases by a factor 3, which probably translates to a proportional speed reduction. Once again the annealing step restores the supply currents to their pre-rad value.

This behaviour is most likely dependent on the dose rate, since there is an evidence of a partial annealing effect taking place at room temperature with a short time constant (about 1.5 hours). The annealing effect is more evident in the shift-register, which can bring back the supply currents to their pre-rad value within a factor 0.7, whereas in the SRAM the recovery is more gradual. The SRAM is the block that suffers most from TID, probably due to the use of ultra-narrow transistor (W=80 nm) in the SRAM memory cell.

The dependence on the power supply is slightly bigger compared to data acquired in a 90 nm technology (different foundry) [2]. Contrary to this, the corresponding dynamic current has a small decrease of about 1E-7 – 1E-9 in the explored TID range.

The SRAM static current, which is more sensitive to TID, increases by a factor 300, which probably translates to a proportional speed reduction. Once again the annealing step restores the supply currents to their pre-rad value.

This behaviour is most likely dependent on the dose rate, since there is an evidence of a partial annealing effect taking place at room temperature with a short time constant (about 1.5 hours). The annealing effect is more evident in the shift-register, which can bring back the supply currents to their pre-rad value within a factor 0.7, whereas in the SRAM the recovery is more gradual. The SRAM is the block that suffers most from TID, probably due to the use of ultra-narrow transistor (W=80 nm) in the SRAM memory cell.
Electronics in experiments

Next generation of silicon pixel detectors for phase-2 upgrade of ATLAS and CMS at HL-LHC sets unprecedented design requirements

- Small pixels (50x50 μm² / 25x100 μm²)
- Large chips (~2x2 cm², ~109M transistors)
- Hit rate up to more than 3 GHz/cm² (high pileup ~200)
- Radiation tolerance: 1 Grad TID, 2x10¹⁶ neq/cm²
- Trigger rate up to 1 MHz, ~12.5 μs trigger latency
Electronics in experiments

- **Data rates:**
  - 5 to 10 Gb/s for up links
  - 2.5 Gb/s for down links

- **Environment**
  - Temperature: -35 to +60 °C
  - Total Dose: 100 Mrad qualification (200 Mrad LpGBT chipset)
  - Total Fluence: $2 \times 10^{15}$ n/cm$^2$ and $1 \times 10^{15}$ hadrons/cm$^2$

LpGBT

Bidirectional High Speed Serial Link
Circuits in 65nm technology

**Goals of RD53 (65 nm technology)**
- Radiation qualification and characterization in 65 nm → guidelines for radiation hardness
- Development of tools and methodology to efficiently design large complex mixed signal chips
- Design and characterization of circuits and building blocks needed for pixel chips → design of shared rad-hard IP library
- Design and characterization of full scale demonstrator pixel chip

**RD53 Working Groups (WGs)**

<table>
<thead>
<tr>
<th>Radiation WG</th>
<th>Analog WG</th>
<th>IP WG</th>
<th>Simulation WG</th>
<th>Top level and chip integration WG</th>
<th>I/O WG</th>
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20 participating institutes: Bari, Bonn, CERN, CPPM, FNAL, LBNL, LPNHE, New Mexico, Milano, Padova, Pavia-Bergamo, Pisa, Perugia, Prague IP-FNSPE-CTU, PSI, RAL, Torino, UC Santa Cruz, Sevilla
Circuits in 65nm technology

Complex Design Manufacturing Rules
DRC deck file line count:
- 250nm: 5,300 lines
- 130nm: 13,500 lines
- 90nm: 38,400 lines
- 65nm: 89,300 lines
Conclusion

• A large effort is going on at CERN and with the associated institutes to qualify a 65nm technology for the experiments upgrades

• Targets are highly segmented detectors and high bandwidth

• Dependencies found at “high” total dose, with complex annealing and dose rate relationships

• IP blocks under developments, through structured collaborations