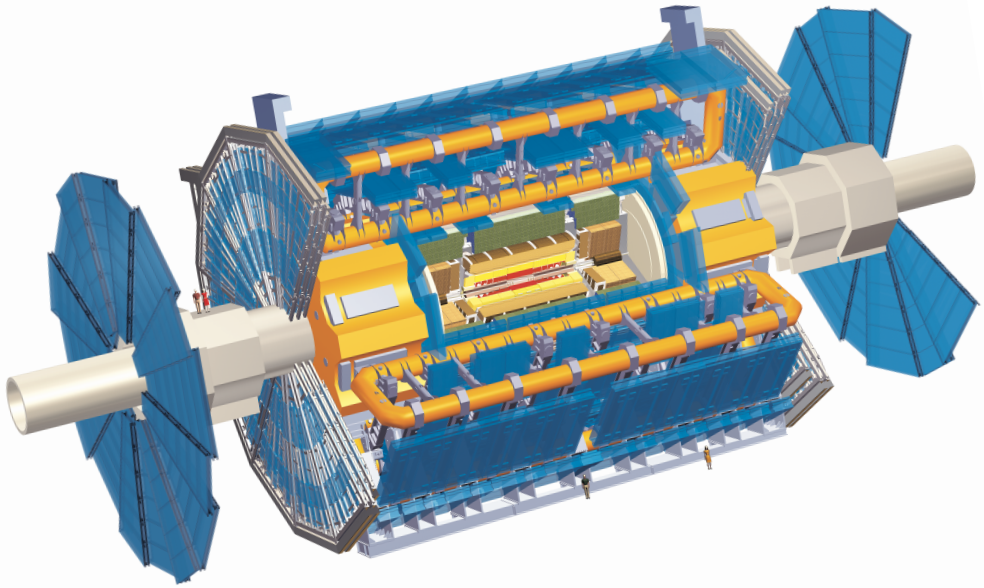
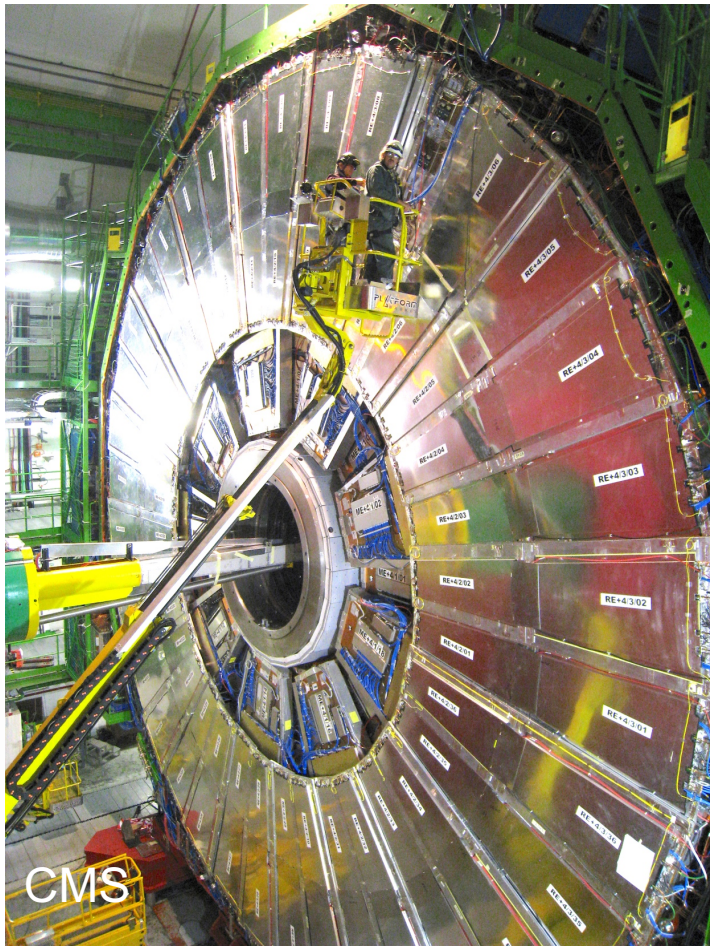
# 65nm Technology Development
## for electronics in the LHC at CERN

Francis ANGHINOLFI CERN EP

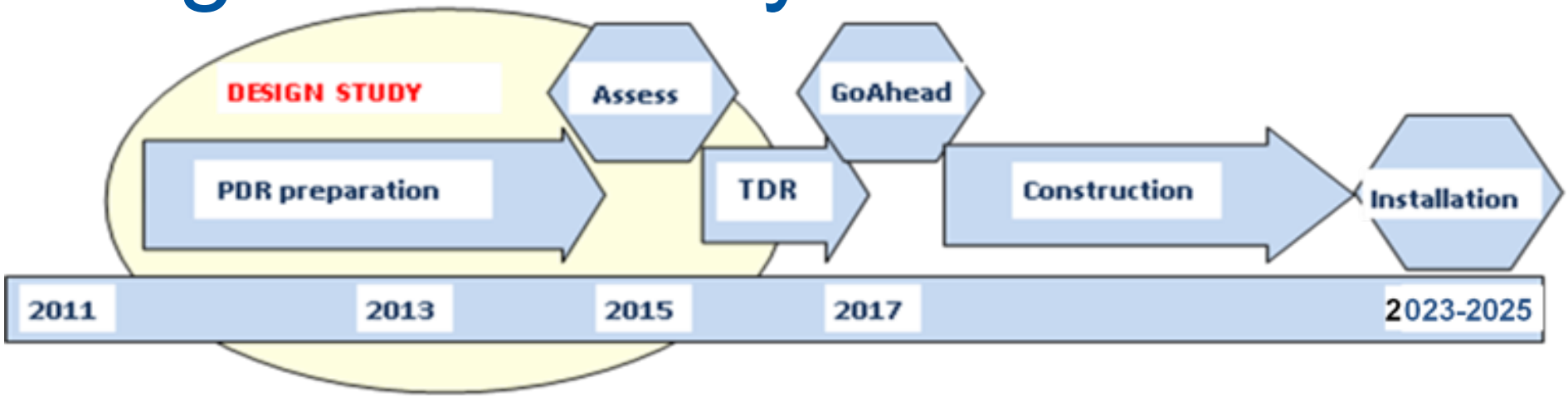


ATLAS



CMS

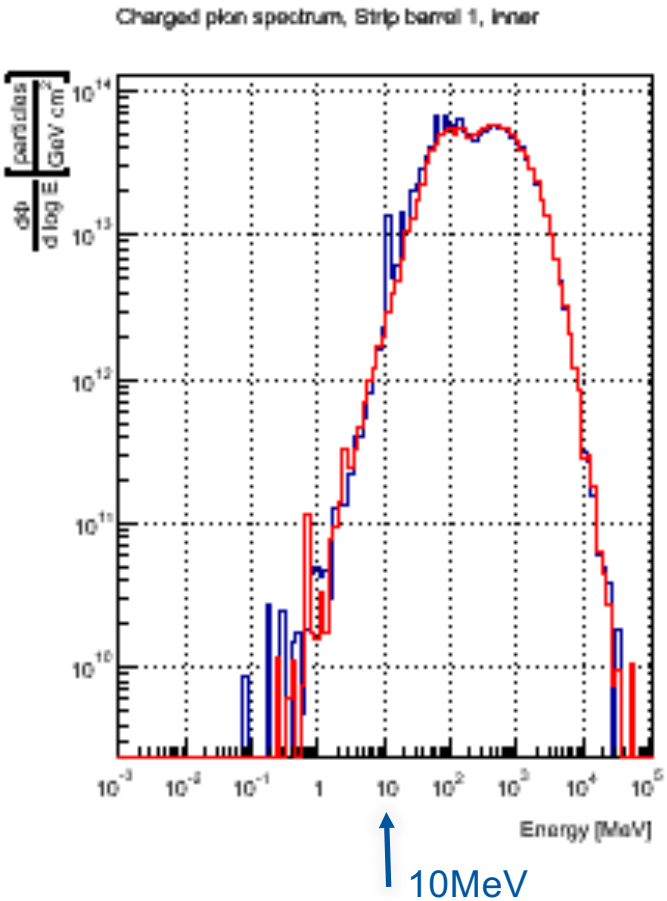
# High Luminosity at the LHC



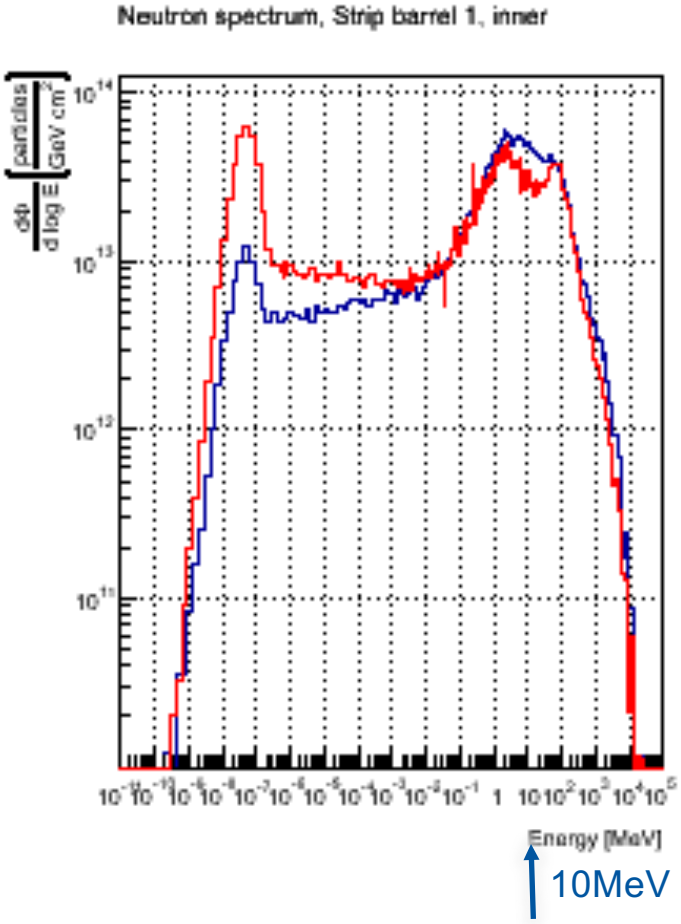

- PDR: Oct 2014 ; Ext. Cost & Schedule Review in Jan-Feb 2015;
- TDR: OCT 2015; TDR_v2 : 2017
- Cryo, SC links, Collimators, Diagnostics, etc. starts in LS2 (2018)
- Proof of main hardware by 2016; Prototypes by 2017 (IT, CC)
- Start construction 2018 for IT, CC & other main hardware
- IT String test (integration) in 2019-20; Main Installation 2023-25
- Though but – based on LHC experience – feasible

# Radiation Environment

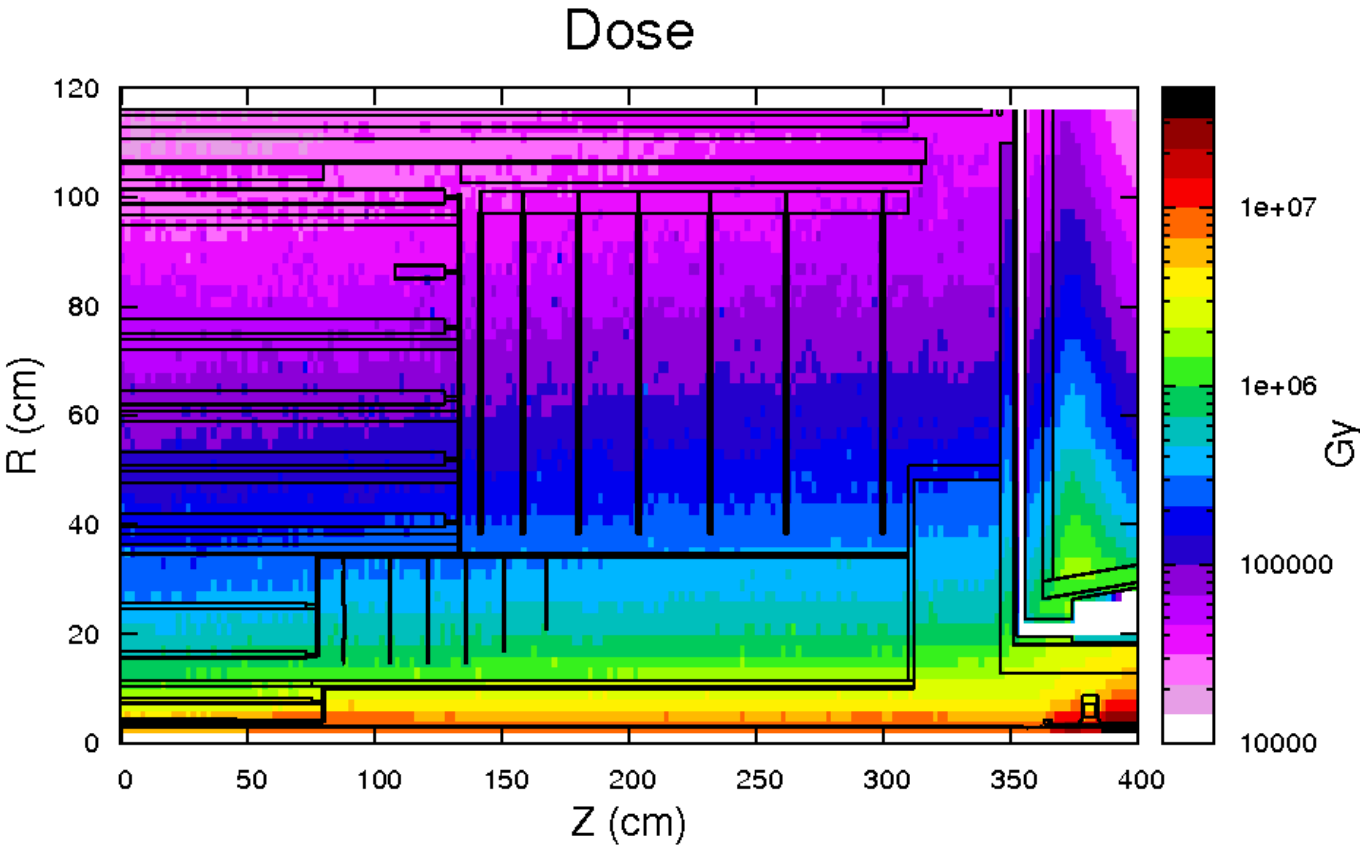
PIONS



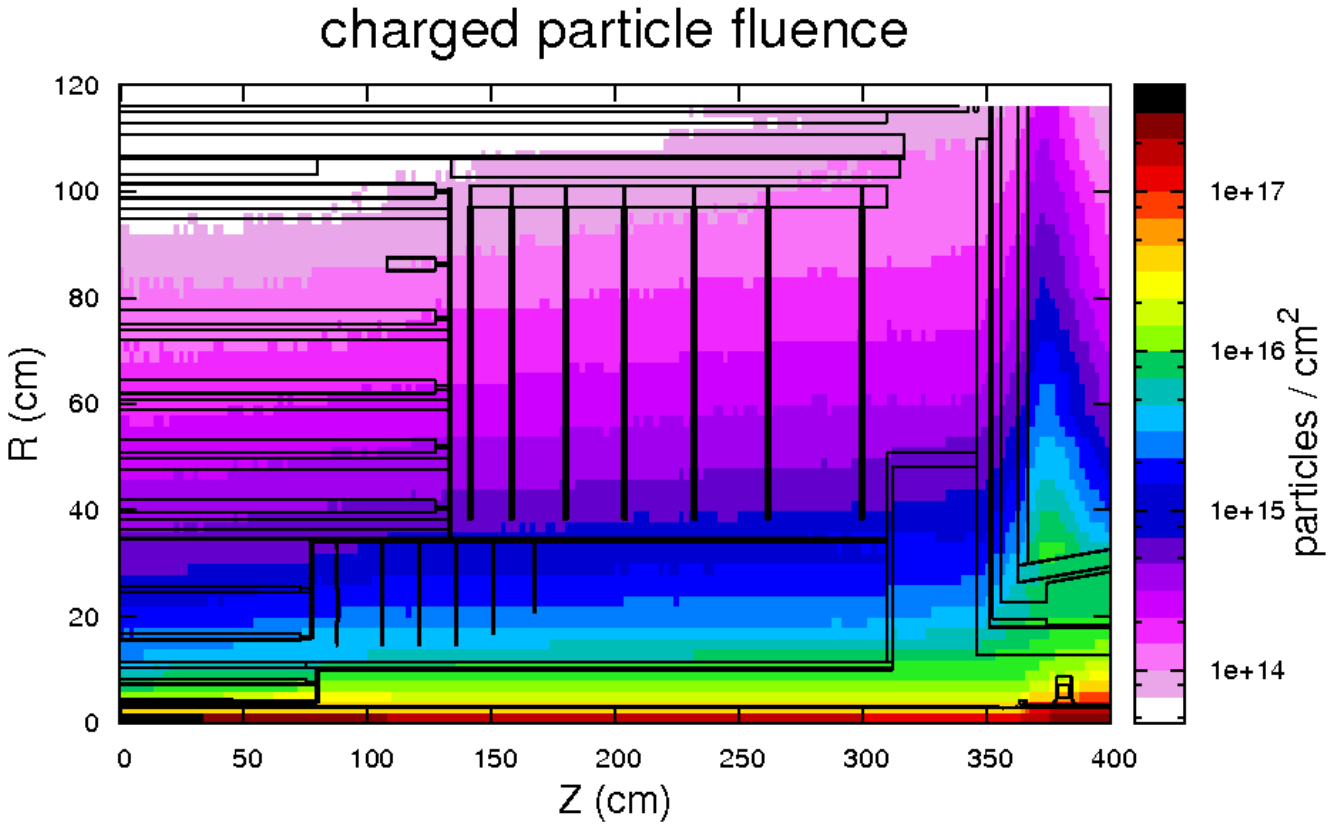

NEUTRONS



# Radiation Environment



# Radiation Environment



# Radiation Environment

- The radiation field in mainly photons, ”light” charged particles, and neutrons
- “No” heavy ions
- Protons and neutrons, in their energy range, can interact with Silicium and produce ions by spallation. The highest LET of these ions is less than 15 MeV/cm2
- The spallation rate is such that the (protons induced) SEU cross section per bit is in the range $10^{-13}$ to $10^{-14}$ $cm^{-2}$
- With appropriate TRM/redundancy the SEU cross section per bit is reduced by a factor ~100
- Also latchup risk is reduced
- The main issue is ionising dose effects in the oxides

# 65nm technology

Provides capability for :

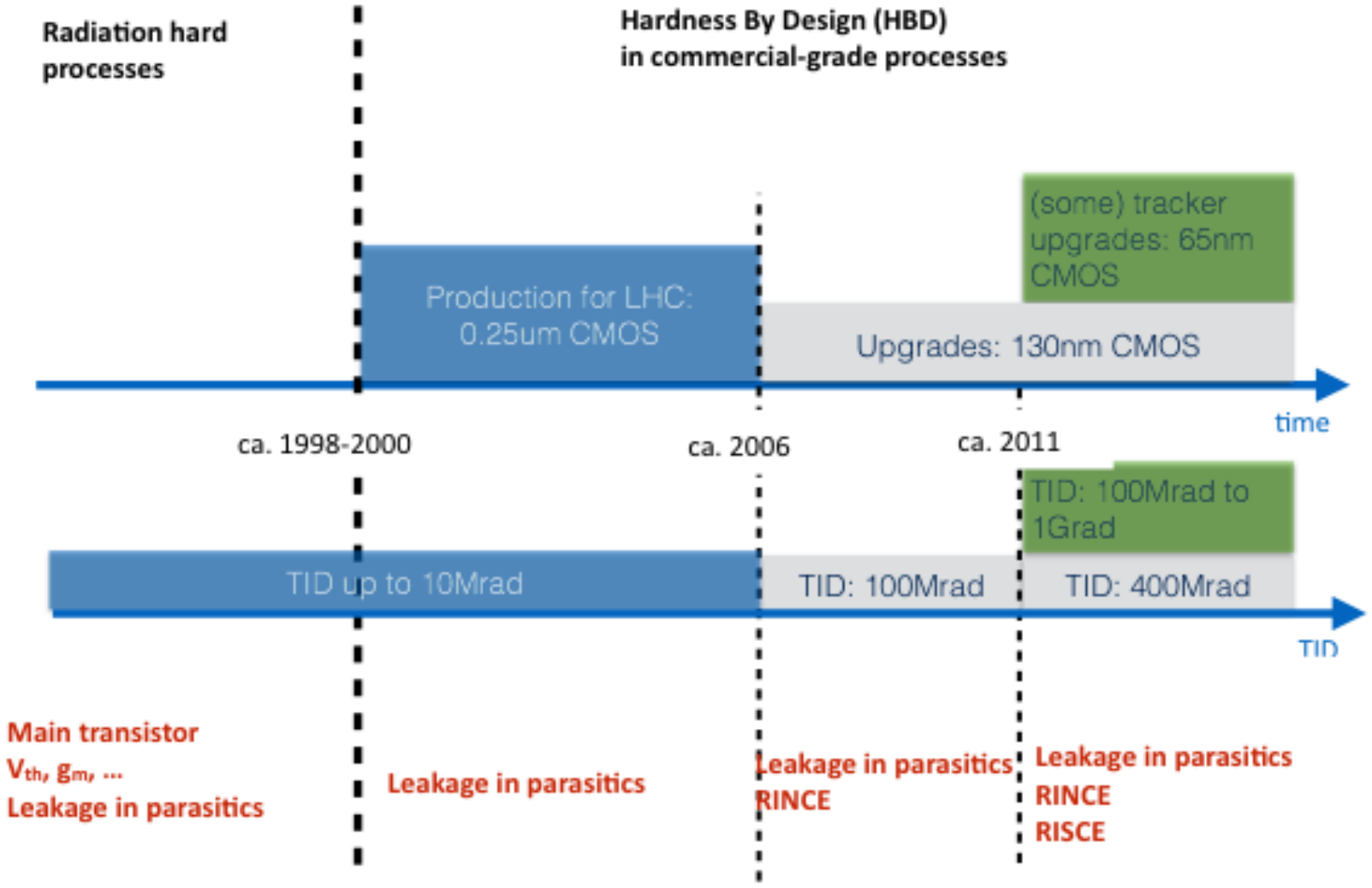
- High density pixel detectors :

  50umx50um with internal buffer and data processing per pixel

- High speed links :

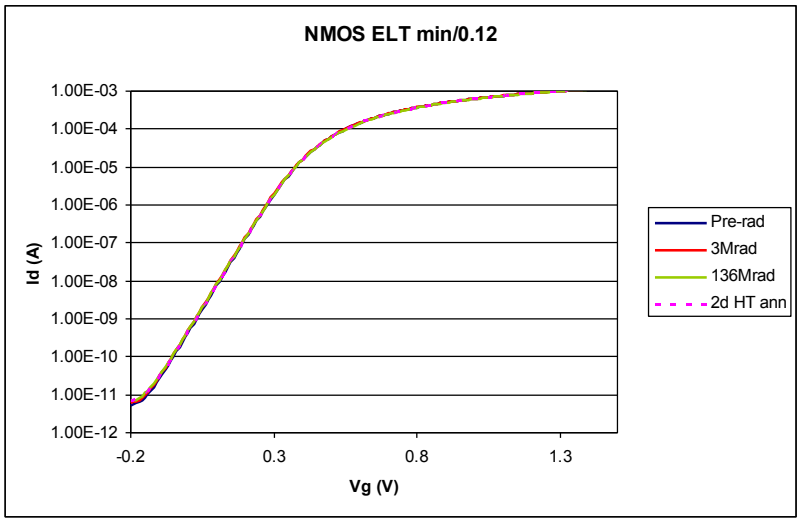
  The trigger rates (that extracts data out of the detector) may increase by a factor 10, plus more detector channels

# Technology roadmap in HEP

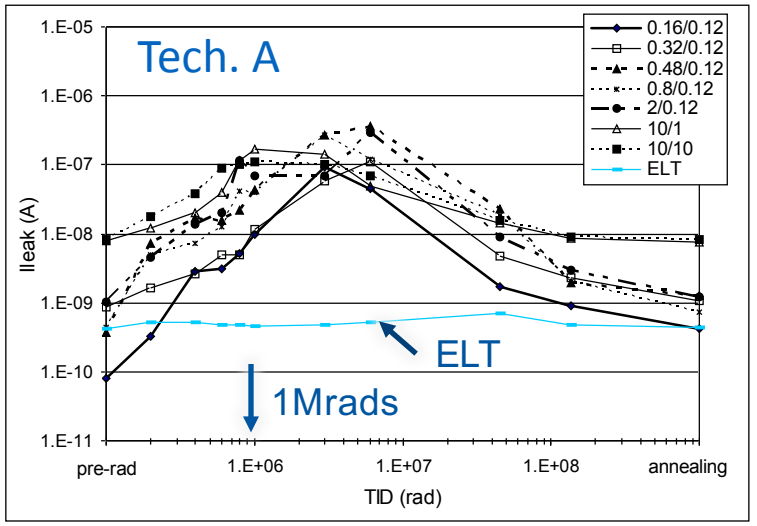


# 130nm technology

- Radiation tests



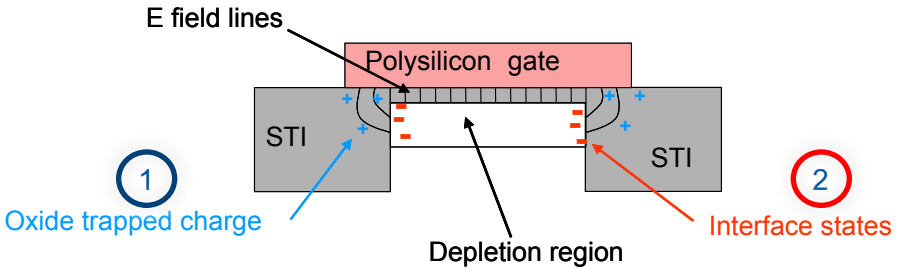

Enclosed Layout Transistor exhibits no degradation

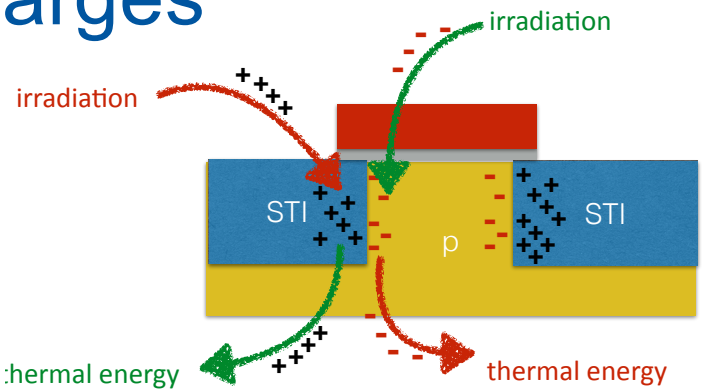


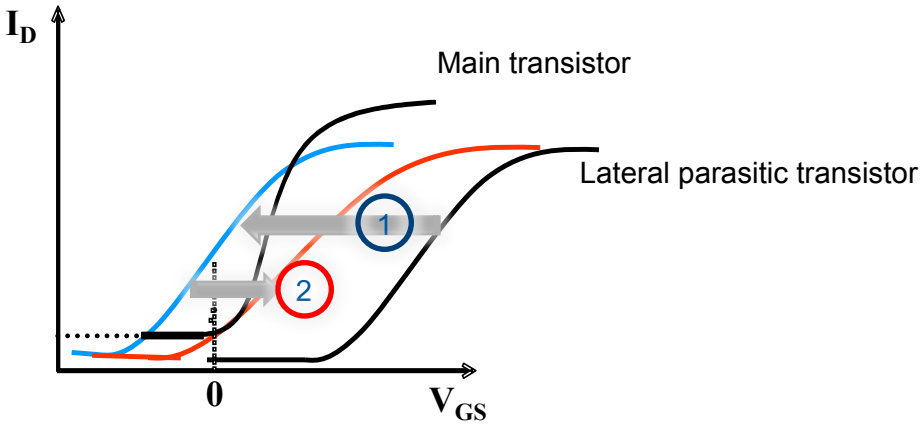

Standard layout exhibits parasitic leakage with a “shape”

# 130nm technology

- Oxide and interface charges



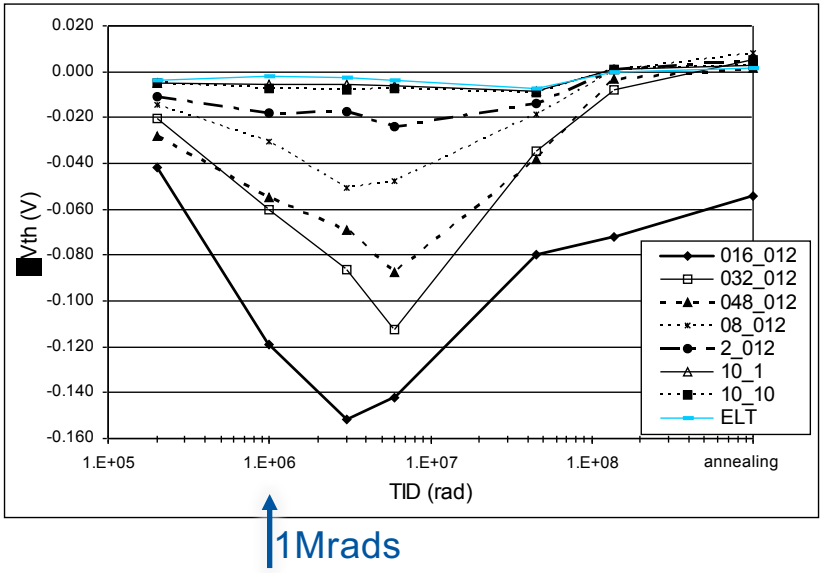



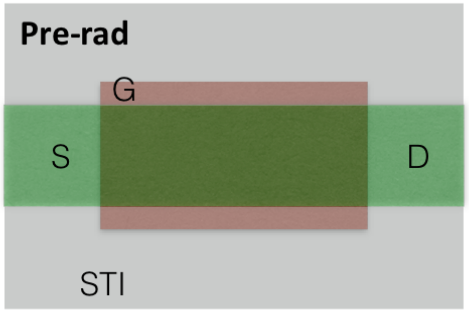
# 130nm technology

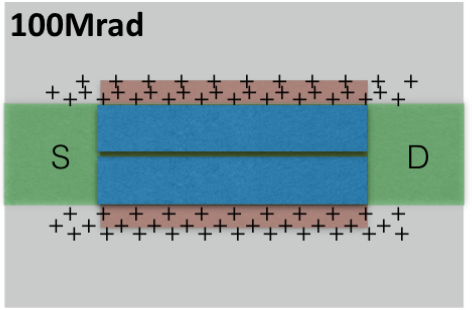
- Radiation tests

NMOS




W=min size



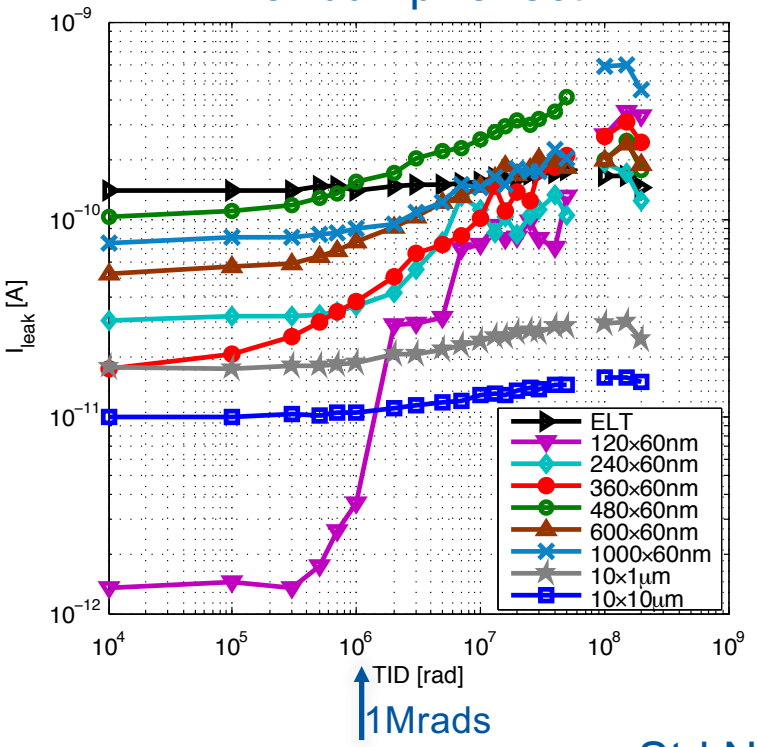

"Radiation Induced Narrow Channel" effect

F.Faccio, G.Cervelli, "RadiaOon-induced edge effects in deep submicron CMOS transistors", IEEE Trans. Nucl. Science, Vol.52, No.6, December 2005, pp.2413-2420

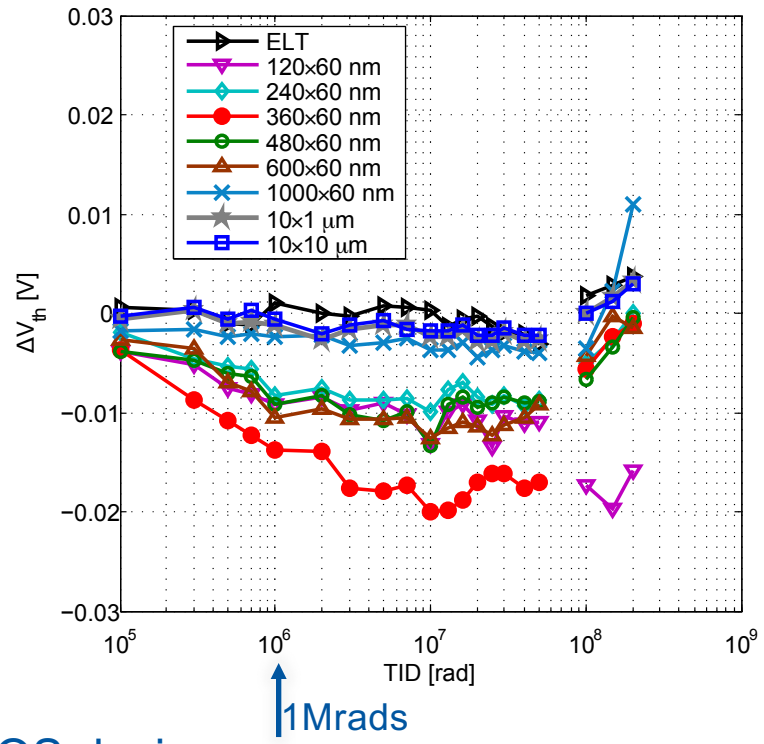
# 65 nm technology

- Radiation tests

"No "bump" effect




Vt shift limited to 20mV

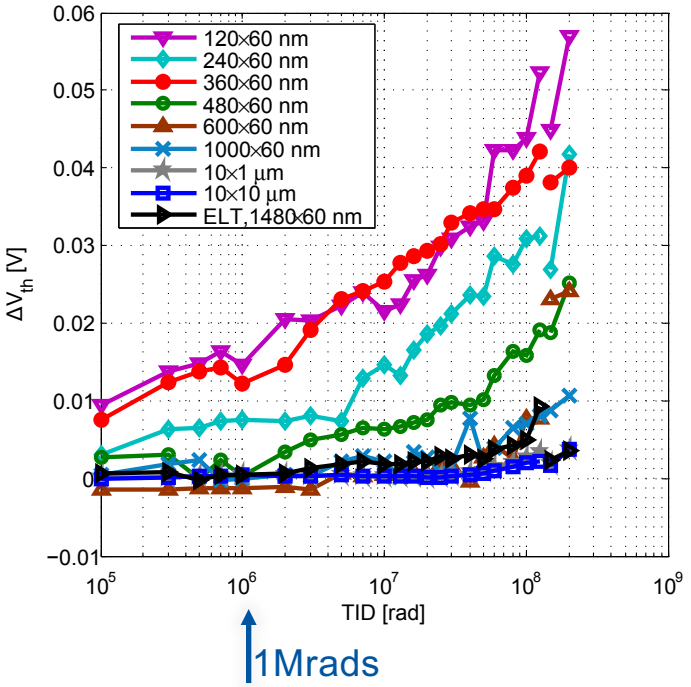



Std NMOS device

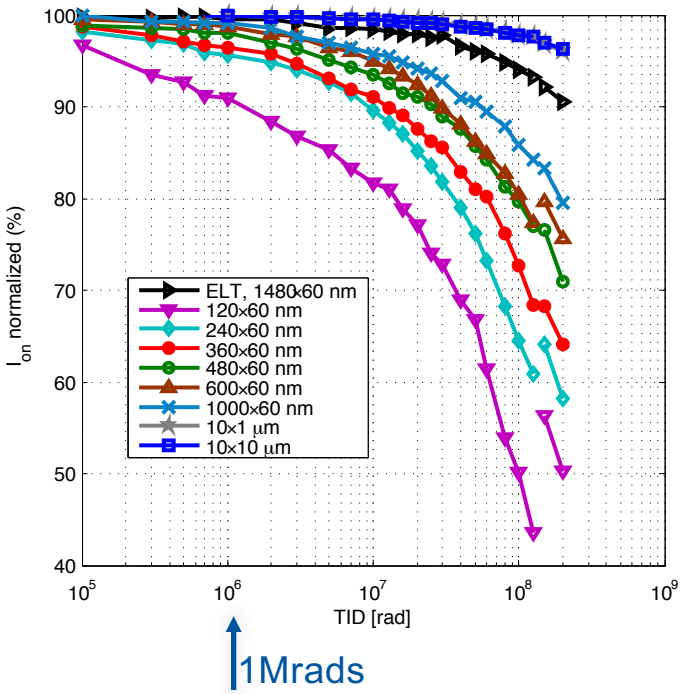
# 65 nm technology

- Radiation tests

Vt shift increases



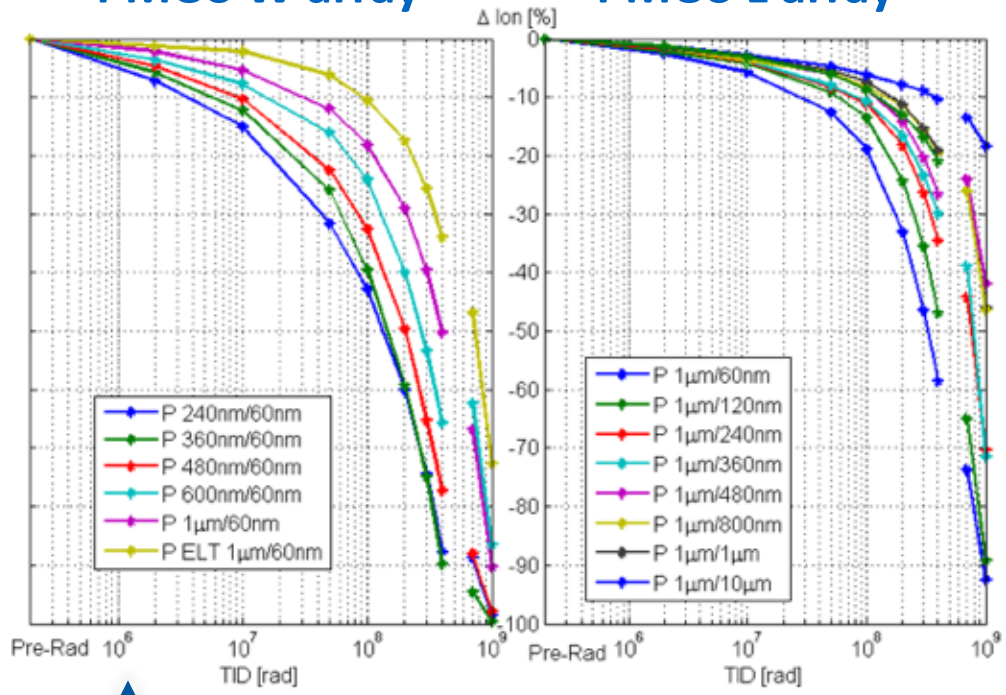

The PMOS drive capability degrades




Std PMOS device

# 65 nm technology

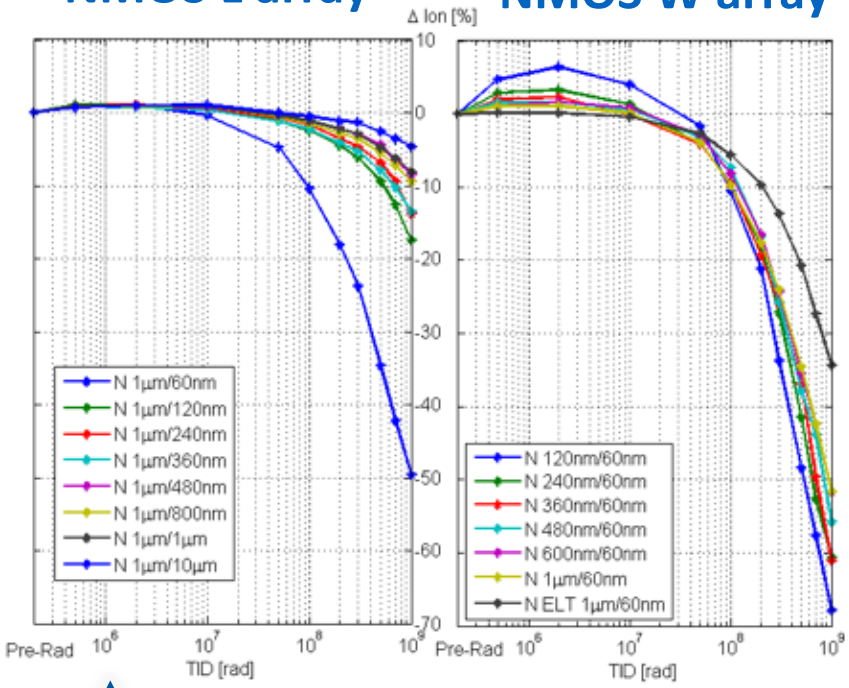
**PMOS W array** **PMOS L array**




1Mrads

Std PMOS device

**NMOS L array** **NMOS W array**

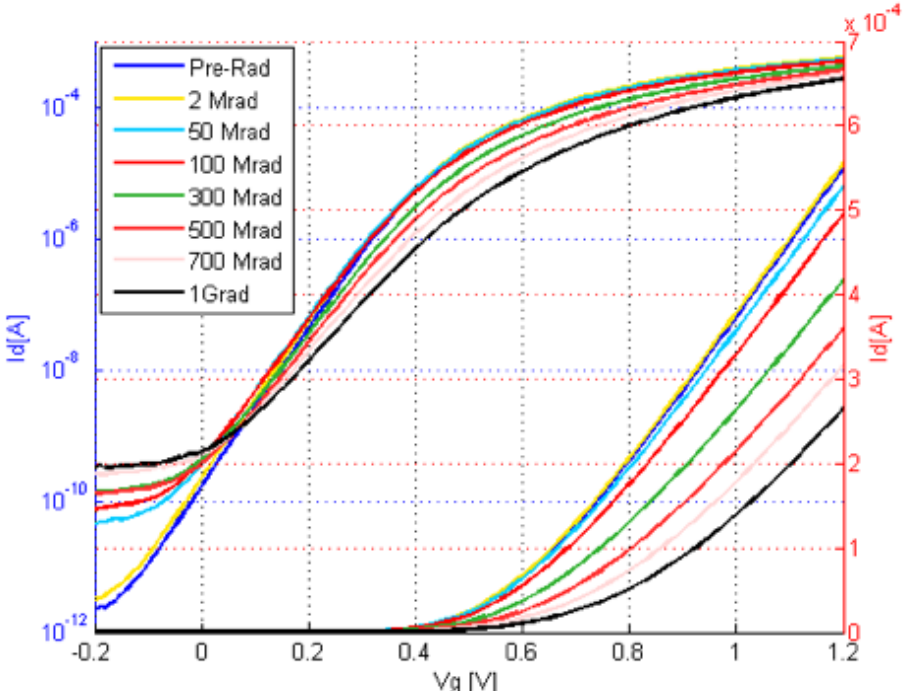



1Mrads

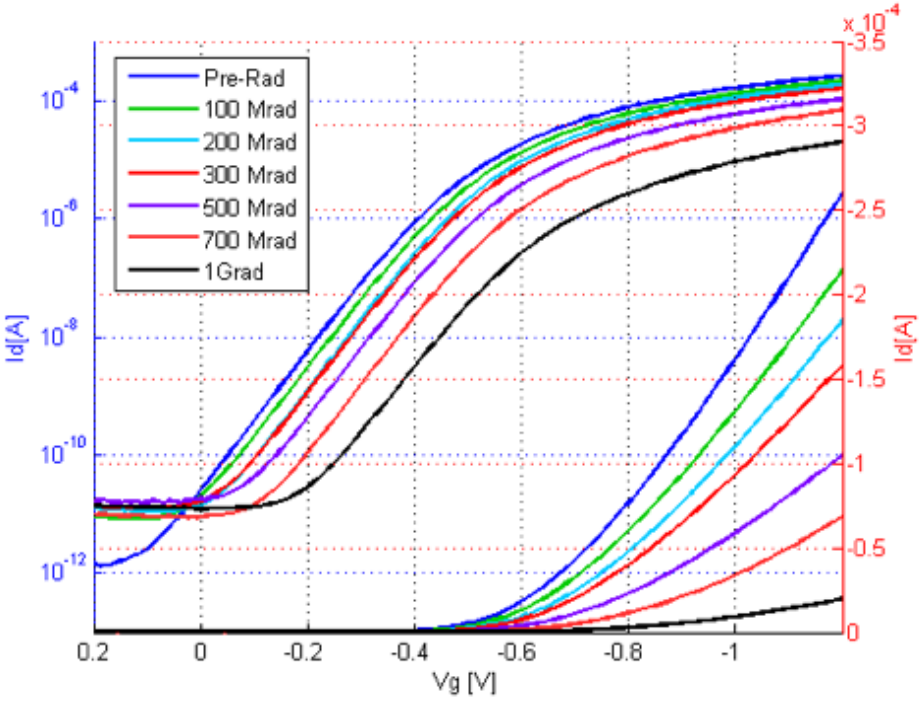
Std NMOS device

# 65 nm technology

**NMOS**



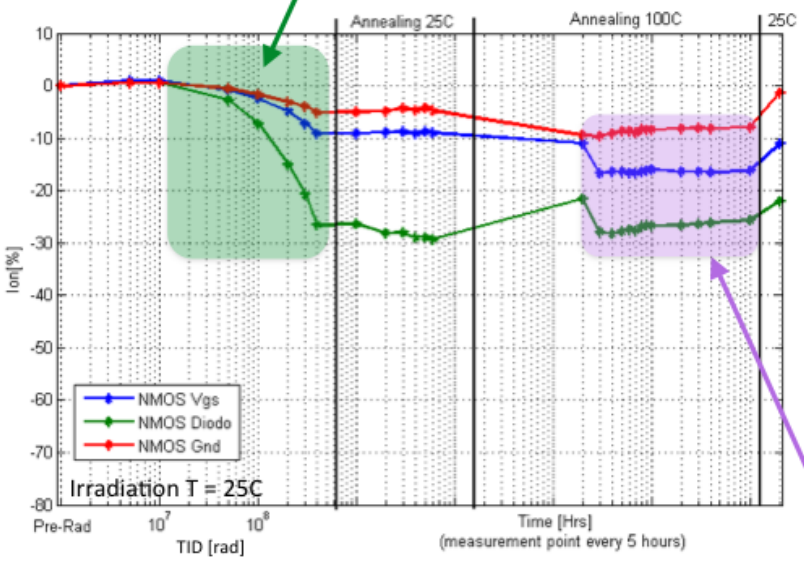

**PMOS**



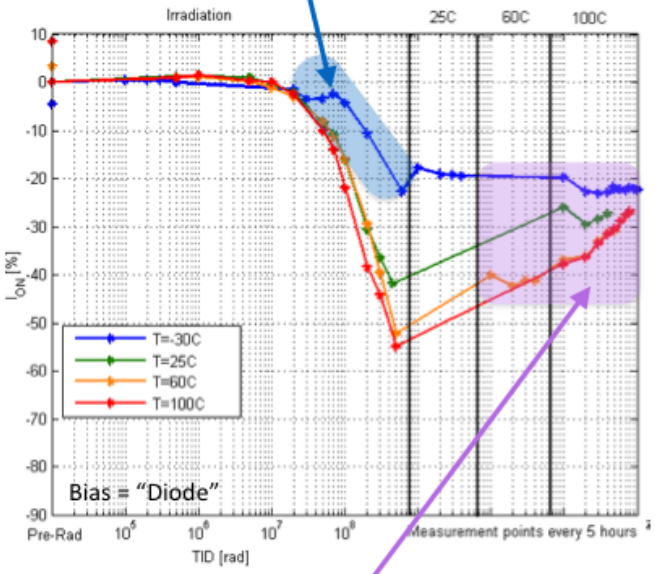

Transistors' size: W=1um, L=60nm
Irradiation conditions:
T = 25C
Bias: |Vgs|=|Vds|=1.2V

# 65 nm technology

- Bias during irradiation is bad!




Sub-zero T during irradiation is good



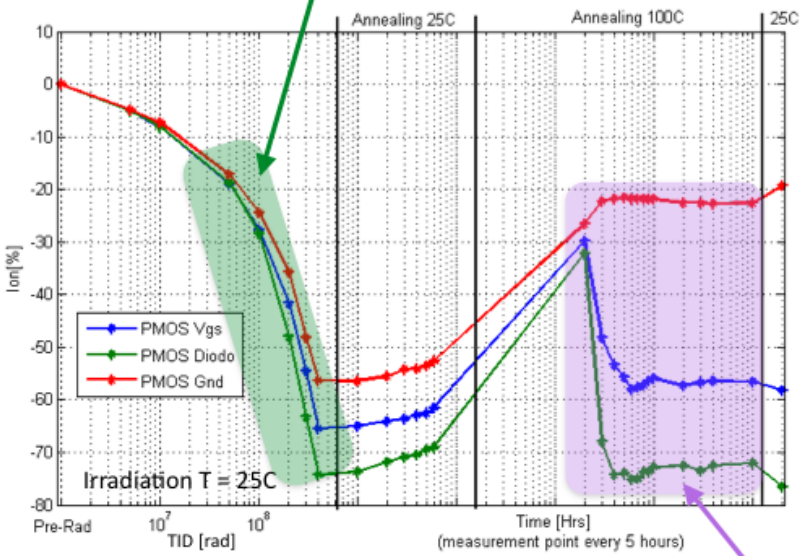

Annealing at high T is neutral or good
(for the most damaged devices)!

Transistors' size: W=0.6um, L=60nm
Irradiation conditions:
* Bias:
"Vgs" => |Vgs|= 1.2V, Vds=0V
"Diode" => |Vgs|=|Vds|=1.2V
"Gnd" =>|Vgs|=Vds=0V

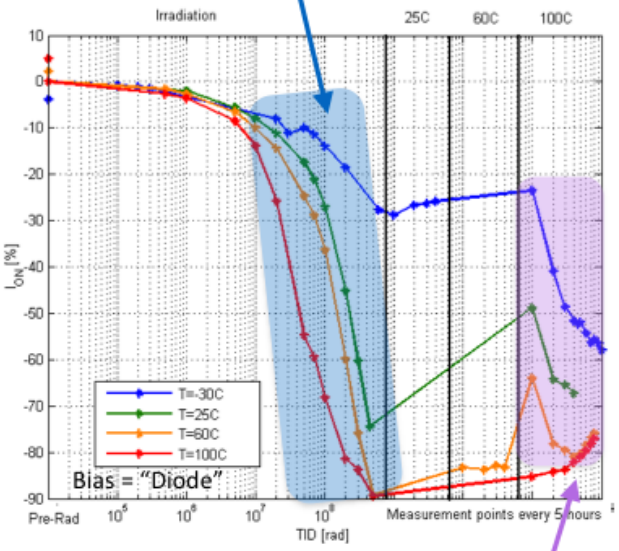
Std NMOS device

# 65 nm technology

- Bias during irradiation is mildly influential




Thermal energy during irradiation is bad!



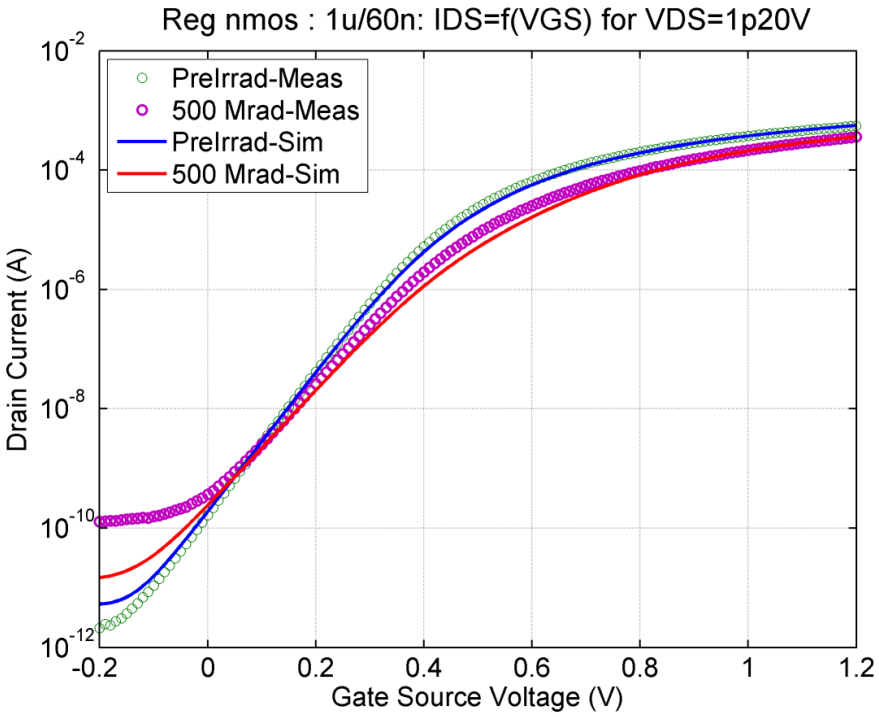

Transistors' size: W=0.6um, L=60nm
Irradiation conditions:
* Bias:
"Vgs" => |Vgs|= 1.2V, Vds=0V
"Diode" => |Vgs|=|Vds|=1.2V
"Gnd" =>|Vgs|=Vds=0V

Annealing at high T is very bad if performed under bias!!

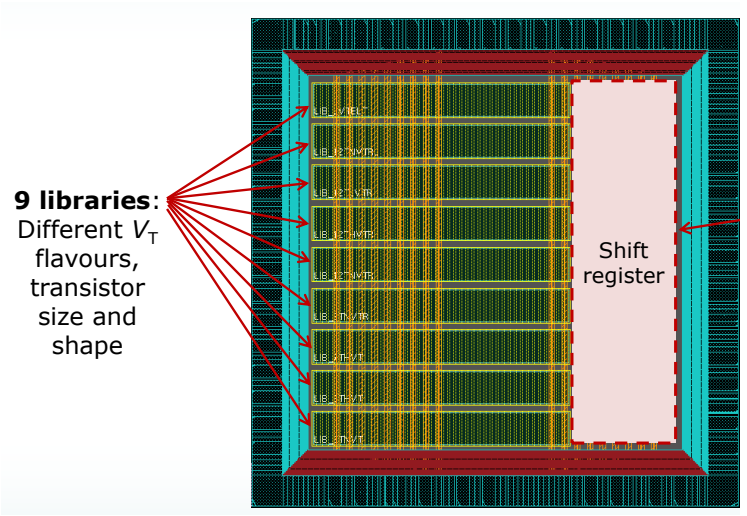
Std PMOS device

# Circuits in 65nm technology

## Digital Libraries




Measured versus Model Pre-Rad and at 500Mrads

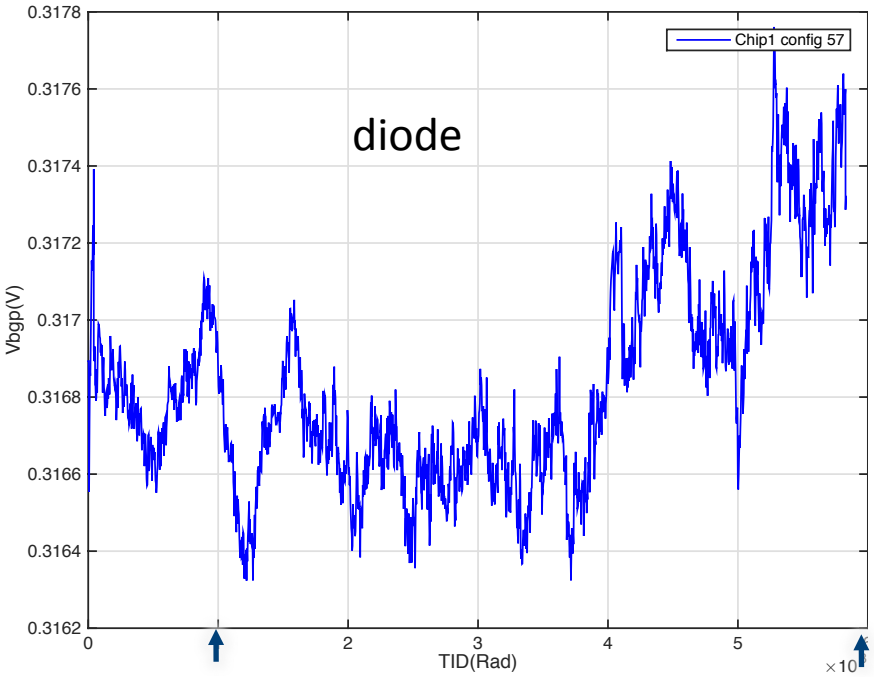



DRAD Chip : evaluation of variants of digital libraries

Models build at 200 and 500 Mrads

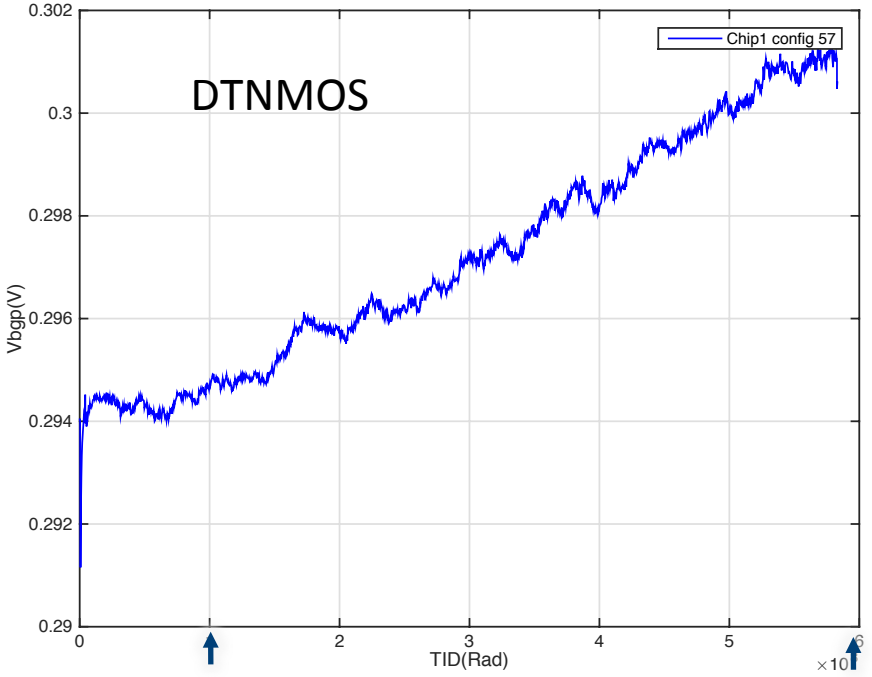
# Circuits in 65nm technology

## Bandgap reference




1Mrads

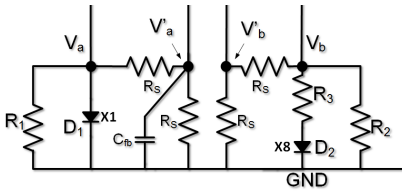
600Mrads



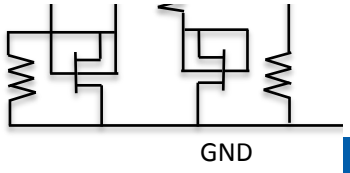

1Mrads

600Mrads

## Bandgap with Diodes

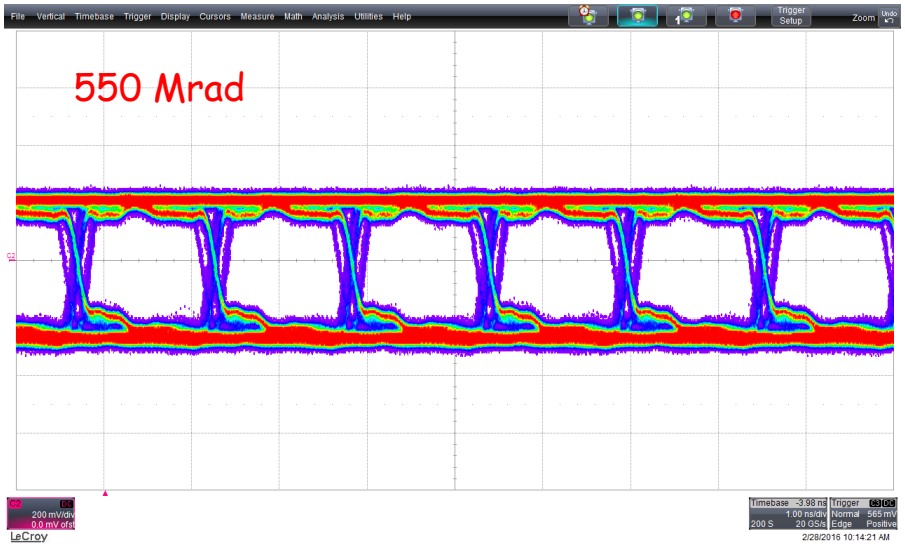



## Bandgap with DTNMOS

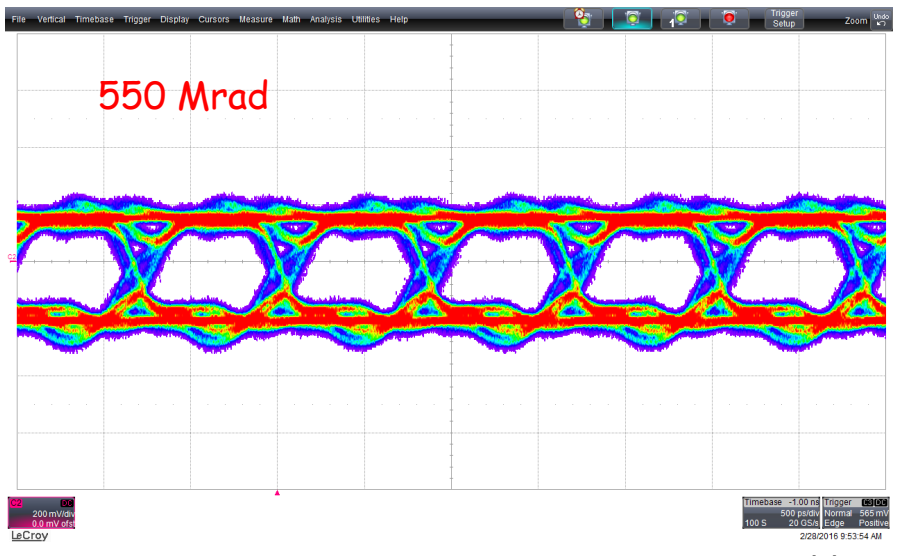


# Circuits in 65nm technology

## I/O cells




SLVS Receiver, 640Mb/s




SLVS Driver cell, 1.2GB/s

# Circuits in 65nm technology

## RAM Generator

Clock synchronous, pseudo dual-port memory

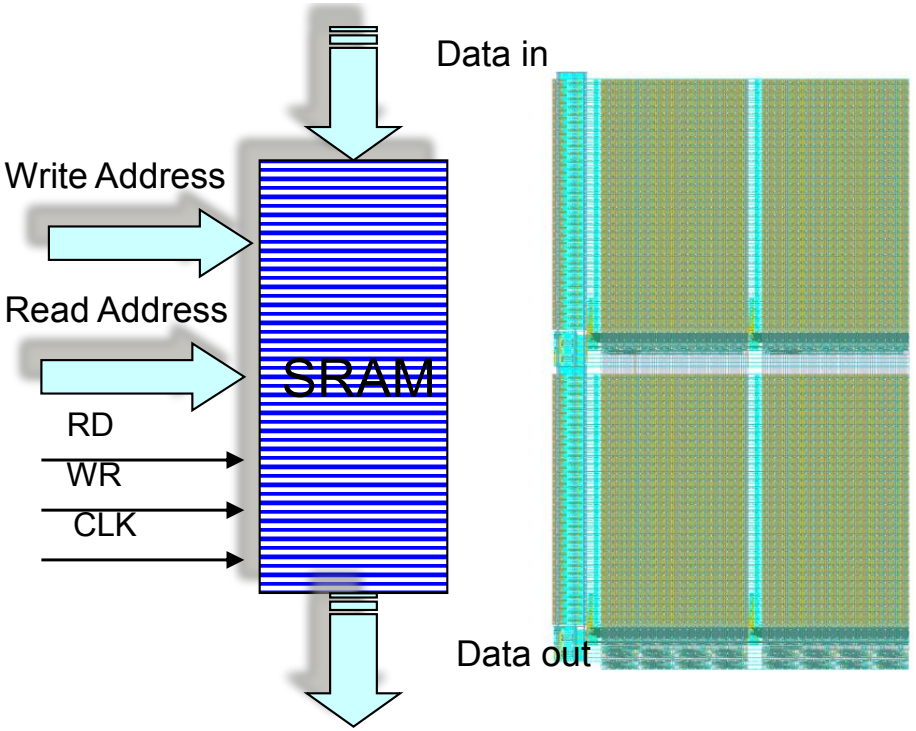
Write/Read operation @ same clock cycle

Operating speed: 80 MHz @ 1.2 V

Memory Compiler specifications:

- Minimum size: 128 words of 8 bit
- Max size: 1k words of 256 bits
- Generates: complete OA database, timing library, datasheets

RadTol design techniques for TID and SET robustness




(Development by IMEC)

# Circuits in 65nm technology

Other cells in preparation

PLL, DLL

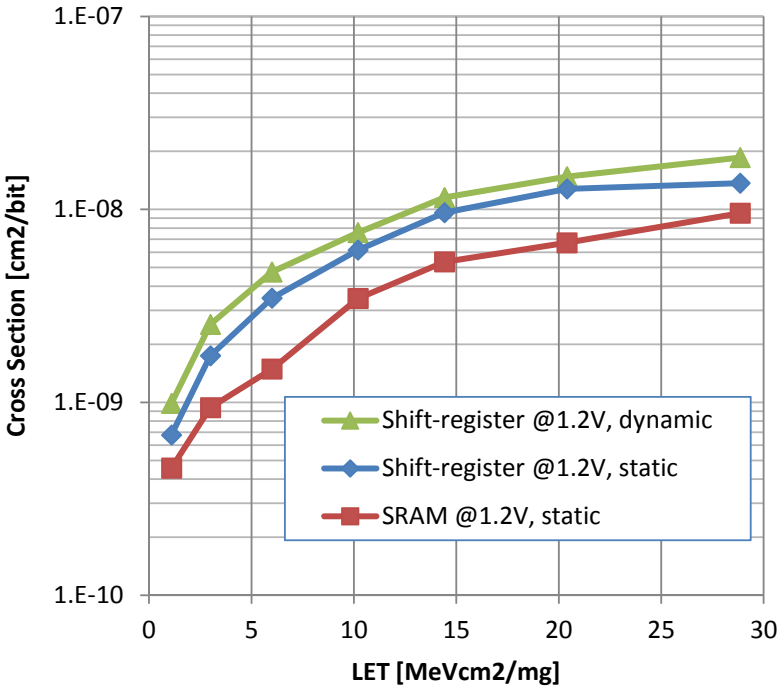
Front-Ends (Amplifiers, filters, discriminators)

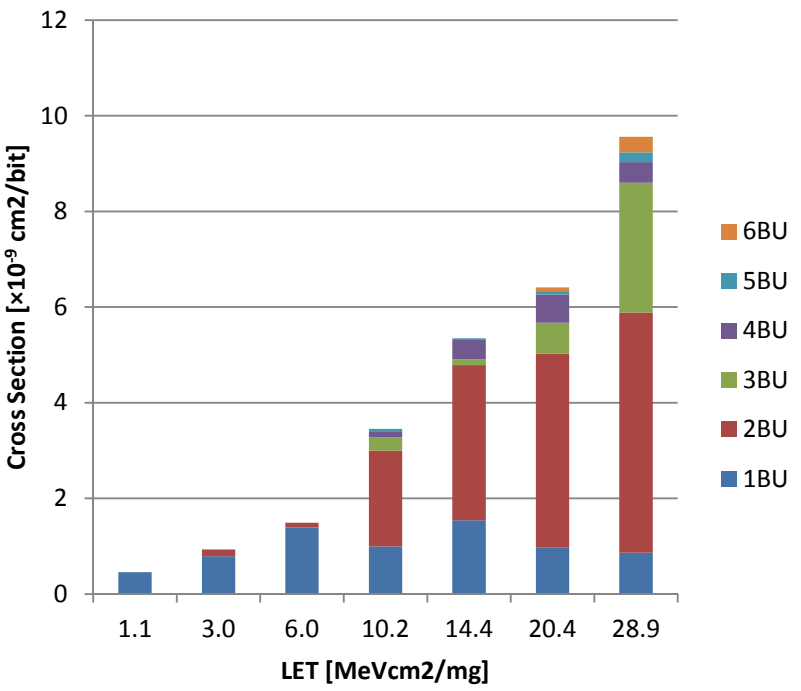
ADC : 12 bits dual ramp (monitoring)

DACs : 10 bits (biasing)

LDO

# 65 nm technology SEU cross section



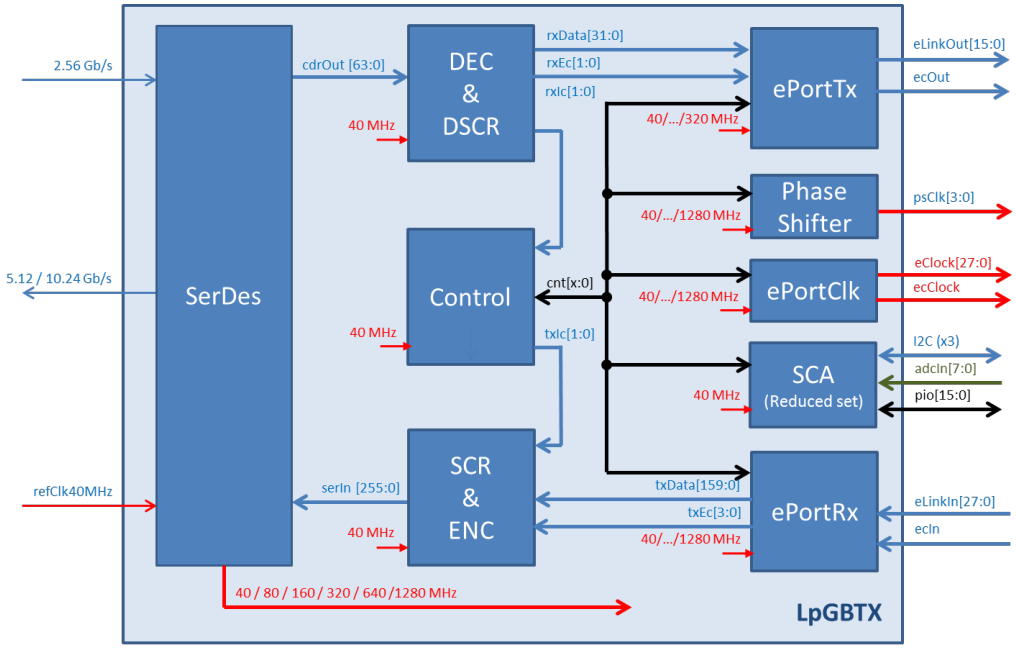



# Electronics in experiments


High density Pixel

Next generation of silicon pixel detectors for phase-2 upgrade of ATLAS and CMS at HL-LHC sets unprecedented design requirements
– Small pixels (50x50 μm2 / 25x100 μm2)
– Large chips (~2x2 cm2, ~109M transistors)
– Hit rate up to more than 3 GHz/cm2 (high pileup ~200) – Radiation tolerance: 1 Grad TID, 2x1016 neq/cm2
– Trigger rate up to 1 MHz, ~12.5 μs trigger latency

# Electronics in experiments




LpGBT

Bidirectional High Speed Serial Link

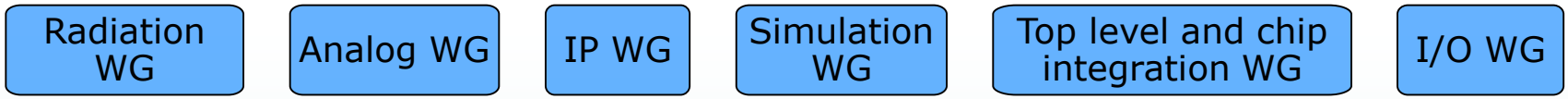
- Data rates:
  - 5 to 10 Gb/s for up links
  - 2.5 Gb/s for down links
- Environment
  - Temperature: -35 to + 60 °C
  - Total Dose: 100 Mrad qualification (200 Mrad LpGBT chipset)
  - Total Fluence: $2 \times 10^{15}$ n/cm2 and $1 \times 10^{15}$ hadrons/cm$^2$

# Circuits in 65nm technology

## *Goals of RD53 (65 nm technology)*

- Radiation qualification and characterization in 65 nm → guidelines for radiation hardness
- Development of tools and methodology to efficiently design large complex mixed signal chips
- Design and characterization of circuits and building blocks needed for pixel chips
  → design of shared rad-hard IP library
- Design and characterization of full scale demonstrator pixel chip

## *RD53 Working Groups (WGs)*




20 participating institutes : Bari, Bonn, CERN, CPPM, FNAL, LBNL, LPNHE, New Mexico, Milano, Padova, Pavia-Bergamo, Pisa, Perugia, Prague IP-FNSPE-CTU, PSI, RAL, Torino, UC Santa Cruz, Sevilla

# Circuits in 65nm technology

Third party IP vendors

Foundry PDKs

90 nm

45 nm

130 nm

65 nm

28 nm

Methodologies

CAE Tools

Complex Design Manufacturing Rules

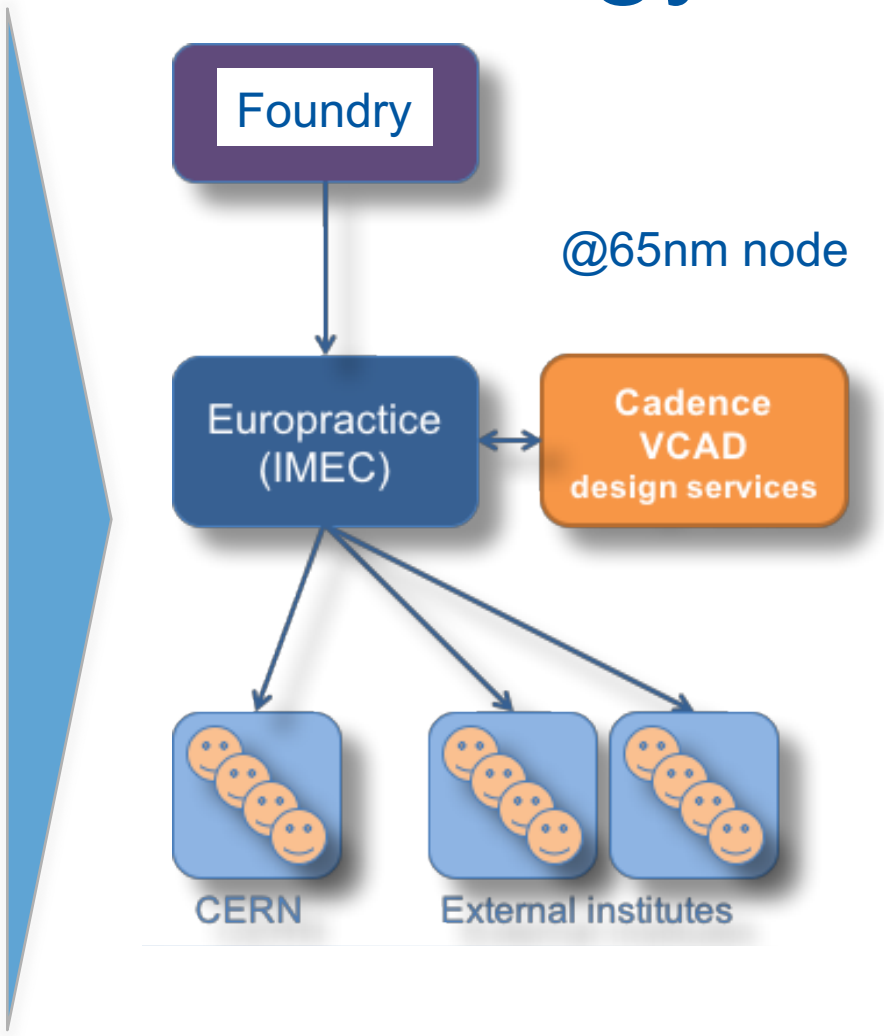
DRC deck file line count:

250nm: 5,300 lines

130nm: 13,500 lines

90nm: 38,400 lines

65nm: 89,300 lines



# Circuits in 65nm technology

Conclusion

- A large effort is going on at CERN and with the associated institutes to qualify a 65nm technology for the experiments upgrades
- Targets are highly segmented detectors and high bandwidth
- Dependencies found at “high” total dose, with complex annealing and dose rate relationships
- IP blocks under developments, through structured collaborations