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FIRST TELECOM APPLICATION OF DIGITAL AND MIXED COMPONENT DEVELOPMENTS: 65NM ASIC AND DATA CONVERTERS

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Outline

FAST project overview : TAS Digital Transparent Processor (DTP)

DTP Key technologies :

- ATMEL-ST-E2V 65nm ASIC
- E2V High speed Data Converters

Conclusion

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FAST DTP : TAS SPACEFLEX

The SpaceFlex Processor Perimeter

On-Board

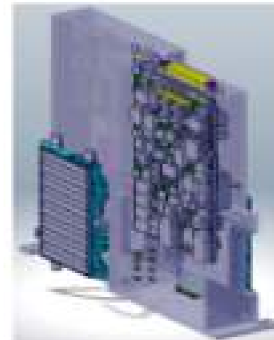
- Switches
- Conversion Chains
- Frequency reference
- Processing & routing (DTP)

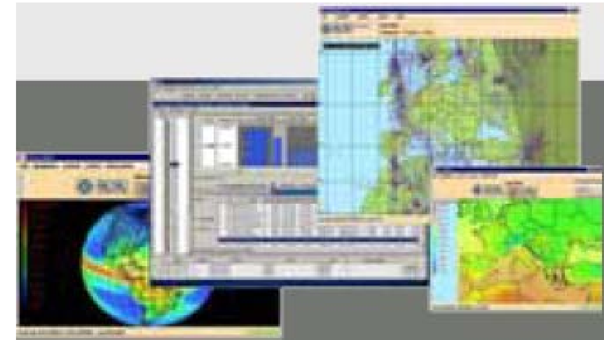
Command & Control

- High Speed Modem & processing

On-Ground

- Dynamic Management Software
- Operating Tool





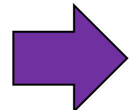
SpaceFlex Processor is a complete product offer from ground interface to space segment and fully scalable from SpaceFlex 2 [2 GHz] up to SpaceFlex 74 [74 GHz]

COMSAT NG

- COMSAT NG Program
  - New generation of defense telecommunications satellites
    - Renewal of in-orbit Syracuse 3 capabilities
    - Two satellites, first satellite in orbit in 2020

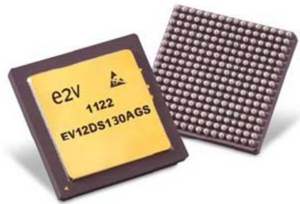
- Dual pre-developments
  - Under CNES responsibility
  - Programs :
    - **FAST : KO in 2012**
    - TELEMAK : KO in 2015

A new generation Digital Transparent Processor is necessary for COMSAT NG program



Dual Developments in progress at Thales Alenia Space

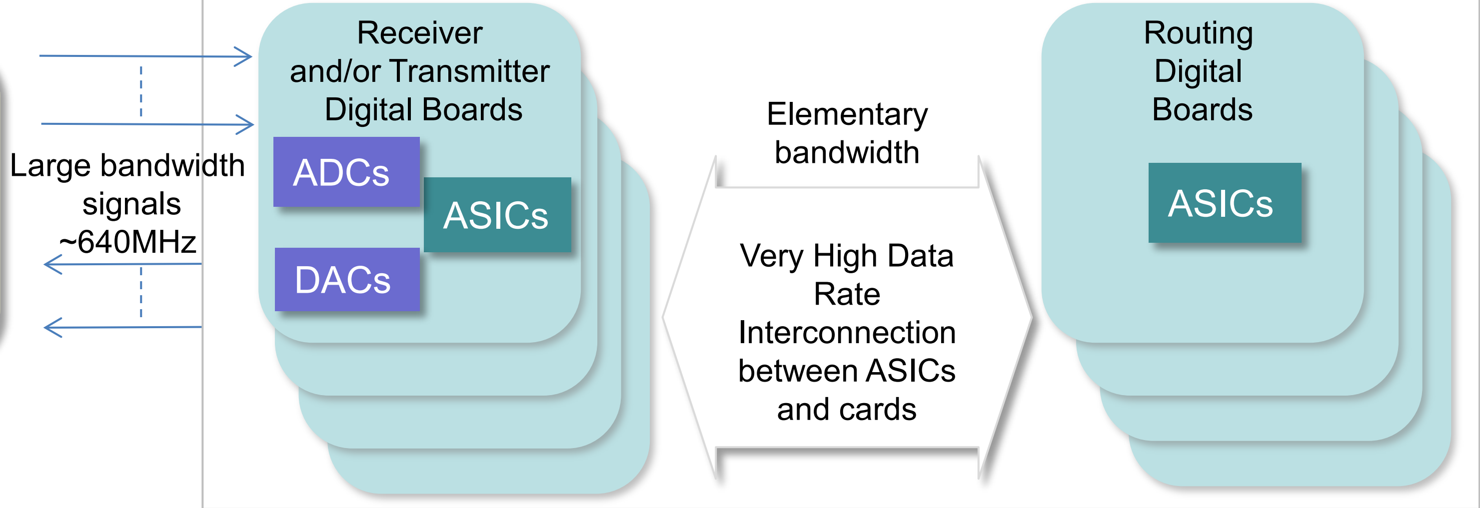
DTP : Key technologies



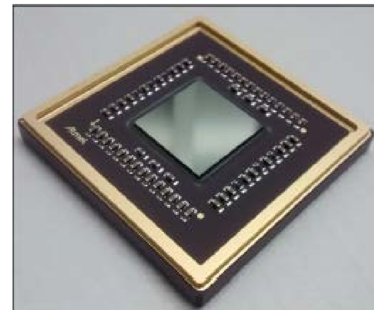
CNA EV12DS130A E2V

E2V Data converters

High speed
Large input bandwidth
Low power consumption
Multi channel



ATMEL-ST 65nm space ASIC
ATMEL-E2V Hermetic Flip-chip assembly
High integration
Low power consumption/Mbps
HSSL IP

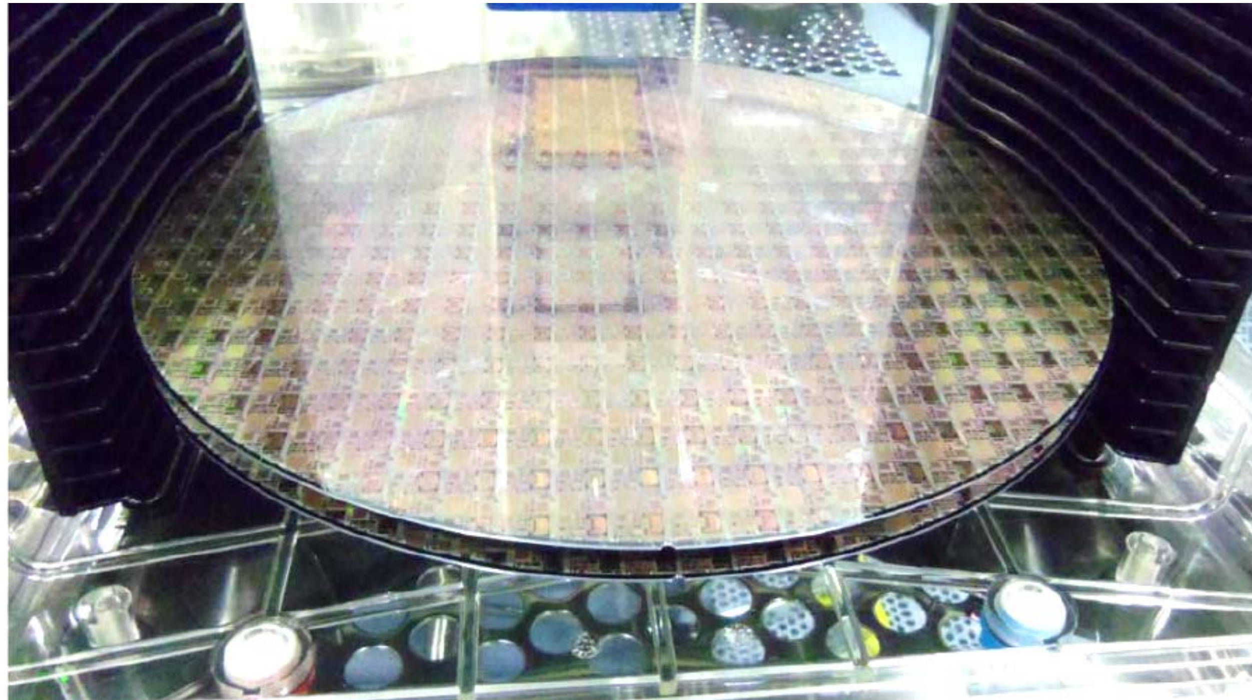


VT65 ASIC ATMEL-ST-TAS-CNES

Other disruptive technologies

Connectors
PCB
DCDC,

65NM ASIC



65nm wafer from ST

65nm ASIC offer : context

- In the frame of ESA and CNES supported activities, ST has developed the C65SPACE, a radiation hardened standard cell library for space, based on the 65 nm bulk process, produced in their fab in Crolles (F).

- 65nm supply chain proposed in 2010 by ST has been selected in 2012 by FAST project

- The C65SPACE platform is supplied by ATMEL with space qualification support, HSSL and Flip-Chip under the AT65RHA name.

For FAST DTP
ATMEL is the supplier of 65nm ASICs
which are based on ST process and e2V packaging

65nm ASIC offer : features

65 nm technology from ST Crolles (F)

>100 usable Mgates equivalent nand2

Hardening-by-Design

Designed In Reliability : Ageing models extended from 10 to 20 years

Supply voltages: 1.2V for core, 1.8V, 2.5V & 3.3V for periphery

Very low operating consumption < 0.5 nW/gate.MHz at 20% activity (target)

Maximum toggle frequency : 30 GHz

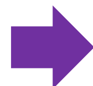
Compiled ROM, SRAM & DPRAM memories

LVDS (655 Mps)

PLL 6 phases 100MHz input / 1.2GHz output

HSSL up to 6.25Gbps

Typical signal I/O’s > 1000 – Hermetic Flip-Chip technology



Disruptive technology

Key performances for DTP

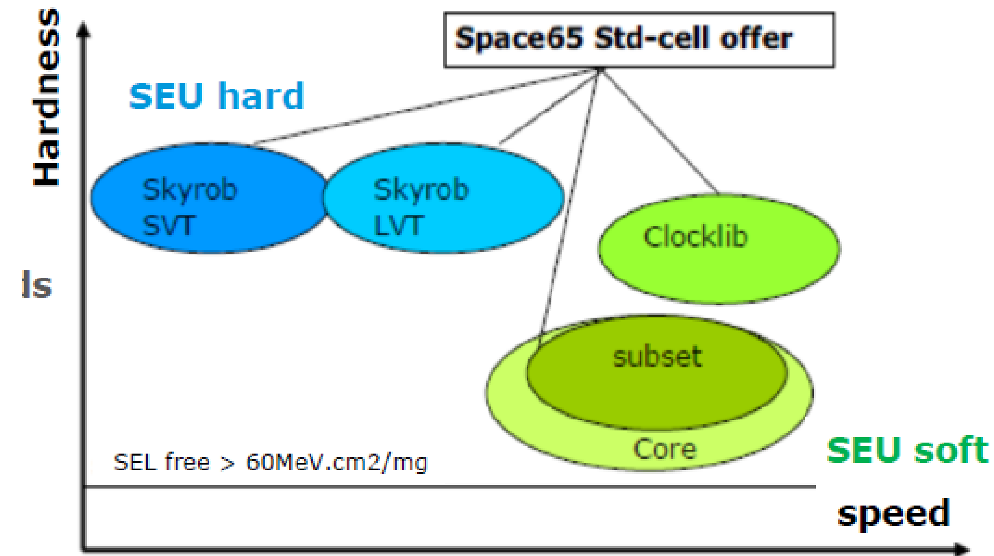
65nm ASIC offer : list of IP

Cell	Memory	IO	Analog
Low leakage	Single Port High Speed	Cold Spare 1V8/2V5/3V3	200-1200MHz 6 phases 40ps/200MHz
Low power	Single Port Register File	LVDS 2V5	200-1200MHz 6 phases new divider factor
Delay	DualPort REG	I2C	Rad-hard Thermal Sensor
High speed	ROM	Basic	
Balanced	ECC	ESD enhanced	
Gated clock	BIST	Flip-chip	
Place & Route	DualPort HD/HS	HSSL 6.25Gbit/s	
Rad-hard		Double rows	
Rad-hard 1GHz		Fast LVDS	

65nm ASIC offer : radiation performances

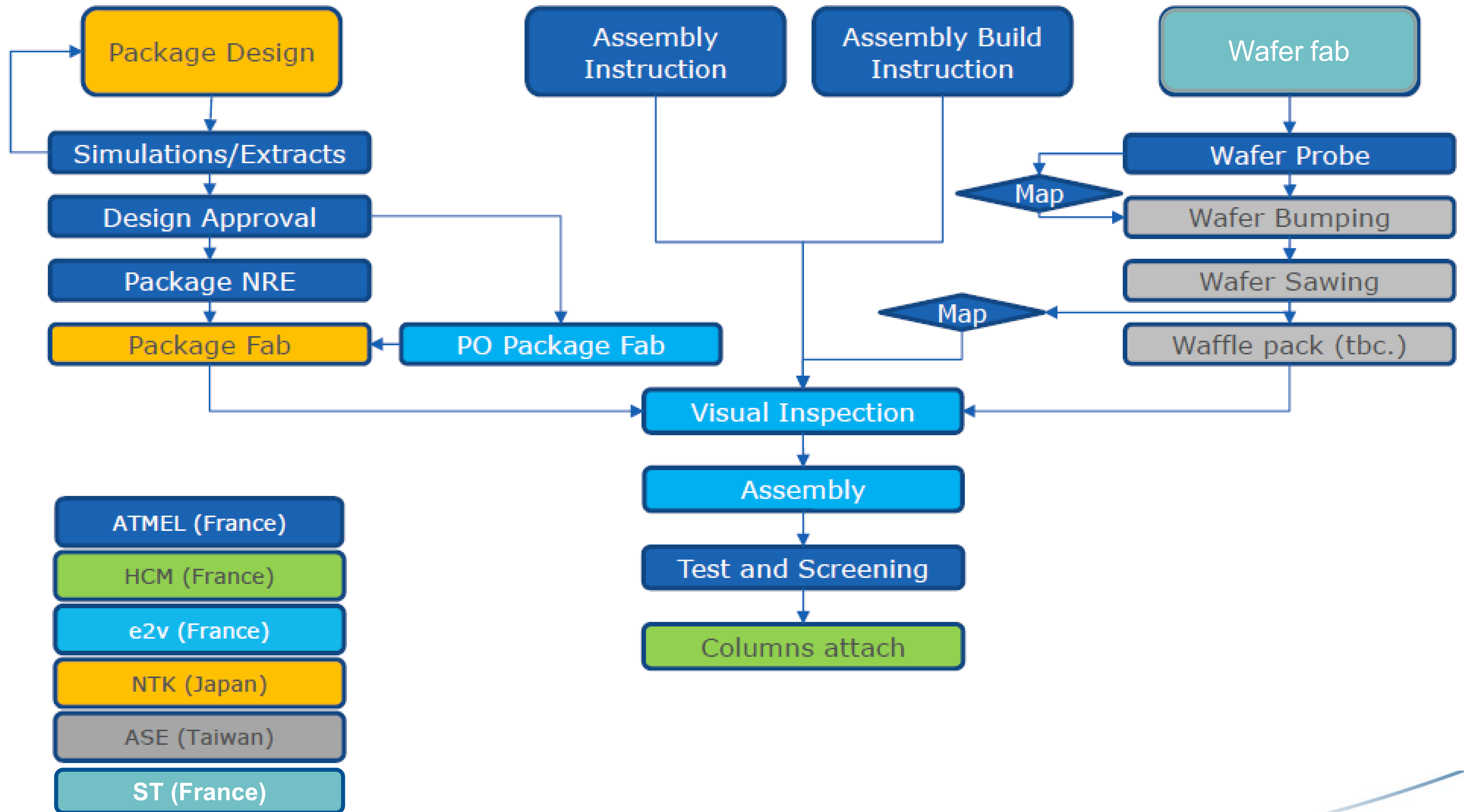
Feature	65nm Library Performances
SEL	No SEL below LETth of 60MeV/mg.cm² at Vccmax
SEFI	No SEFI detected on libraries
SEU	SEU cross section are available
TID	Technology suitable up to 300Krad5si) for Vccmax

Std cells libraries	Target
SKYROBLPSVT	Radiation Hardened with standard Vt transistors
SKYROBLPLVT	Radiation Hardened with low Vt transistors (faster)
CORE65LPSVT	Library offering a wide range of combinational and sequential cells for area/power optimisation, without specific radiation hardening
CLOCK65LPSVT	Clock-tree cells designed to mitigate duty cycle distortion on clock trees networks

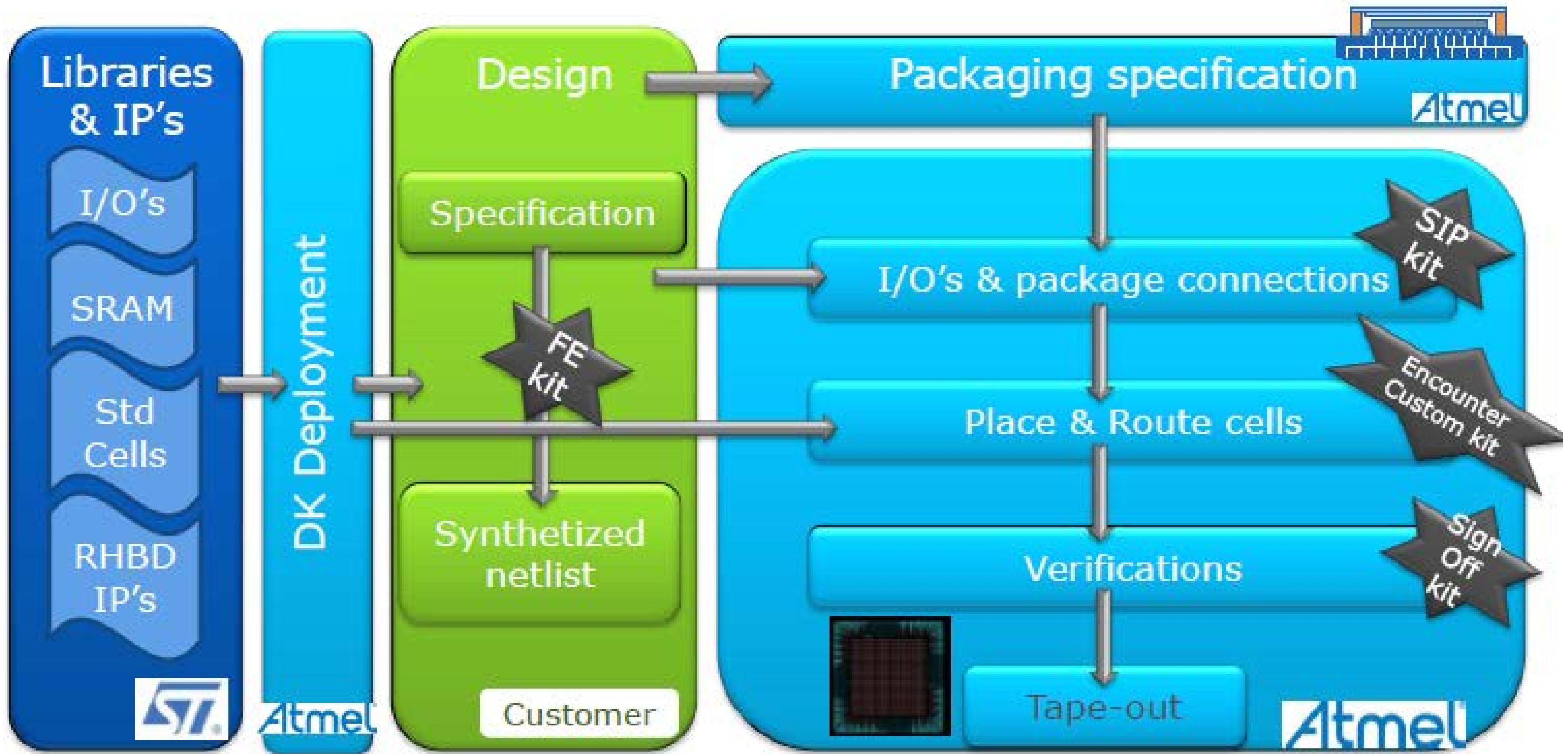


SEU rate improvment for SKYROB ranging from 80 to 500

AT65RHA Supply Chain



AT65RHA Design flow

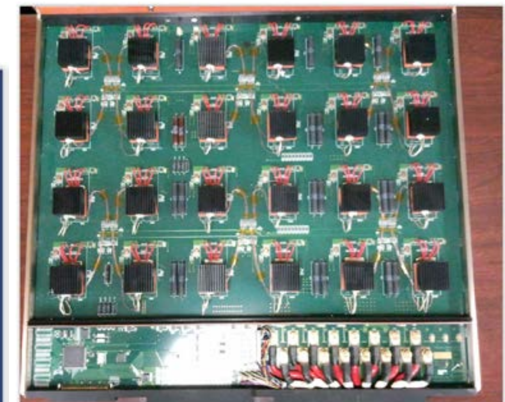


ATMEL test capabilities for 65nm ASICs

- 300mm wafer Prober

- High performance tester for Digital and Analog: Xcerra Sapphire
  - 400 MHz, up to 800 Mbits/sec, 768 digital pins, High accuracy

- High Power Burn-in system
  - Dynamic Burn-In
  - Testing capabilities for high-power devices.
  - Individual Temperature Control
  - Up to 8 different pattern zones with one burn-in board per zone.



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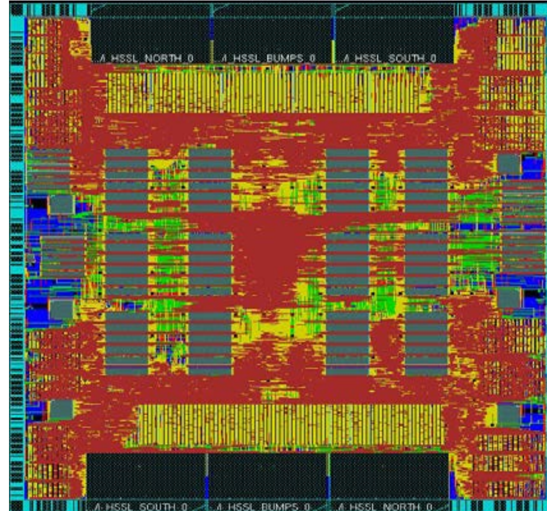
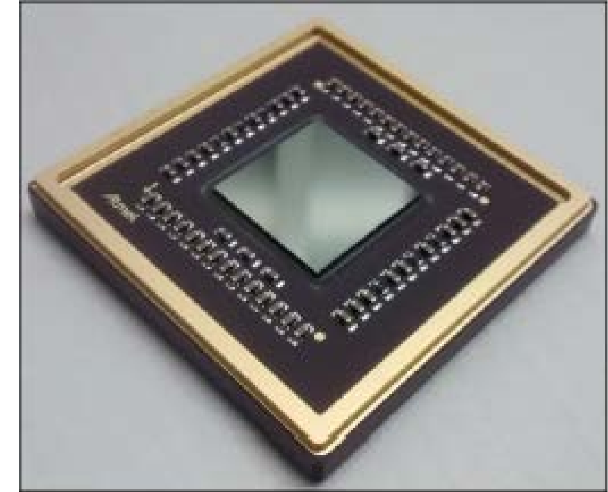
1st 65nm ASIC : TAS-ATMEL-ST VT65

VT65 ASIC characteristics :

- Working Frequency > 600 MHz
- Technology : AT65RHA
- Core Power supply : 1.2V
- IO : 3.3V & 2.5V
- Package > 1600 IO
- Usefull pins > 500



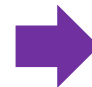
VT65 ASIC die > 200mm²



VT65 ASIC in CCGA1752 package

Core Cells summary:

- > 40 Mgates eq.
- > 600 memories
- HSSL IP (6.25Gbps)
- PLL IP (100MHz input / 1.2GHz output)
- THSENS IP
- Cold Sparing buffers
- LVDS (655Mps)



For a same design,
Frequency is x 2
Layout area is ÷ 2 to 3
with 65nm vs 180nm

Total transistors > 200 Million

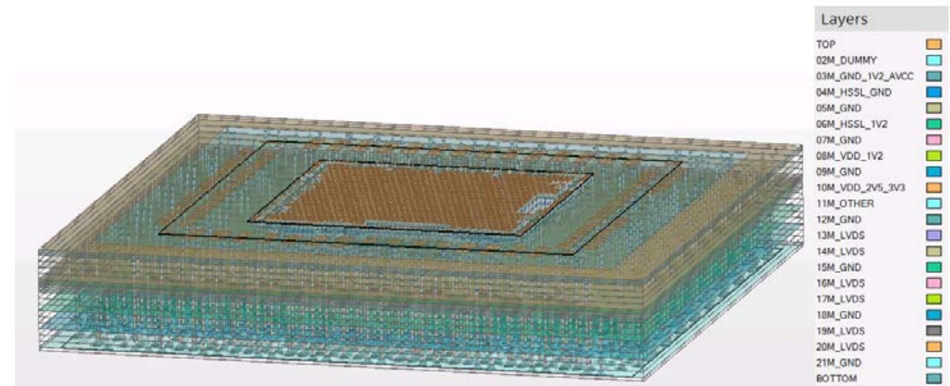
VT65 ASIC : CCGA1752
Flip-chip package

Flip-chip package is mandatory :

- **Complexity and I/O number**
- **HSSL link performances**

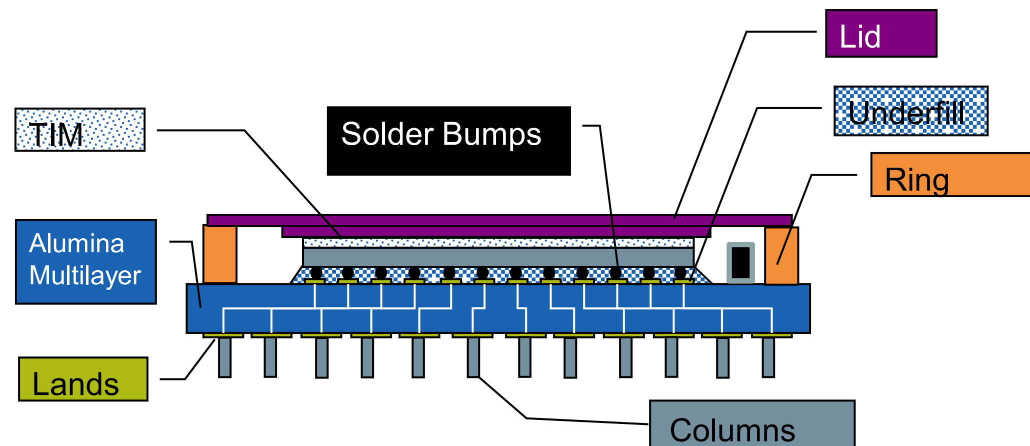
Hermetic Package

- CCGA1752 (alumina – 18 layers)
- Body size: 45x45mm - 4.2mm thick
- Design by Atmel, Assembly done by E2V

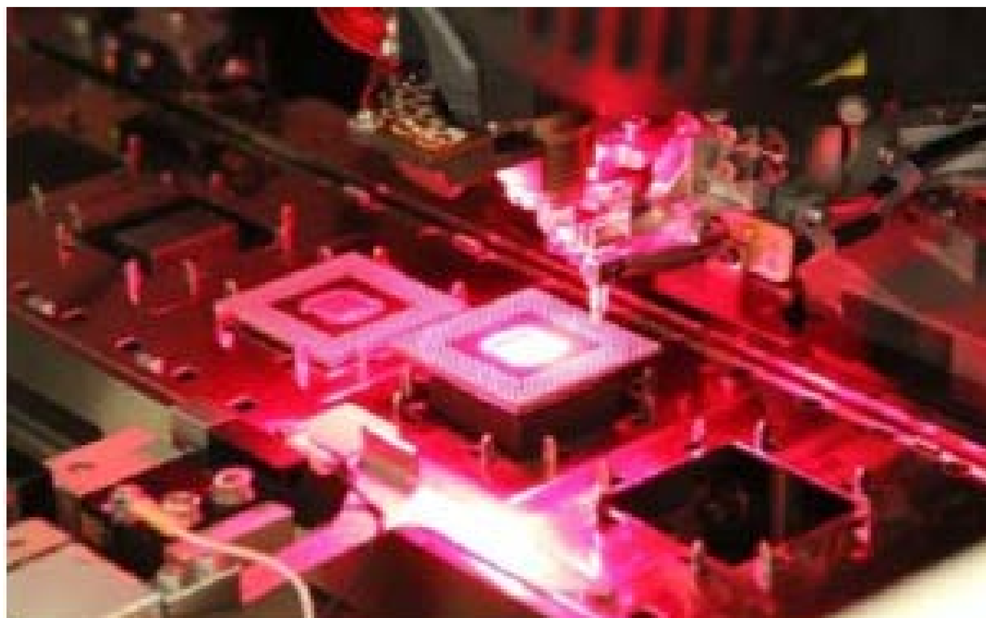


Die

- Die Size 15.4x15.4mm
- Bumps count: 3814



DATA CONVERTERS



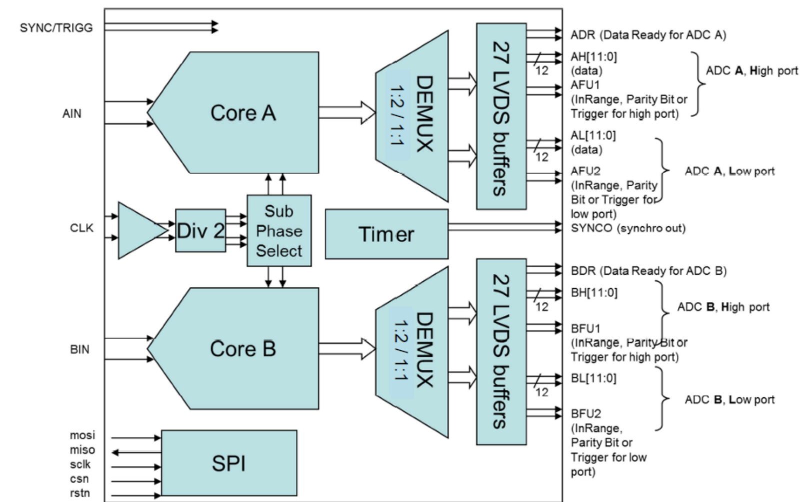
E2V assembly line

E2V EV12AD550 ADC

Developement and ESCC evaluation in the frame of CNES and DGA programs

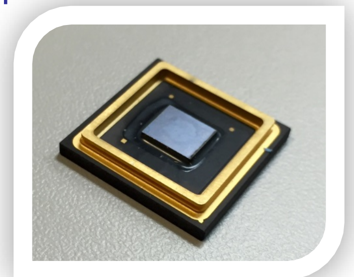
ADC Main Features :

- Dual channel ADC
- 12-bit resolution
- 1.5 Gsps conversion rate
- Large input bandwidth up to ~3,7GHz
- LVDS parallel outputs 1:2-1:1 DEMUX.
- 2.1 W typ in 1:1 DEMUX ratio per core



EV12AD550 block diagram

- Flip-chip Hermectic package CCGA323 (AIN 21x21mm, Pitch 1.0mm)
- 130nm BiCMOS from ST (F)



EV12AD550 is under Evaluation

- **Electrical characterization and Radiation tests completed**
- **ESCC evaluation and in progress**

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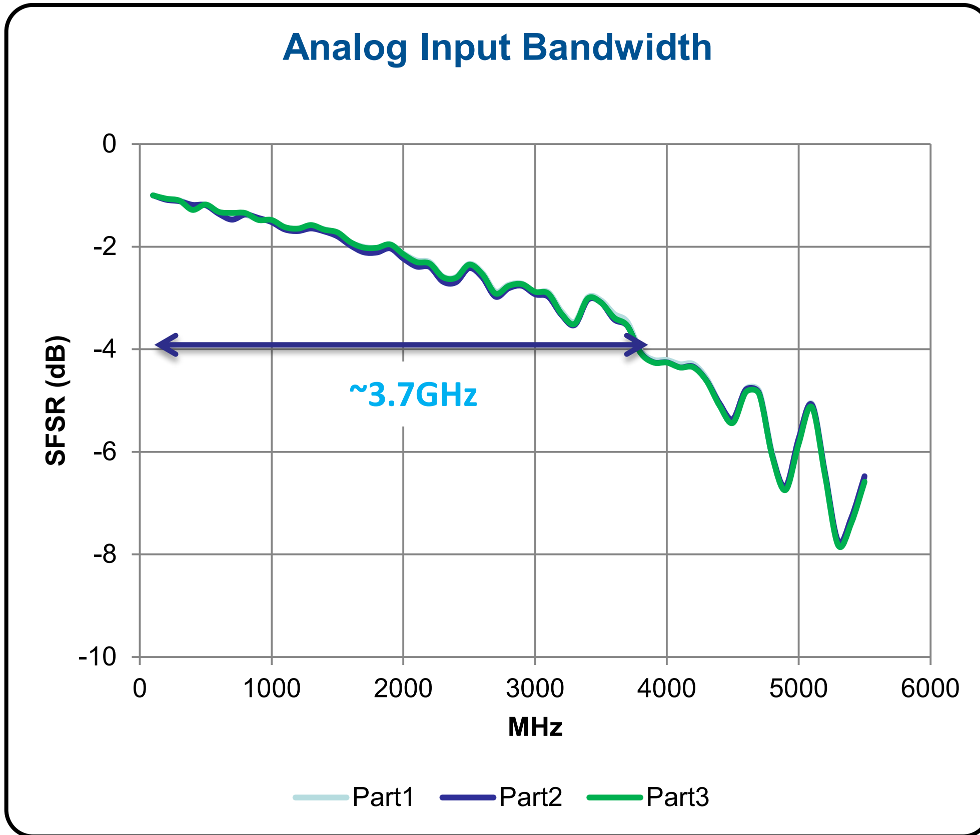
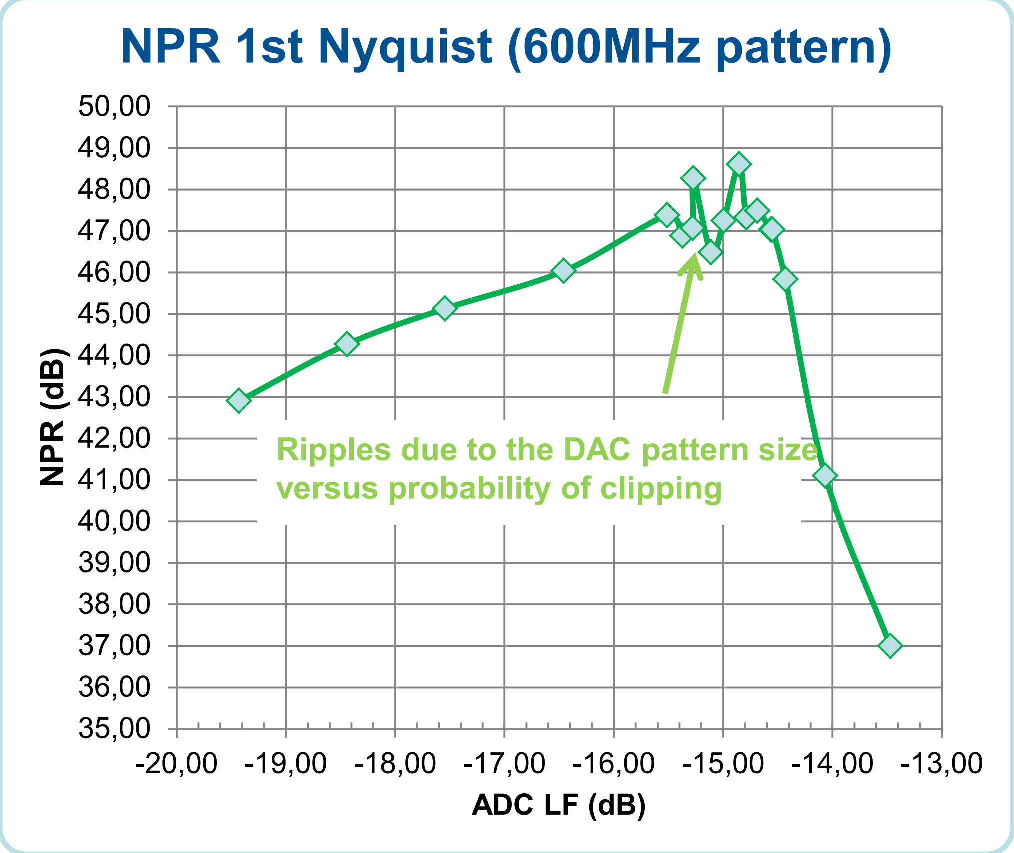
EV12AD550 Bandwidth and Broadband performances

FAST





Large input bandwidth up to ~3,7GHz

NPR ~ 48 dB in 1st Nyq. at -15dB loading factor

EV12AD550 Output Spectrums

Fs = 1500MSps, Fin = 2980MHz / -12dBFS

Fin = 2980MHz / -12dBFS

H2 H3 H4 H5 H7 H9

ENOB = 9.21 bit
SNR = 58.0 dBFS
THD = -65.0 dBFS
SFDR = -67.0 dBFS (H2)
SINAD = 57.24 dBFS

dBFS: 0, -10, -20, -30, -40, -50, -60, -70, -80, -90, -100, -110

MHz: 0, 100, 200, 300, 400, 500, 600, 700

Fs = 1500MSps, Fin = 1480MHz / -12dBFS

Fin = 1480MHz / -12dBFS

H2 H3 H4 H5 H7 H9

ENOB = 9.44 bit
SNR = 58.9 dBFS
THD = -70.4 dBFS
SFDR = -75.4 dBFS (H3)
SINAD = 58.6 dBFS

dBFS: 0, -10, -20, -30, -40, -50, -60, -70, -80, -90, -100, -110

MHz: 0, 100, 200, 300, 400, 500, 600, 700

E2V EV12DS130A DAC

- **Development and ESCC evaluation in the frame of CNES program**

- **DAC Main Features :**
  - 12-bit resolution
  - 3 Gsps Conversion rate
  - 6 GHz analog output bandwidth
  - 4:1 or 2:1 built in MUX (selectable)
  - 1.3 W Power Dissipation
  - NRZ, Narrow RTZ, 50% RTZ, RF modes
  - IUCM mode (Patent e2v/CNES)
  - SEL& SEFI free, 110 krads
  - Ci-CGA255 Package (21x21mm, pitch 1,27mm)
  - B7HF200 SiGeC techno. from Infineon (G)

- 1st Nyquist (NRTZ): NPR = 51.3dB at Fs = 3Gsps
- 1st Nyquist (NRTZ): NPR = 55.7dB at Fs = 1.5Gsps
- 2nd Nyquist (NRTZ or RTZ): NPR = 44.6 dB at Fs = 3 Gsps
- 3rd Nyquist (RF): NPR = 42.5 dB at Fs = 3 Gsps

EV12DS130A is used on Telecom projects

- **ESCC evaluation completed since 2012 : very good performances, reliability and radiation results**
- **QMLV qualified in 2015**

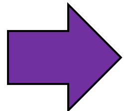
Conclusion

- DTP Key performances :
  - 640 MHz digitalized bandwidth
  - Many tens of GHz of full capacity
  - Cost decreases in Mass/consumption/volume per GHz

- ASIC Key performances :
  - High speed link: 6,25Gbps rad-hard HSSL IP
  - High integration with 65nm ASIC die size up to 400 mm²
  - > 600 MHz working frequency
  - Flip-chip Packaging

- Data converters Key performances:
  - High speed >1,5Gsps
  - L-band & S-band
  - Integration with multi channel
  - Low power consumption ~ 2W
  - Flip-chip Packaging

DTP is a high tech product with high innovation
For drastically enhanced performances



Constructive collaboration between all the FAST partners, Telecoms, Technologists, Components engineers and Manufacturers

Acknowledgements

ATMEL : AT65RHA team

ST : C65Space team

E2V : CALLISTO team

TAS : FAST team

CNES : FAST team

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DGA : G.Jestin

Thank you !

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