On the Design of a Rad-Hard Signal Conditioning ASIC for Pressure Modules

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Abstract

European Sensor Systems has designed, fabricated and tested a radiation tolerant signal conditioning ASIC for capacitive sensors in the course of an ESA activity for "Standard Accuracy Pressure Transducer". This paper presents the architecture of the ASIC, the radiation mitigation strategy, the electrical characteristics and the radiation results.

I. INTRODUCTION

European Sensor Systems develops and manufactures high quality sensors based on MEMS technology. In the course of ESA activity "Standard Accuracy Pressure Transducer" [1], European Sensor Systems has been developing a "Space Qualified Family of MEMS Pressure Modules for Satellite Applications". European Sensor Systems has designed four MEMS sensors to cover the application's pressure ranges (7, 22, 150, 310 bar) with dimensions 2×2×0.4 mm^3 using European Sensor Systems TM30P1111 technology, which is a combination of SOI, bulk and surface micro-machining process for the fabrication of capacitive pressure sensors. European Sensor Systems is the IP owner and exclusive user of this process.

A custom radiation-hardened capacitive sensor signal conditioning ASIC has been designed to interface with the MEMS. Based on the architecture of its commercial counterpart ASIC, the chip is built using X-FAB XH018 Process, a 0.18 micron Modular Mixed Signal HV CMOS Technology.

The structure of the paper is as follows. Section I presents the detailed architecture of the ASIC, Section II presents the radiation mitigation strategy, Section III presents the ASIC characteristics and Section IV presents the radiation results.

II. ARCHITECTURE OF THE ASIC

The architecture of the ASIC is shown in Figure 1. It is a mixed-signal radiation-hardened capacitive sensor signal conditioning ASIC.

The external voltage supply is 5.7V and is internally regulated to 3.3V both for the analog and digital part. The core of the ASIC is the capacitance-to-voltage converter. The output of this block is converted to a 1-bit output by second-order ΣΔ modulator, which is then down-sampled and low-pass filtered in the digital domain.

The ASIC provides two pressure outputs: a 32-bit digital output accessible via the serial communication interface along with a Pulse Width Modulation output bit stream of 10-bit resolution.

The ASIC also features an internal temperature sensor with a 32-bit digital output accessible via the serial communication interface.

The trimming of the device is performed via register programming using an I^2C compatible Two Wire Interface (TWI). A specific configuration can be written to the One Time Programmable (OTP) memory. The internal analog and digital regulator, the bandgap reference, the oscillator and the power-on reset eliminate the need of any additional components.

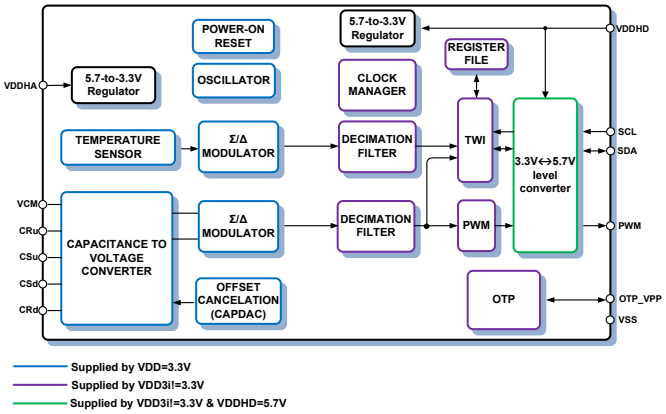

Figure 1: Functional block diagram of ASIC

A. Voltage regulation scheme

The ASIC has two distinct power domains: the 3.3V digital domain and the 3.3V analog domain with common ground. The chip is supplied by Texas Instruments' LM117 [2], which is configured to provide 5.7V. The output voltage of the external regulator needs to be converted to 3.3V for the operation of the digital and analog sub-blocks. This is realized using a 5.7-to-3.3V regulator for the digital part and a 5.7-to-3.3V regulator for the analog part. The I/O communication is performed using the high 5.7V supply in conjunction with appropriate level-shifting of 3.3V to 5.7V and vice-versa.

B. Capacitance to Voltage Converter

MEMS capacitive pressure sensors consist of two sense capacitors ($C_{Su,}$ C_{Sd}) and two reference capacitors ($C_{Ru,,}$ C_{Rd})

and typically have a steady-state capacitance C_0 in the order of few pF. MEMS capacitors share a common plate. The Capacitance to Voltage Converter implements Eq. (1).

$$\Delta V_{OUT} = \frac{\left(C_{Su} - C_{Ru} + C_{Sd} - C_{Rd}\right)}{C_F} \cdot \frac{V_{DD}}{2} \qquad \text{Eq. (1)}$$

where C_F is an internal capacitor for gain adjustment in a fully differential configuration. The fully differential topology offers many advantages such as rejection of common mode non-idealities and noise and suppression of even order non-linearities. Noise reduction techniques were implemented to reduce the low-frequency noise and offset.

Offset cancellation capability is implemented by digitally trimming internal capacitor arrays in parallel to each MEMS input capacitor.

C. ΣΔ A/D converter

ΣΔ modulators are low complexity oversampling A/D converters appropriate for baseband narrowband applications. The theoretical Signal to Noise Ratio (SNR) of an L^{th} order modulator with an N-bit quantizer and decimation rate DR is given by Eq. (2).

$$\text{SNR}=10log_{10}\left[\frac{3}{2}\left(\frac{2L+1}{\pi^{2L}}\right)(2^N-1)^2 DR^{2L+1}\right] \qquad \text{Eq. (2)}$$

The design of the modulator is based on a switched-capacitor topology with implementation of noise reduction techniques to eliminate the noise. It is a second-order topology based on a cascade of resonators with 1-bit quantizer. It combines a non-delaying and a delaying integrator to form a stable resonator. The choice of 1-bit quantizer is a compromise between complexity and performance.

The outputs of the capacitance-to-voltage converter Vout-p and Vout-n are sampled by the modulator. The 1-bit output is processed by a low-pass decimation filter. The architecture of the filter is based on cascaded integrator-comb (CIC) filter. By using a CIC filter the computational complexity is reduced compared to narrowband low-pass Finite Impulse Response (FIR) filters. An efficient way to realize a decimation filter consists of a series of L cascaded accumulators followed by a cascade of L differentiators [3] implementing Eq. (3).

$$\text{H(z)}=\left[\left(\frac{1-z^{-M}}{1-z^{-1}}\right)^L\right] \qquad \text{Eq. (3)}$$

where L is the order of the filter and M is the differential delay.

D. Pulse Width Modulation Unit

The filtered output of the CIC filter is converted to a 10-bit resolution pulse width modulation (PWM) bit stream at the frequency of 10 KHz, which corresponds to the raw analog signal from the sensor. The PWM signal is then filtered off-chip by an RC filter in order to generate an analog signal. The PWM output pulse can be adjusted in terms of scale factor and offset.

III. RADIATION MITIGATION STRATEGY

In order to address the problem of Single Event Upsets (SEUs), the Triple Module Redundancy (TMR) method with voting has been adopted. This mitigation scheme uses three identical logic circuits performing the same task in parallel with corresponding outputs being compared through a majority voter circuit. The technique has been applied at the level of digital synthesis. The TMR technique has been applied to all flip-flops of the digital part.

For Single Event Latch-up (SEL) immunity in the digital part, a library of custom digital cells has been designed and modeled in house. The library contains combinational, sequential and special cells (layout fillers, antenna protection cells). It was based on existing cells of the digital library D_CELLSL_JI3V (triple-well junction isolated cells for 3.3V operation). The increase of the layout area of the rad-hard cell compared to its conventional counterpart varies from 2x to 4x.

In the analog part, all PMOS devices have been enclosed by N-type guard rings and all the NMOS devices have been enclosed by P-type guard rings.

IV. ELECTRICAL CHARACTERISTICS

The layout of the ASIC is shown in Figure 2.

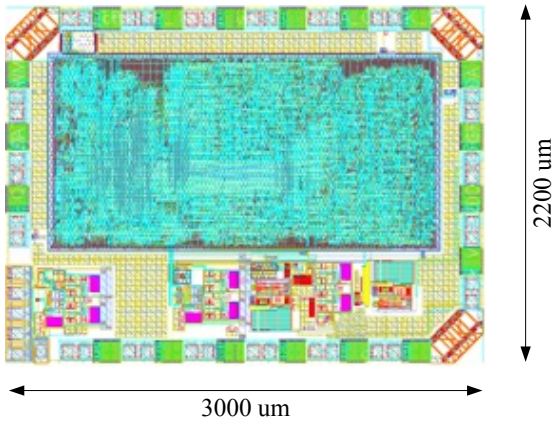

Figure 2: ASIC layout

The PCB with the fabricated ASIC and MEMS is shown in Figure 3.

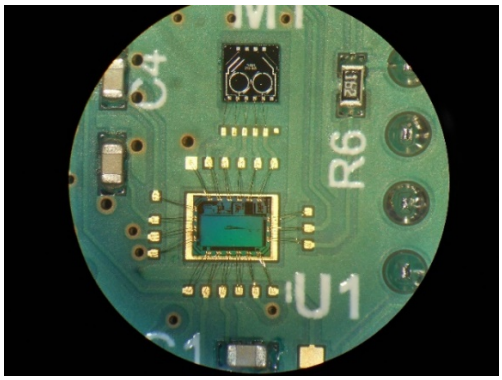

Figure 3: PCB with ASIC and MEMS

The ASIC characteristics are summarized in Table 1.

Table 1: ASIC Characteristics

VOLTAGE/CURRENT LEVELS	
Analog Part Voltage Supply (VDDHA)	5.2V-6.2V
Digital Part Voltage Supply (VDDHD)	5.2V-6.2V
Regulated Analog Voltage	3.3V, PSRR 50 dB @1KHz
Regulated Digital Voltage	3.3V, PSRR 50 dB @1KHz
OTP Programming Value	7.2V
Current Consumption	7mA
CLOCK	
Oscillator Frequency (programmable)	10MHz
CAPACITANCE TO VOLTAGE CONVERSION	
C_0: Base Capacitance	20pF (typ) to 100pF (max)
ΔC: FS Input Capacitance Range	± 2.8 pF
Digital Pressure Output Resolution	> 19 bits @10 Hz
Decimation Rate (BW)	256-32768 (1.3KHz-10Hz)
PWM OUTPUT	
PWM resolution	10-bits
PWM frequency	10 KHz
TEMPERATURE SENSOR	
Accuracy	±1°C
Resolution	0.1°C
Sensitivity	1.6 mV/°C
ENVIRONMENTAL CONDITIONS	
Temperature Range	-40°C to 100°C
SERIAL COMMUNICATION INTERFACE	
Two Wire Interface, I^2C compatible	
ISD Interface	

V. Preliminary Radiation Tests Results

For the radiation tests a low-pass RC filter with cut-off frequency f_c at 10 Hz is used.

Ten ASICs –shown in Figure 4- have been tested for Total Ionization Dose (TID) up to 100 Krad at ESA ESTEC facility.

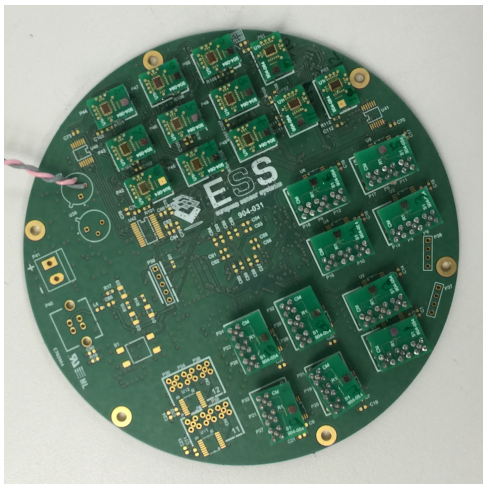

Figure 4: PCB with mounted DUTs for TID

Figure 5a shows that the digital pressure output varies less than 1 mV over all irradiation steps. Figure 5b shows a drop of approximately 325mV in the RC filtered PWM output versus TID dose.

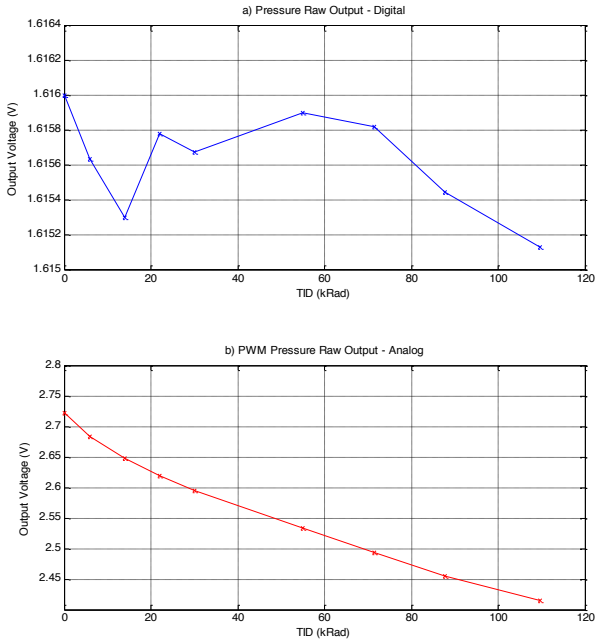

Figure 5: a) Pressure raw digital output b) PWM pressure output vs. TID dose

The digital output of the PWM block has a range of 0V to 3.3V. It is up-converted to the range of 0V to 5.7V. The inverter of the last stage of the level-converter is implemented using high-voltage transistors (Figure 6). Due to irradiation the off-resistance of transistor M_1 is decreasing [4], thus its sink current is increasing explaining the voltage drop shown in Figure 5b.

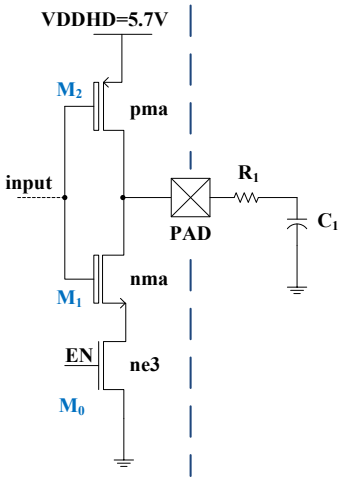

Figure 6: Output stage of 3.3V-to-5.7V level converter and RC filter

Figure 7a shows the outputs of the analog (blue line) and digital (green line) regulators. The experimental shift (increase) over radiation is about 1%, and is attributed to the incorporation of several High-Voltage transistors, as in the case of the regulators' pass element.

Figure 7b shows the digital temperature output (solid blue line). The predicted digital temperature output (dashed blue line, Figure 7b), assumes constant temperature and takes into account the aforementioned analog regulator's output shift. By comparing the two curves, it is deduced that the analog regulator's output shift, is mostly responsible for the shift on the digital temperature output. The remaining difference is well within the environment's temperature variation, suggesting that the temperature sensor, which is based on a bandgap-type circuit with bipolar transistors, is also tolerant to TID (up to 100 Krad).

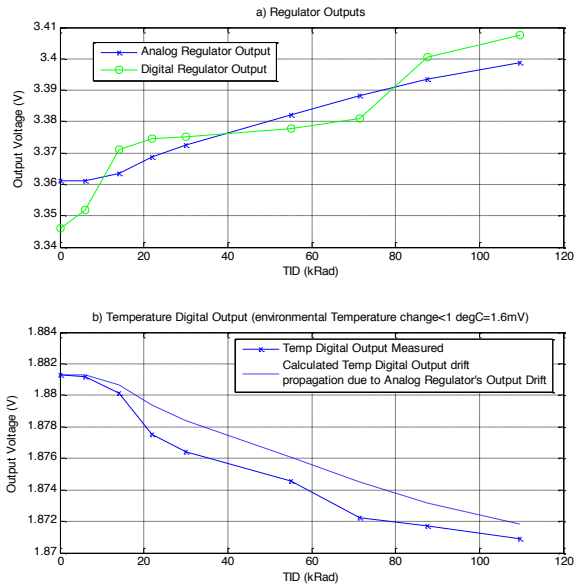

Figure 7: a) Regulator outputs b) Temperature Digital output

Three ASICs have been tested for SEE/SEL in the UCL cyclotron accelerator facility – as shown in Figure 8. The ASIC exhibited SEL immunity up to 62.5 MeV/(mg/cm^2) using Xe-995. Instantaneous increases of current consumption were visible in the digital part and can be attributed to SEFIs. Restore to normal operation performance occurred without any external intervention.

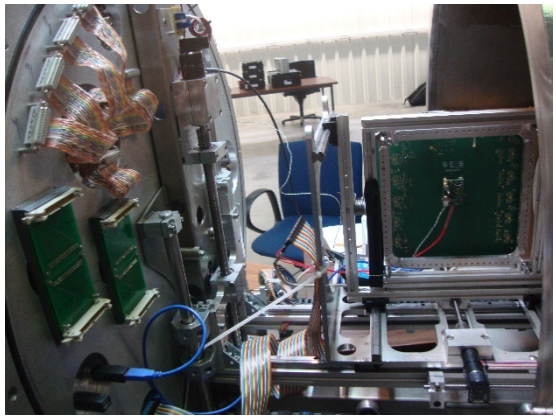

Figure 8: SEE test setup

Preliminary post-processing of irradiation results suggests SEU immunity at least up to 32.4 MeV/(mg/cm^2) using Kr-769.

Displacement damage tests have been performed at three ASICs at UCL up to 62 MeV and a LET of $8.39 \cdot 10^{-3}$ MeV/(mg/cm^2) without any performance degradation.

VI. Conclusions

The design of radiation tolerant ASIC in a standard 0.18um CMOS process has been presented. The fabricated chip exhibited immunity to SEL, SEU and DD proving that the radiation mitigation strategy was successful. TID up to 100 Krad did not affect the ASIC's core, which utilizes Low-Voltage transistors, while High-Voltage transistors are responsible for any performance degradation.

European Sensor Systems is currently assessing the necessary redesign steps to address the above issues.

VII. References

[1] ESTEC Contract No: 4000 111841/14/NL/CBi

[2] Texas Instruments, LM117, LM317-N Wide Temperature Three-Pin Adjustable Regulator Datasheet Available: http://www.ti.com/lit/ds/symlink/lm117.pdf

[3] E. Hogenauer, (1981). "An economical class of digital filters for decimation and interpolation". IEEE Transactions on Acoustics, Speech and Signal Processing, Vol. ASSP-29, No 2, p. 155–162.

[4] D. Moroni (Airbus DS) et al, "Radiation-Tolerant High-Voltage ASIC Library Evaluation for Space Applications", AMICSA 2014.