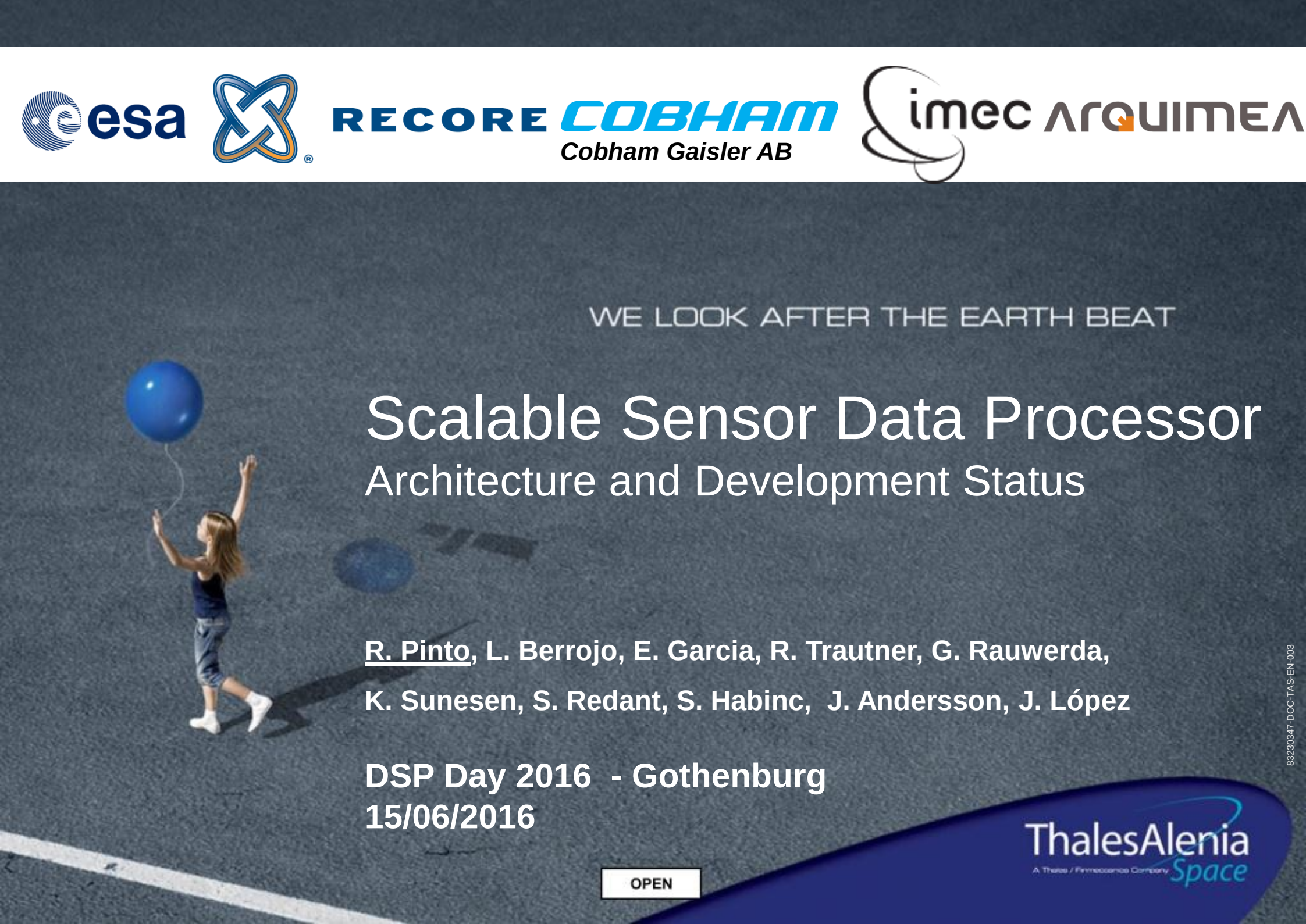
esa
RECORE
COBHAM
Cobham Gaisler AB
imec ARQUIMEA
WE LOOK AFTER THE EARTH BEAT
Scalable Sensor Data Processor
Architecture and Development Status
R. Pinto, L. Berrojo, E. Garcia, R. Trautner, G. Rauwerda,
K. Sunesen, S. Redant, S. Habinc, J. Andersson, J. López
DSP Day 2016 - Gothenburg
15/06/2016
OPEN
ThalesAlenia Space
A Thales / Finmeccanica Company
83230347-DOC-TAS-EN-003

# Outline



- Introduction
- Architecture
- Prototyping Support
- Status
- Conclusion

# Introduction



- The Scalable Sensor Data Processor (SSDP) has been commissioned by ESA on the scope of the CTP programme, aimed at being used by next-generation instruments, payloads and robotic exploration applications, e.g. rovers and landers
- The SSDP is a “One-stop shop” mixed-signal ASIC, offering control and data processing resources together with a diverse set of Input/Output interfaces together with Data Acquisition and Conversion in the same package
- Cost-effective alternative to ASICs and FPGAs upon design of instruments, payloads and even spacecraft control, e.g. ICUs, DPUs, OBCs and robotic exploration applications both at processing and sensors & actuators level

# Introduction
## SSDP Use Cases



- On-board Data Processing
  - DPU – Data Processing Unit
    - Data processing, e.g. Filtering, Compression, Encryption, etc.
    - Avionics Networks
  - ICU – Instrument Control Unit
    - Data Acquisition
    - General Purpose I/O and Avionics Networks
- On-Board Computer
  - Real-Time Operating System support, e.g. RTEMS (or VxWorks)
  - Time- and House-keeping
  - Avionics Networks
- Robotic Exploration
  - Image & Vision Processing
  - Sensors and Actuators
  - Drive Control
  - …

- Massively Parallel Processor Breadboard – MPPB
  - TRP aimed at validating multicore DSPs for Space applications
  - Heterogeneous Computer Architecture, 2x DSPs + 1x GPP
    - DSPs : Recore Xentium
    - General-Purpose Processor: Cobham Gaisler LEON2
  - Software Development Environment (SDE)
- IMEC DARE180 (DARE Digital Cells in UMC 180 nm tech.)
  - **D**esign **A**gainst **R**adiation **E**ffects Cell Library
  - Heavy Ion Tolerant (HIT) Flip-flops
  - TID: tested up to 1 Mrad (Si)
- Analogue Blocks from Cosmic Vision, e.g. Fast ADC

# Introduction
## SSDP Industrial Consortium



**Prime, ASR, ADD, V&V**

ThalesAlenia Space
A Thales / Finmeccanica Company

**Library, Layout, Packaging, Manufacturing & Testing**

imec

**Commercialization**

COBHAM
Cobham Gaisler AB

**IP & Support**

RECORE

COBHAM
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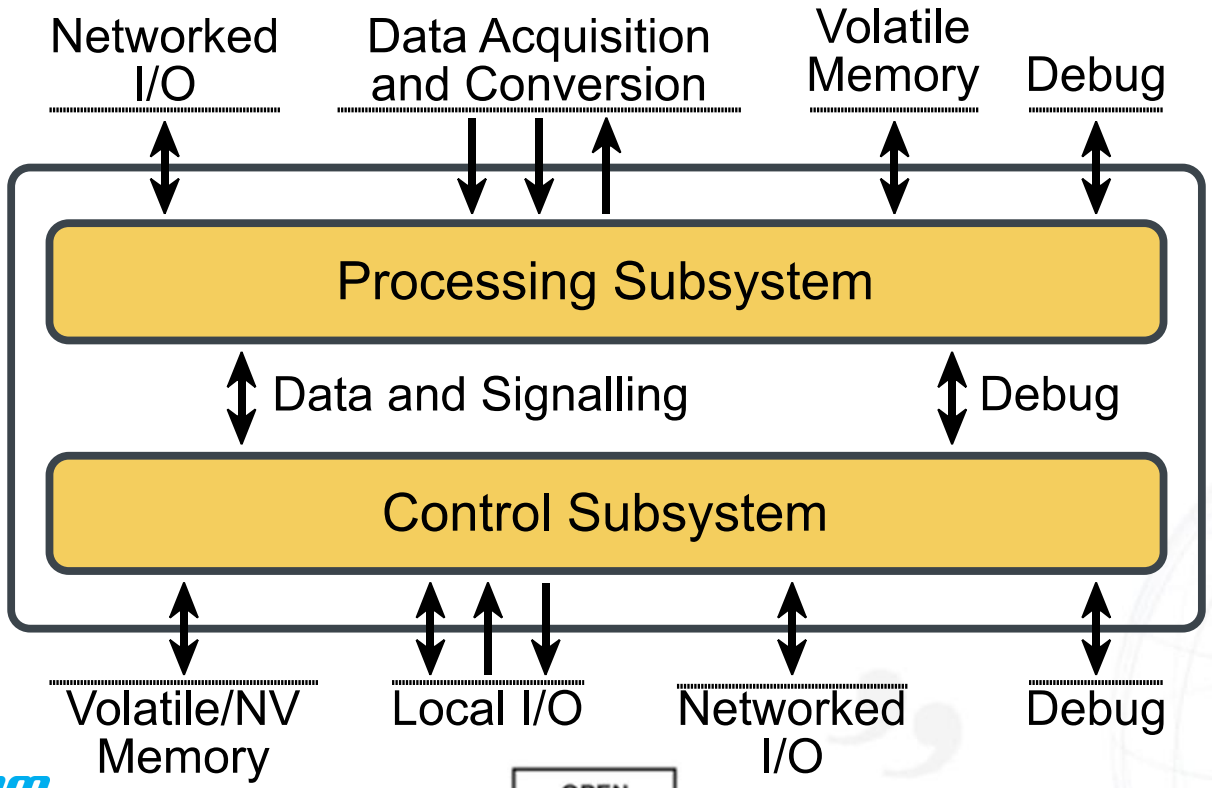
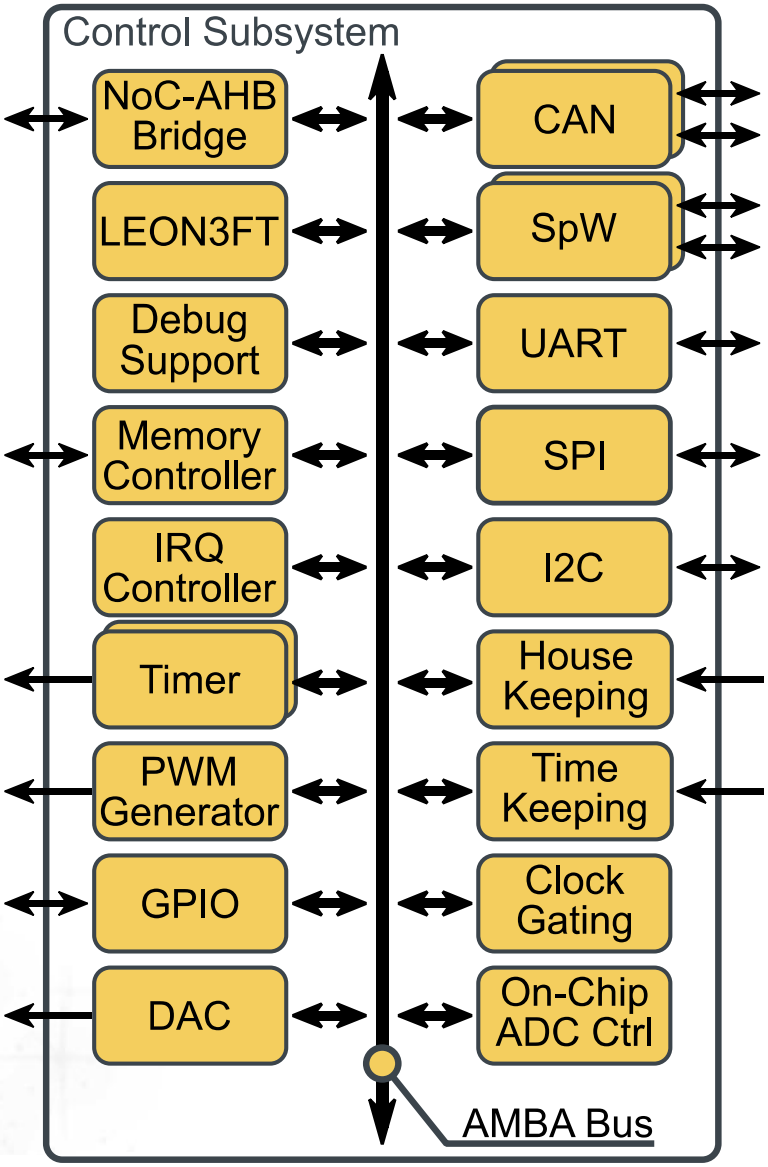
- **Heterogeneous Multicore Mixed-Signal System-on-a-Chip** (SoC) with processing, I/O and DAq in the same package
- Two major Sub-systems capable of exchanging information can be identified, based on the type of processing resource architecture and peripherals: **Processing** and **Control**



# Architecture
## Control Subsystem

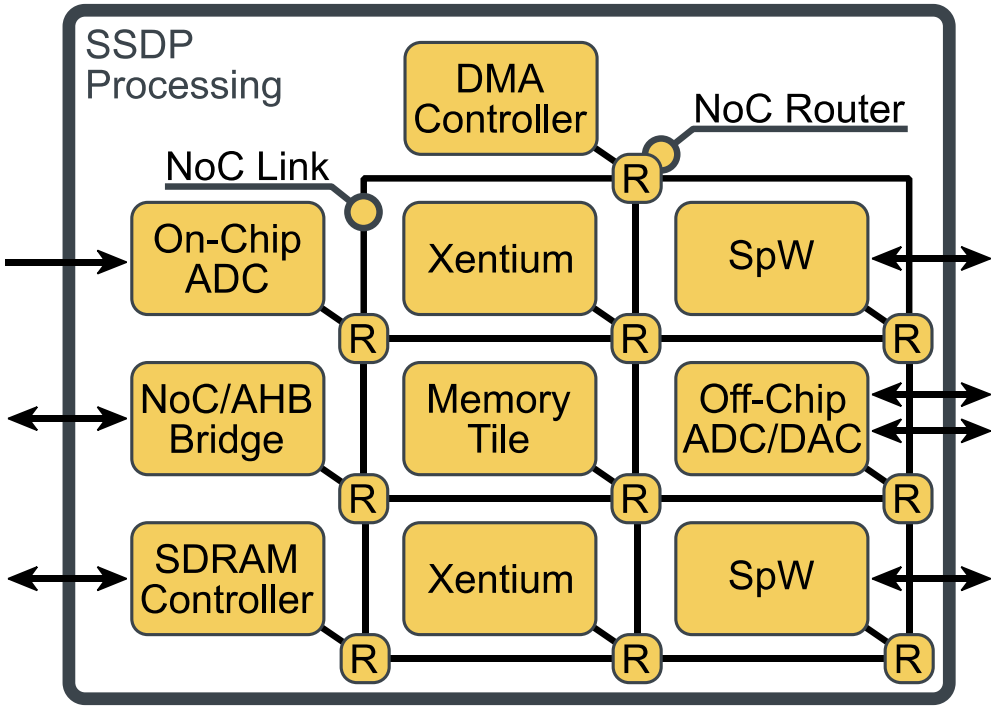





- Cobham Gaisler LEON3FT
  - 16 kB Caches (I$/D$), MMU
  - IEEE-754 High-Performance FPU
- AMBA 2.0 Bus Interconnect
  - 3.2 Gbps throughput @ 100 MHz
  - Many peripherals allow DMA operation, e.g. SpW and CAN
- Memory Controller, supporting EDAC and MRAM technology
- Clock Gating, for power savings, including Processing Subsystem
- Intended to be as compatible with CG GR712RC as possible

# Architecture
## Processing Subsystem (I)

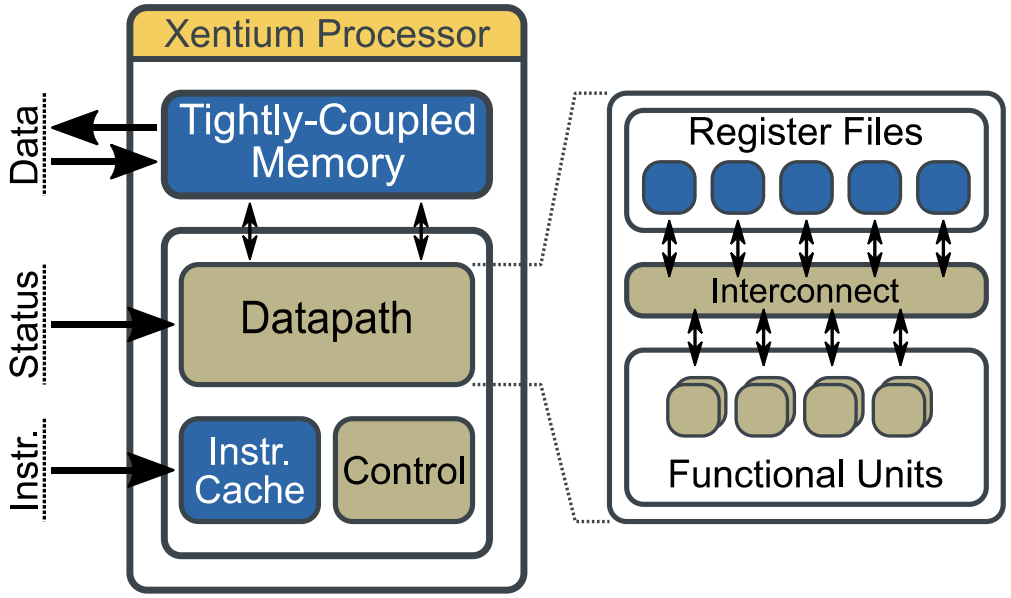





- 2x Recore Xentium Digital Signal Processors
- Network-on-Chip Interconnect
  - Full-duplex 32-bit links, contention-avoidance via routing
  - 3.2 Gbps throughput @ 100 MHz
- Shared 64 kB Memory Tile
- DMA Controller, for autonomous data transfer between modules
- On- and Off-chip Data Acquisition and Conversion

# Architecture
## Processing Subsystem (II)






- Xentium Processor
  - 32-bit Fixed-Point Architecture
  - 32 kB Tightly-Coupled Memory
  - 16 kB Instruction Cache (I$)
- Highly Parallel Data Path
  - 5x Register Files
  - 10x Functional units, partitioned in functions such as load/store, arithmetic, logical, control, etc.
- Throughput (per cycle)
  - 4x Load/Store
  - 4x 16-bit MACs
  - 2x 32-bit MACs



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# Architecture
## Input/Output Interfaces



- Networked I/O
  - 4x SpaceWire with RMAP Target
  - 2x CAN 2.0B
- Local I/O
  - 16x General Purpose I/O (GPIO)
  - 12x PWM, for robotics applications (actuators), heaters, etc.
  - UART, I2C, SPI for local devices
- Analogue I/O (Data Acquisition and Conversion)
  - On-chip Low-Speed ADC and DAC
  - On-chip High-Speed ADC
  - Off-chip ADC and DAC
- Chip-to-Chip Communication

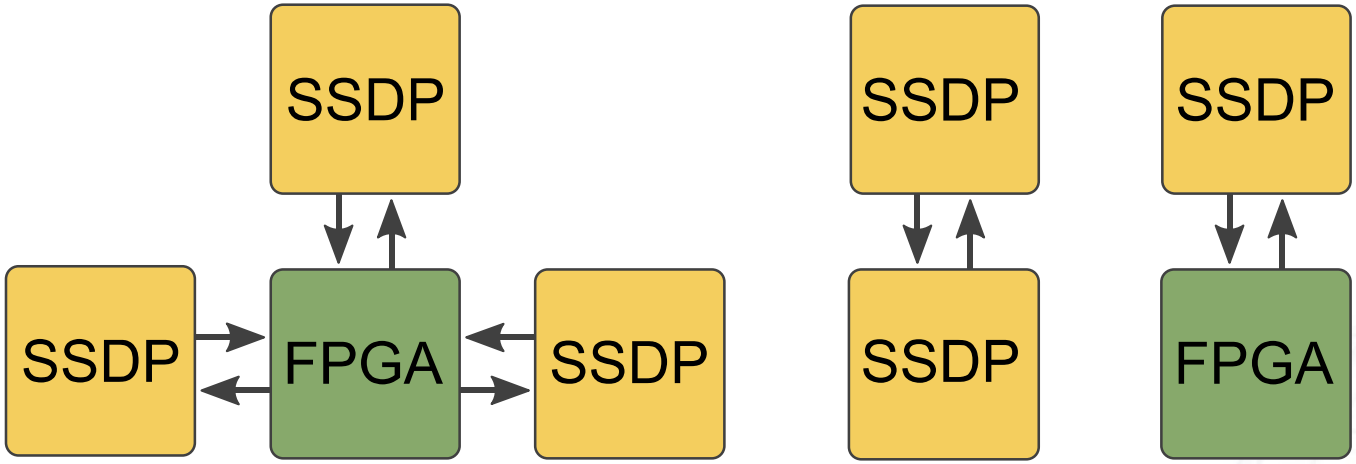
# Architecture
## Data Acquisition and Conversion (I)



- High-Speed On-chip ADC and Off-chip ADC and DAC at the Processing Subsystem
- On-chip High-speed ADC, connected directly to the Processing Subsystem, ENOB 12-bit @ 100 Msps (TBC)
- The SSDP has the capability to interface with external (off-chip) data acquisition and conversion devices (ADC and DAC), allowing direct connection to instruments/sensors
  - ADC and DAC connected directly to the Processing Subsystem
  - 16-bit width, maximum sample rate of 50 Msps
  - Interface in line with the one of qualified components

- Low-speed On-chip ADC and DAC available at the Control Subsystem
- ADC – Voltage
  - 13-bit, ≤ 833 ksps
  - Up to 64 external parameters can be measured via multiplexing, up to 6 internal including temperature and voltage
  - Main use is House-Keeping activities, but fully functional as a “regular” ADC
- DAC – Current
  - 12-bit, ≤ 64 ksps
  - Main use is thermal management, e.g. current reference for thermistors, temperature read back by the house-keeping ADC
  - Can also be used in transducers, diode control, current references, etc.

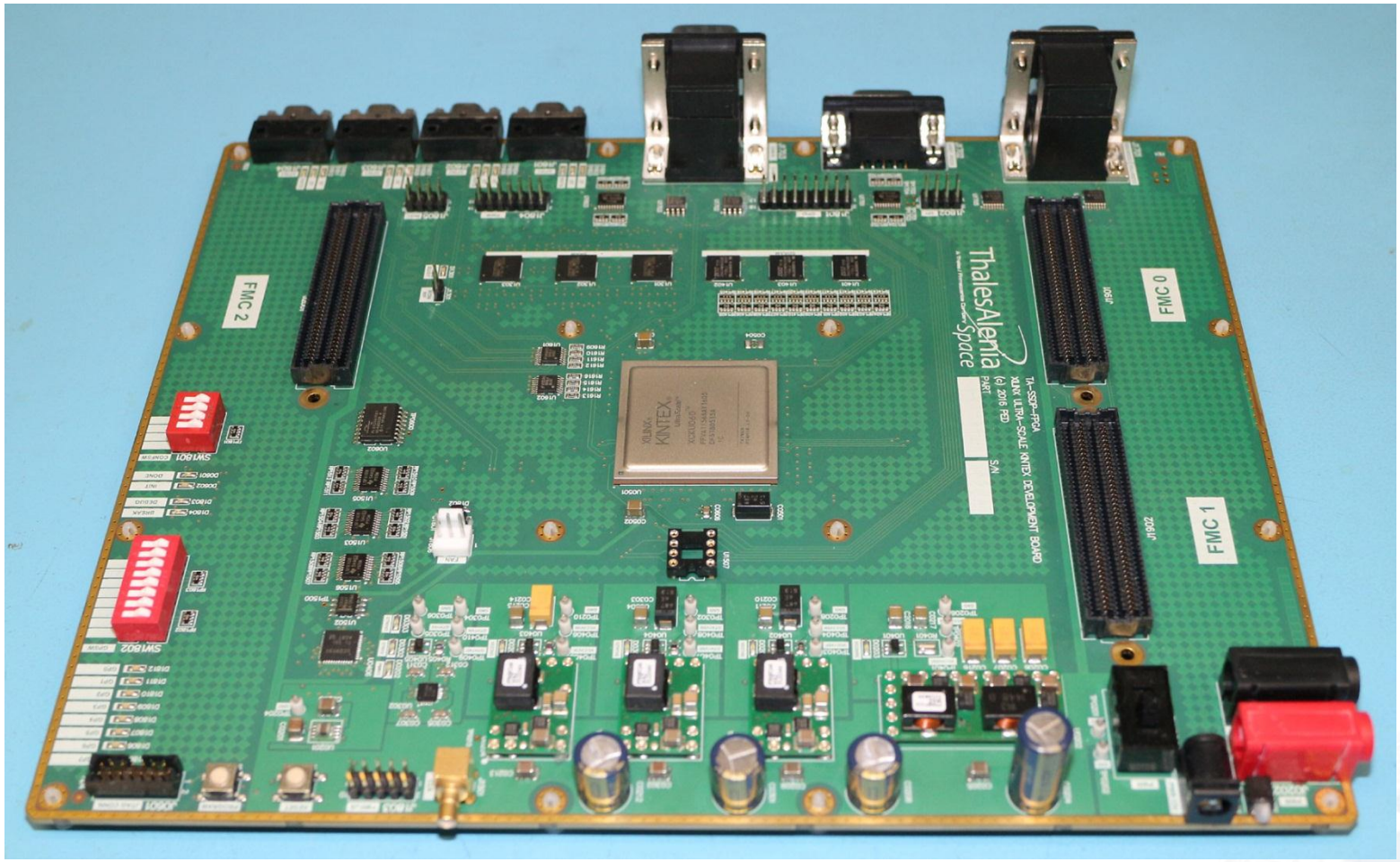
- Off-chip Data Acquisition and Conversion interface can be used as a generic parallel Chip-to-Chip interface, e.g. connecting several SSDPs and/or enabling the connection to FPGAs and other devices
  - 16-bit data path
  - Full-duplex communication with dedicated flow-control signalling
  - 50 MHz clock rate, yielding 800 Mbps throughput each way



- SSDP is being prototyped on an FPGA-based board
  - State-of-the-Art Xilinx Kintex UltraScale XCKU060 FPGA device, with enough resources to hold both Control and Processing subsystems
  - All (digital) I/O interfaces are available at the board level
- Analogue Front-end of Mixed-Signal Data Acquisition and Conversion IPs is being *emulated*
  - ROM which cyclically outputs a digital word, delivered to the digital back-end
  - Test Bench Hardware digital I/O module with FPGA
- Board design and manufacture
  - TAS-E: Defined the Spec. and internally captured the schematic
  - Pender Electronics: Routing, manufacture, assembly and testing

# Prototyping
## SSDP Prototyping Board





# Status
## Overview (I)



- Development is on-going with the integration of subsystems and validation tests at the prototyping platform
  - Network-on-Chip components have been enhanced wrt FDIR
  - Multicore Debugging has also been enhanced

- Preliminary Datasheet available Q2 2016
  - Architecture and Block Diagrams
  - Preliminary Electrical Characteristics, based on the foundry technology and previous ASICs
  - ***Intended to be distributed to interested parties***

- Selected package is CQFP-352, preliminary design activities have begun

# Status
## Overview (II)



- SRR closed, next milestones
  - Reviews
    - PDR – Q3 2016
    - DDR – Q4 2016
    - CDR – Q1 2017
  - Prototype Manufacturing
    - Q2 2017
  - Prototype Electrical, Functional Tests and Validation
    - H2 2017
  - Radiation Testing, Qualification, FM availability
    - 2018

# Concluding Remarks I



- The SSDP offers a unique platform for developing space systems and applications, embedding many functions in the same package
  - High-Performance Processing with multicore DSPs
  - Reliable Control with Fault-Tolerant GPP
  - On- and Off-chip Data Acquisition & Conversion, Low- and High-Speed
- It can embody several different roles
  - Instrument Control, Payload Control and Data Processing
  - Spacecraft/Rover/Lander Control and Processing
- Enables the design and implementation of sophisticated systems, e.g GPP/DSP Algorithm Partitioning/Co-Design

# Concluding Remarks II



- The Processing Subsystem is highly compatible with Cobham Gaisler GR712RC – despite the SSDP having just 1 core. Such similarity enables the porting and/or reusing of code and algorithms developed for GR712RC

- The SSDP provides a few “novelties”…
  - Heterogeneous Multicore Mixed-Signal SoC ASIC for Space
  - Space Network-on-Chip (NoC)
  - Embedded High-Speed Data Acquisition
  - Embedded House-Keeping ADC
  - MRAM Support

# Questions / Comments?