Scalable Sensor Data Processor: Architecture and Development Status

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Abstract

Future science missions are envisaged to be demanding w.r.t. on-board data processing capabilities, due to the scarcity of downlink bandwidth together with the massive amount of data which can be generated by next-generation instruments, both in terms of data rate and volume. Therefore, new architectures for on-board data processing are needed.

The Scalable Sensor Data Processor (SSDP) is a next-generation mixed-signal ASIC aiming at fulfilling the processing needs of such missions, integrating in the same chip a heterogeneous multicore architecture, with two Digital Signal Processing (DSP) cores and a general purpose processor, together with Input/Output interfaces and data acquisition capabilities.

This paper details the current development of the SSDP ASIC, providing an overview of its architecture and highlighting the processing capabilities, together with design enhancements stemming from previous projects. The project status is also documented, both regarding current and future activities and milestones.

I. Introduction

Instruments for future space missions are getting more capable, offering the possibility of acquiring larger sets of data, e.g. higher resolution. However, the on-board data storage and downlink bandwidth are not keeping up with such capabilities, and are regarded as the bottlenecks for the exploitation of the instrument. This constraint is not recent, and many techniques for on-board data processing and reduction have been introduced in order to overcome it, or at least mitigate it: decimation, filtering, down-sampling, compression, among others.

Data processing and reduction algorithms often require specialized hardware, in order to be implemented in an efficient way. Such hardware can be Field-Programmable Gate Arrays (FPGAs) or even Application-Specific Integrated Circuits (ASICs), which have a non-negligible impact both in terms of cost and development time. Furthermore, such processing hardware is usually a companion to control hardware, which is in charge of instrument/payload control, together with local house- and time-keeping tasks, processing and input/output activities.

The Scalable Sensor Data Processor (SSDP) is a next generation on-board data processing mixed-signal ASIC, envisaged to be used in future scientific missions requiring high on-board data processing capabilities, but without neglecting the control functions. It offers a novel heterogeneous multicore architecture, combining two high-performance Xentium Digital Signal Processing (DSP) cores [1] together with a LEON3FT general-purpose processor (GPP) [2], all integrated in a System-on-a-Chip (SoC) design and served by a rich set of Input/Output (I/O) interfaces, including on-chip Analogue-to-Digital Converters (ADCs).

The envisaged domains of applicability of the SSDP are future science and robotic exploration missions like JUICE [3], easing the development and implementation of data processing functions, without neglecting the control capabilities offered by a GPP. The main forces driving its design are *processing power*, *power consumption* and *radiation tolerance*. The focal point of these characteristics lies between flexibility and scalability, enabling the usage of the SSDP in missions with profiles so diverse as deep-space missions or planetary landers.

The SSDP builds on the experience and expertise gathered through the successful Massively Parallel Processor Breadboard (MPPB) project [4] commissioned by ESA, which aimed at developing a demonstrator of a (scalable) heterogeneous multicore DSP platform for Space applications. The mapping into ASIC technology will be performed with DARE180 digital cells. Development is sustained by a consortium led by Thales Alenia Space España, and comprising Recore Systems, IMEC, Cobham Gaisler and Arquimea, bringing together expertise in the digital, analogue and mixed-signal domains. Such diverse expertise is of the utmost importance in order to tackle the technical challenges posed by integrating the many different components, yet achieving the proposed goals.

This paper is organized in the following manner: Section II provides some on-board processing use-cases envisaged for future Space applications, Section III provides an overview on the SSDP Architecture, namely its subsystems and I/O interfaces; Section IV details the processing capabilities of the SSDP, including architectural enhancements introduced; Section V presents the current project status and timeline for the following stages and milestones, and finally Section VI concludes this paper.

II. Future SRE Data Processing Needs

Future data processing needs of Science and Robotic Exploration (SRE) missions can be divided in two major domains: *on-board data reduction*; *robotics processing and control*. Each domain has its own specificities regarding processing needs, briefly presented in this section. Nevertheless, there is a common denominator in both domains: *processing power*, in order to execute sophisticated algorithms.

A. On-board Data Reduction

Next-generation instruments are capable of generating a massive amount of data, which can be orders of magnitude higher than the available down-link. A first form of data reduction can be achieved by performing digital signal processing on the captured samples, with (simple) functions like filtering and down-sampling. Nevertheless, more sophisticated functions which are currently performed at ground segment level can be performed directly on-board.

Another form of on-board data reduction can be achieved by performing *compression* on the data. Several standards exist, both for general data and images, and typically resort to transforms and other algorithms which are suitable to be implemented by DSPs.

B. Robotics Processing and Control

Robotics is a vast yet growing domain, with several different disciplines like computer science, algorithms and mechanics. Current robotics-based missions are highlighting the need for not only powerful processing capabilities, but also appropriate I/O interfaces for precise control, including exploitation of sensors and actuators.

1) Image Processing

A typical application in robotics is *image and vision processing*, which requires a fair amount of processing power. Such processing is used by the robotics application to identify its surroundings, and then be able to take a decision regarding its future state based on what it finds.

An illustrative example is path-decision algorithms of a rover, which requires identifying potential routes – and hazards – before moving. Such class of algorithms is processing-intensive due to the amount of data and steps needed to take a decision. Moreover, they can be *time and energy consuming* if the appropriate processing architecture is not used.

2) Actuator and Drive Control

Another robotics application deals with the control of actuators, e.g. motors. This kind of applications usually involves a feedback control loop: gathering information from sensors, input it into a control algorithm e.g. PID[1], and then use the output to control actuators, like wheel motors or steering. Such application requires not only processing power – in fact the requirements for control are usually modest, with loops below the kHz range - but also a set of special-purpose input/output interfaces, like general-purpose pins, low-speed ADCs and pulse-width modulated (PWM) outputs.

[1] **P**roportional, **I**ntegral, **D**erivative

III. SSDP Architecture

Most systems nowadays follow the System-on-a-Chip (SoC) paradigm, embedding in the same package processing resources together with Input/Output (I/O) interfaces. The SSDP is not an exception, aiming at providing in a single chip all the resources needed to perform a wide range of tasks pertaining to on-board data processing.

The SSDP architecture can be divided in two major subsystems, based on their main scope:

- *Control*, with a General-Purpose Processor (GPP) at its heart, providing general control tasks including Fault Detection, Isolation and Recovery (FDIR) functions;
- *Processing*, with two Digital Signal Processors (DSPs) providing the raw processing power together with high-speed I/O.

A top-level block diagram depicting the two subsystems and their interconnection is shown in Figure 1.

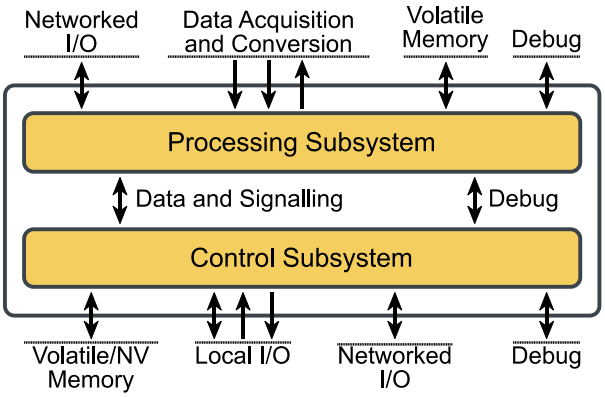


Figure 1: SSDP High-level Block Diagram

Each subsystem has its own internal SoC bus: AMBA for Control, a Network-on-a-Chip (NoC) for Processing. The subsystems are interconnected via a special-purpose Bridge interface, allowing them to exchange information such as data and signalling (interrupts and errors). Reception of signalling information from the Processing subsystem permits the effective implementation on the Control subsystem of FDIR handling mechanisms.

The two subsystems have a set of local and networked I/O interfaces: Controller Area Network (CAN), SpaceWire (SpW) with RMAP target support, Serial Peripheral Interface (SPI), Pulse-Width Modulator (PWM), among others, which gives a high degree of flexibility w.r.t. applications. Dynamic power saving was not neglected, and a clock gating is used to turn-off major IP cores when not in use, enabling significant power savings.

Besides the diverse I/O interface set, the SSDP is also capable of performing both on- and off-chip data acquisition and conversion, using Analogue-to-Digital (ADCs), and Digital-to-Analogue (DAC) converters. On-chip ADCs provide both high- and low-speed capabilities, allowing a wide spectrum of applications ranging from high-speed sensor data acquisition to low-rate house-keeping activities.

A. Control Subsystem

At the heart of the Control Subsystem there is a SoC based on the flight-proven Cobham Gaisler LEON3FT, a fault-tolerant SPARC V8 architecture. The SoC modules are interconnected via a shared 32-bit ARM AMBA 2.0 bus, yielding a maximum throughput of 3.2 Gbps. A block diagram depicting the Control Subsystem and its components is shown in Figure 2, with the remaining SoC components, also from the Cobham Gaisler GRLIB.

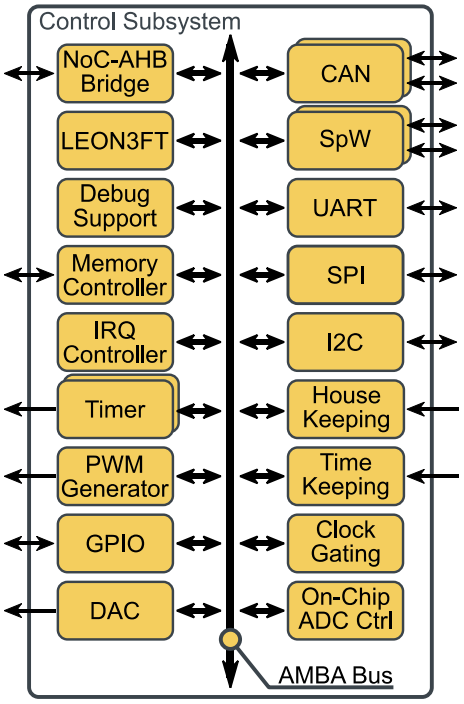


Figure 2: SSDP Control Subsystem Block Diagram

The following Sections detail some of the features of the Control Subsystem depicted in Figure 2.

1) Input/Output Interfaces

The Control Subsystem has a rich set of I/O interfaces, both local and networked, allowing it to interact with and/or control both local and remote devices/systems. Such interfaces range from SpW and CAN to local device control with SPI or I2C.

There are interfaces dedicated to directly interface with actuators, such as Pulse-Width Modulation (PWM) outputs. The provision of such functions in hardware paves the way to fine-grained control of actuators, such as brushless motors.

Analogue I/O interfaces also exist, such as an on-chip low-speed current DAC. The purpose of such device is to be able to measure external temperature via a thermistor such as a platinum probe (Pt1000). This interface is complemented by a low-speed voltage ADC, intended primarily to be used in house-keeping activities, but also capable of being used in other applications.

2) Memory Support

The storage and execution of software applications is supported by a Fault-Tolerant Memory Controller supporting both non-volatile (mature PROM, EEPROM and novel MRAM) and volatile (SRAM) memory technologies. Furthermore, these can be protected by Error Detection and Correction (EDAC) mechanisms in order to ensure reliable operation in the harsh space environment. These are further aided by dedicated and autonomous memory scrubbing hardware mechanisms (not shown in Figure 2).

3) House-keeping and Time-keeping & distribution

As previously mentioned, house-keeping data can be acquired with the on-chip low-speed ADC. The device is capable of measuring several parameters, either internal to the ASIC or external, e.g. internal supply voltage or temperature.

Time-keeping services are also provided, and complemented by (Spacecraft/Instrument) time distribution is managed by the novel SpaceWire Time Distribution Protocol (SpW-TDP) [5], whose IP core has been enhanced with time-keeping and management functions. Besides the presence of SpW-TDP, local time distribution and synchronization is also possible via dedicated input pins, e.g. Pulse Per Second (PPS).

4) Operating System and Debug Support

Operating system (OS) support is provided, via timer units, interrupt controller and even a Memory Management Unit (MMU). Such components allow running both Real-Time Operating Systems (RTOS) like RTEMS, or modern generic operating systems like Linux.

A Debug Support Unit is provided for on-ground application development, using standard Cobham Gaisler tools, together with profiling mechanisms.

5) Advanced Features

Although the LEON3FT GPP is envisaged to be mostly in charge of SSDP control activities, its processing features were not neglected, being endowed with advanced features such as:

- High-performance IEEE-754 compliant Double Precision Floating Point Unit (FPU);
- Separate 4-way set-associative 16 kB Data and Instruction cache memories.

Furthermore, it is possible to lock lines of instruction cache, allowing to speed-up the execution of some portions of code by reducing latency, e.g. fast interrupt-handling routines.

6) Summary

The Control Subsystem offers many resources which enable its exploitation as a fully capable On-Board Computer (OBC) component, without neglecting processing tasks:

- Networked I/O: CAN, SpW
- Local I/O : GPIO, SPI, I2C, among others
- EDAC-protected Memory Storage
- Timer Units, IRQ Controller, MMU
- House-keeping, Time-keeping and distribution
- FPU and Cache Memories

The architecture of the Control Subsystem is intended to be highly compatible with the commercially available GR712RC GPP from Cobham Gaisler [6], which is also based on the LEON3FT. The objective of such compatibility is to allow the reuse in the SSDP of code, tools and procedures already developed for the GR712RC and its applications.

B. *Processing Subsystem*

The Processing Subsystem is powered by a multicore SoC based on the novel Recore Systems' Xentium Processor [1], a VLIW[2] fixed-point DSP architecture. The DSPs are connected to the remaining SoC components via a high-performance Network-on-a-Chip (NoC) interconnect. The SSDP Processing Subsystem is depicted in Figure 3 through a block diagram, showing how the SoC components are connected via the NoC.

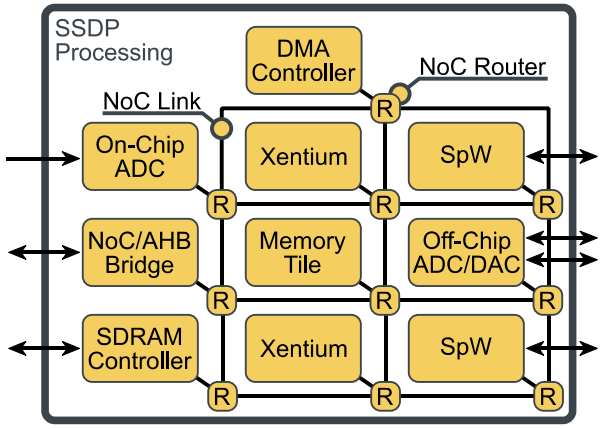


Figure 3: SSDP Processing Subsystem Block Diagram

SoC elements are connected via Network Interfaces (NI) to NoC routers with 32-bit full-duplex links, yielding a maximum throughput of 3.2 Gbps each way. Each router has five ports: one for the NI, and four to connect to other adjacent routers (*see* Figure 3). The following sections detail the characteristics of the SoC components.

1) Xentium Processor

The Xentium Processor is a 32-bit fixed-point high-performance parallel Processing Element (PE) capable of executing multiple instructions on multiple data (MIMD). The Xentium Processor is depicted in Figure 4, showing its main components: *Tightly Coupled memory (TCM)*, providing a high-bandwidth connection to the NoC for data input/output; *Datapath*, with the computing resources used for processing; *Instruction Cache* for speeding-up the execution of application program code..

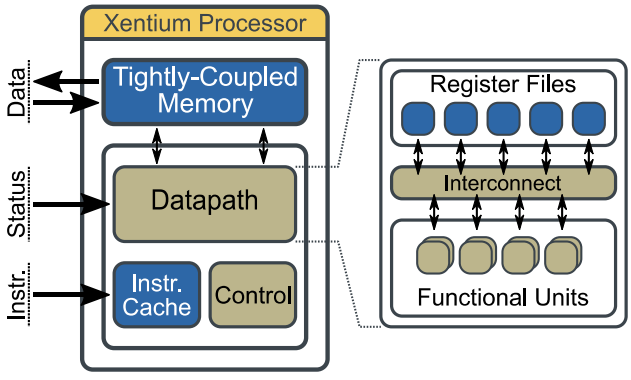


Figure 4: Xentium Processor

The Datapath is composed by *functional units* (FUs), providing the data computing resources, and *register files* (RFs), providing temporary data storage. There are ten FUs, which are grouped based on the different operations they can perform: arithmetic, logical, multiplication and load/store. Execution can be controlled through external status signals, e.g. synchronization (wait on bit).

There are five RFs, each with two read and write ports each, allowing two simultaneous operations. Datapath data input and output is managed by the load/store FUs, which are connected via 64-bit ports to the Tightly-Coupled Memory (TCM), running at system speed and organized in four independent banks, thus allowing the programmer to design the application in order to avoid FU contention upon memory access.

The Xentium Processor is capable of performing the following operations per clock cycle:

- 4x 16-bit Multiply-Accumulate Operations (MACs)
- 2x 16-bit Complex MACs
- 2x 32-bit MACs
- 2x 64-bit load/store operations

2) Input/Output and Data Acquisition

I/O interfacing was not neglected on this subsystem, despite having as main scope the processing of massive amounts of data. Two SpW interfaces with RMAP target are available to be used directly by the Xentium Processors. These interfaces are capable of exchanging data with a data rate up to 200 Mbps.

Data acquisition and conversion is also a feature of the Processing Subsystem, with both on- and off-chip acquisition (ADCs). On-chip acquisition is envisaged to be capable of acquiring 16-bit samples at 100 Mega-samples per second, (re)using an ADC design developed under previous ESA contracts. Off-chip acquisition has been designed to interface with already existing radiation-hardened ADCs. The sample rate of this interface allows up to 50 Mega-samples per second acquisitions, with a sample width up to 16-bit.

3) Memory Hierarchy

Efficient exploitation of memory hierarchy is the crux of effective processing algorithms' implementations, often the application's bottleneck resides in the rate at which data can be put and retrieved to/from the processing element or system. The SSDP has a full-fledged memory hierarchy in place, listed here from high latency to low latency:

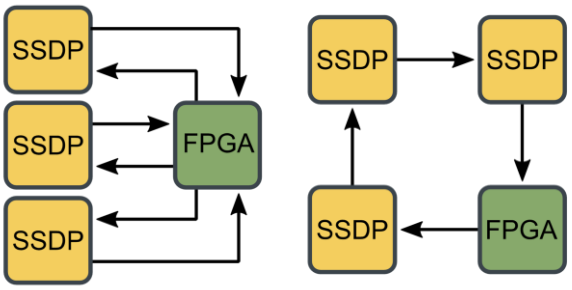
- High capacity SDRAM Memory, up to 512 MB
- Internal low-latency 64 kB SRAM Memory Tile
- Local TCMs, 32 kB per Xentium Processor

The Memory Tile provides a large SRAM accessible via the NoC at full system speed, which can be used to store large chunks of data which will then be transferred either to the TCMs, SDRAM or any available I/O interface. This allows the implementation of a *software-based cache memory*. Memory addressing is performed in little-endian, i.e. the least significant byte is stored in the lowest address.

[2] **V**ery-**L**arge **I**nstruction **W**ord

4) System Scaling

The scaling of SSDP-based systems has been envisaged, and with that purpose a Chip-to-Chip (CtC) interface has been introduced. This full-duplex parallel interface has a 16-bit width, and is capable of exchanging data at a speed up to 50 MWords per second, yielding a maximum throughput of 800 Mbps. The interface has hardware-based flow-control mechanisms, thus enabling reliable communication support. The CtC interface allows data exchange between one or more SSDP devices, or the exploitation of companion devices, including functions supported by FPGAs (*see* Figure 5).



(a) Star/Single (b) Ring

Figure 5: Chip-to-Chip Interface Usage Examples

The bi-directional interconnection of the SSDP with a companion FPGA is depicted in Figure 5a, in a *star* topology: the FPGA is at the centre, and can be used with a specific purpose (companion device), and/or be used to route data between the SSDP devices. A single-device topology would be a star with a single SSDP. Another topology is shown in Figure 5b, where the devices are connected in a *ring* topology. These topologies enable a powerful processing chain, with each device being in charge of a given task, or subset of tasks, or even being connected to multiple different instruments/acquisition devices.

5) Summary

The Processing Subsystem provides a high-performance multicore DSP SoC, with data acquisition capabilities. Its most striking features are:

- Multicore 32-bit fixed-point VLIW DSP (x2)
- Internal 64 kB SRAM, external SDRAM
- SpW I/F with RMAP target, up to 200 Mbps (2x)
- On-chip ADC up to 100 Msps
- Off-chip ADC and DAC up to 50 Msps
- Chip-to-Chip Interface, up to 800 Mbps

These features can be efficiently exploited by application designers through compilers and a graphical Software Development Environment, with debugging capabilities.

IV. SSDP Advanced Features

The SSDP draws heavily from the MPPB platform, inheriting most of its architecture and components. Building on this heritage, improvements and features were introduced, based on MPPB usage and evaluation activities performed both by industry and academia. This section details some of the advanced features, and how they can enable the design and implementation of sophisticated systems and algorithms.

A. Efficient DMA Transfers

The availability of DMA transfers allows the exchange of data autonomously, without needing processor intervention. The SSDP Processing Subsystem provides a DMA Controller which is capable of performing *stride-based* transfers, where data which is not stored in contiguous positions can still be efficiently accessed without paying a severe penalty. The same feature can be used for sub-sampling / decimation without consuming processor/DSP resources.

The availability of DMA transfers (both 2D and stride-based) enables creative – and efficient - uses of the memory hierarchy. An example is implementing an effective *software-based cache*, with the DMA controller being used to transfer data between the SDRAM, Memory Tile and TCMs, for ensuring that the Xentium processors would always be working on data, i.e. they would not suffer data starvation.

B. Endianness Conversion

Memory accesses performed by most of Processing Subsystem modules are done in little endian, i.e. the least-significant byte is stored at the lowest memory address. Such access fashion clashes with the one used by the Control Subsystem, whose modules inherit the big-endian addressing from the LEON3FT architecture.

The issue of endianness conversion is addressed on the SSDP at the points where information has to cross a so-called "endianness domain crossing", i.e the bridges between the two subsystems. At these points there are specially crafted mechanisms to provide automatic and transparent conversion. Transparency is achieved by having different memory maps for big- and little-endian information exchange, which will determine if there should be a conversion or not.

C. Application Profiling

Profiling an application is the logical step to be taken after its (initial) implementation and validation, and it should be performed before attempting to introduce any optimization. The Xentium Processors have been enhanced w.r.t. profiling support, with new performance monitoring mechanisms added. A new set of counters is provided, which can be used to assess the performance of an application in a non-intrusive manner: read and write cycles, latency, cache misses and hits, among others.

D. Fault Detection, Isolation and Recoveryl

Space-based applications must provide FDIR functions in order to be able to cope with errors induced by the harshness of the Space environment. Such function must be built on top of hardware-based mechanisms, providing the capability of detecting errors, which may trigger faults.

In the SSDP the Control Subsystem is in charge of dealing with FDIR functions. In order to provide effective FDIR, the NoC and modules of the Processing Subsystem have been enhanced w.r.t. error detection and signalling capabilities. Such capabilities allow the hardware based detection of errors. Error notifications are forwarded to the Control Subsystem in order to trigger the execution of appropriate handlers.

V. Development & Status

The SSDP is being developed through an industrial consortium led by **Thales Alenia Space España** (ES), and encompassing several partners across Europe with different domains of expertise:

- **Recore Systems** (NL), providing the multicore DSP and components of the Processing Subsystem, together with the Software Development Environment (SDE) and support;
- **Cobham Gaisler** (SE), with the LEON3FT SoC and support
- **IMEC** (BE), providing specific IP cores, DARE180 cell library, and also the layout services, package, assembly support, foundry interface and manufacture testing;
- **Arquimea** (ES), with the on-chip fast ADC.

The SSDP is now at its development and validation stage, including FPGA-based prototyping. The SSDP development will result in a CQFP-352 mixed-signal ASIC, built in UMC 180 nm technology with DARE180 digital cell technology [6]. Engineering Models (EMs), Flight Models (FMs) and evaluation boards will be commercialized by Cobham Gaisler.

A. Prototyping, Testing and Validation

The prototyping and testing activities are being carried out on a custom board based on a Xilinx Kintex Ultrascale FPGA, providing enough resources to accommodate both SSDP subsystems. The schematic was captured internally at TAS-E, and the manufacture commissioned to Pender Electronics. This board will provide all the I/O interfaces needed by the SSDP, thus allowing their validation.

The SSDP testing and validation activities are being carried out with support of a National Instruments PXI testbench comprising both hardware and LabView software. The SSDP runs small pieces of software to support the validation procedures. Such a setup allows a simple yet powerful validation loop, which can be used at all levels of the validation procedures, from interfaces to full system.

Benchmarking will be performed throughout the development cycle, in order to characterize the SSDP from a processing point of view. For that purpose, the NGDSP benchmark suite [8] will be used.

B. Development Milestones

The SRR was successfully closed out in October 2015, and the current activities related to development and subsystem integration will culminate with a PDR in 2016. The current schedule for the following (major) milestones is the following:

- Q1 2017 – CDR
- Q2 2017 – Prototypes Manufacturing
- Q3/Q4 2017 – Prototypes (EM) Available
- 2018 – FM Available

Evaluation boards with EMs are expected also during Q3/Q4 2017, after the testing and validation campaign.

VI. Conclusions

The Scalable Sensor Data Processor (SSDP) is a next-generation data processing mixed-signal ASIC, providing in a single package a sophisticated architecture with a Processing Subsystem with powerful multicore DSP processing capabilities, together will a Control Subsystem using well-established general-purpose processing resources capable of delivering fast and reliable control and house-keeping. Each of these is a full System-on-a-Chip (SoC) on its own, with Input/Output capabilities besides the processing resources.

The Control Subsystem offers a general-purpose LEON3FT with a floating-point unit, together with SpaceWire, CAN and local I/O such as SPI and I2C, being highly compliant with the LEON3FT-based Cobham Gaisler GR712RC SoC, thus allowing the porting to the SSDP of applications developed for such platform.

Besides the powerful Xentium Processors, the Processing Subsystem is supported by a high-performance Network-on-Chip (NoC), interconnecting the processing resources, SDRAM storage, I/O such as SpW and on- and off-chip data acquisition for ADCs and DACs. A Chip-to-Chip interface is also provided, allowing scaling a system with other devices, such as additional SSDP ASICs, FPGAs or others.

The SSDP RTL is currently being integrated, tested and validated, supported by a custom FPGA-based prototyping board. The next step after validation will be to perform the ASIC layout. The SSDP ASIC will be implemented in UMC 180 nm technology, using DARE180 digital cells, providing a high degree of SEE tolerance which is in line with envisaged future science and robotic exploration missions. The first prototypes for testing and validation are expected to be delivered during the second half of 2017, with evaluation boards being made available by Cobham Gaisler.

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