



Radiation Prediction Tool Dedicated to Analyze and Harden by Design Readout Circuits of Photonic ICs

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retour sur innovation

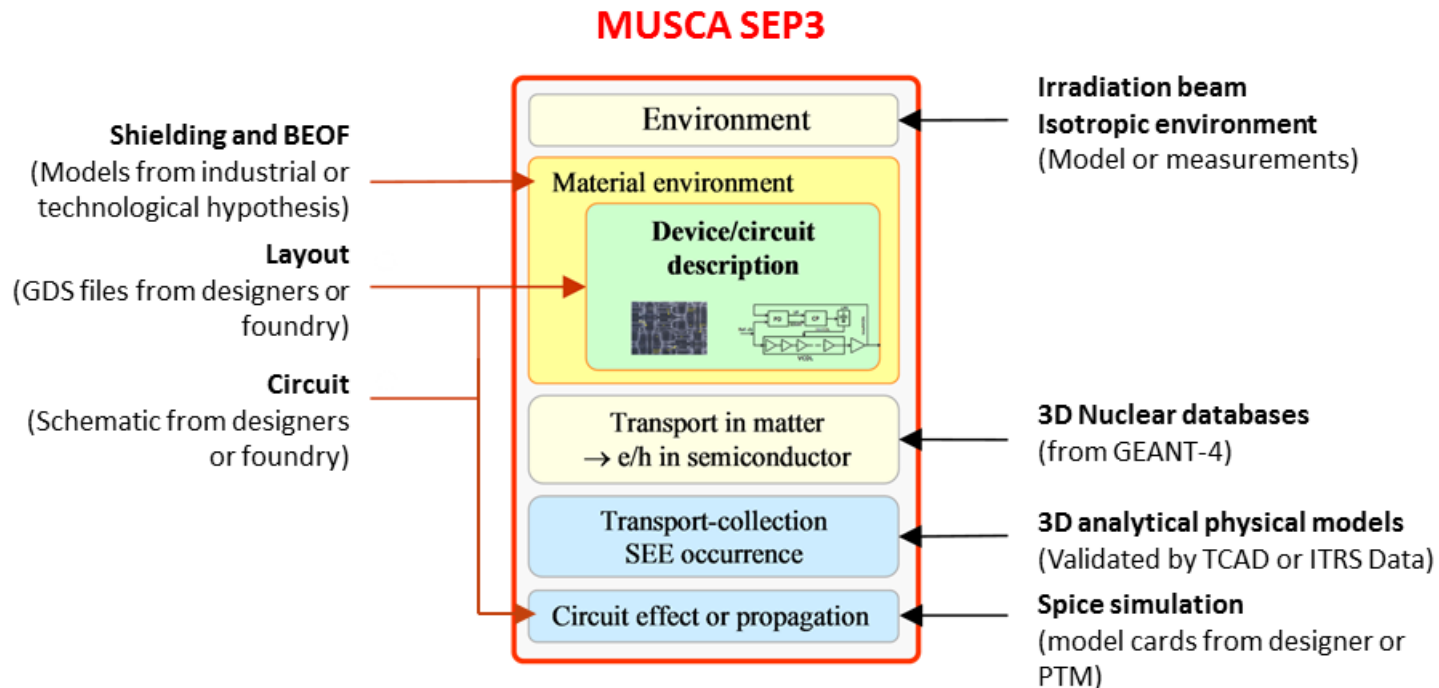


- CMOS technology is relevant for integrate electronic functions in image sensors (raw decoders, registers, Flip-Flops)
- The SEEs (SEU and SET) sensitivity of CMOS technology increases with technological roadmaps for analog and digital circuits
- High temperatures rise the soft error duration and the SEU occurrence
- For performance reasons, infrared image sensors developed by Sofradir works at very low temperatures down to 77°K

→ What are the SEU sensitivity trends of Flip-Flops used in the read-out circuit at ambient temperature and down to 77°K under heavy ions?

→ Prediction tool relevant to propose a hardened design for Flip-Flop cell used in the read-out circuit of Photonic IC ?

- MUSCA SEP3 is a Monte-Carlo prediction tool based on a multi-physics and multi-scales approach developed at ONERA dedicated for researches, space agencies, and industrials



- Outputs: SEE (SET, **SEU**, SEL) estimations of **cross section**, operational rate, **hardened design**

- Modeling of the circuit at layout and schematics level
 - Design extraction from GDS and circuit modeling
- Estimation of SEU sensitivity of Flip-Flops in 0.25 μ m technology
 - Validation of SEU cross section estimations
 - Estimation of temperature impact on the SEU cross section
 - Failure analyses of Flip-Flops by sensitivity maps modeling
- Hardening by design of DFF cell based on prediction tool
 - Presentation of the new hardened design of the DFF cell
 - Evaluation of the hardening technique
- Conclusions and outlooks for analog and mixed-signal applications

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- Test chip developed by Sofradir called SEU2_01A
 - 6 references of Flip-Flop cells designs

Analyzed
designs

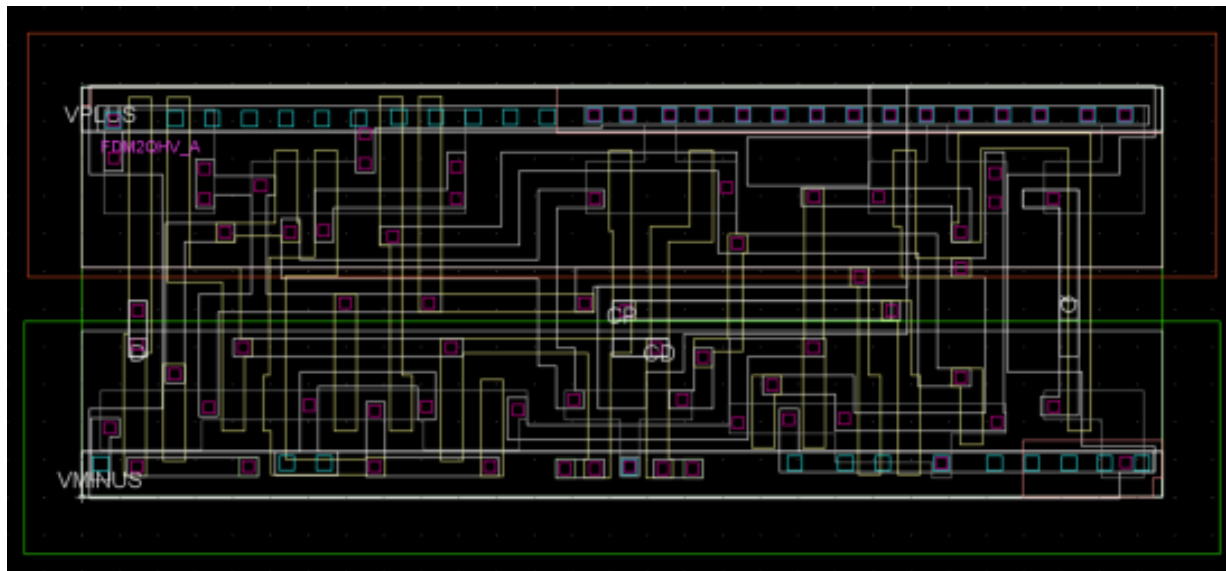


Reference	Cell area (normalized)	Width (normalized)	High (normalized)	Techno. Node (μm)
SEU_01A				
Design 1	1,03	1,03	1	0,25
Design 2	1	1	1	0,25
Design 3	1,1	1,1	1	0,25
Design 4	1,07	1,07	1	0,25
Design 5	1,2	1,2	1	0,25
Design 6	1,17	1,17	1	0,25



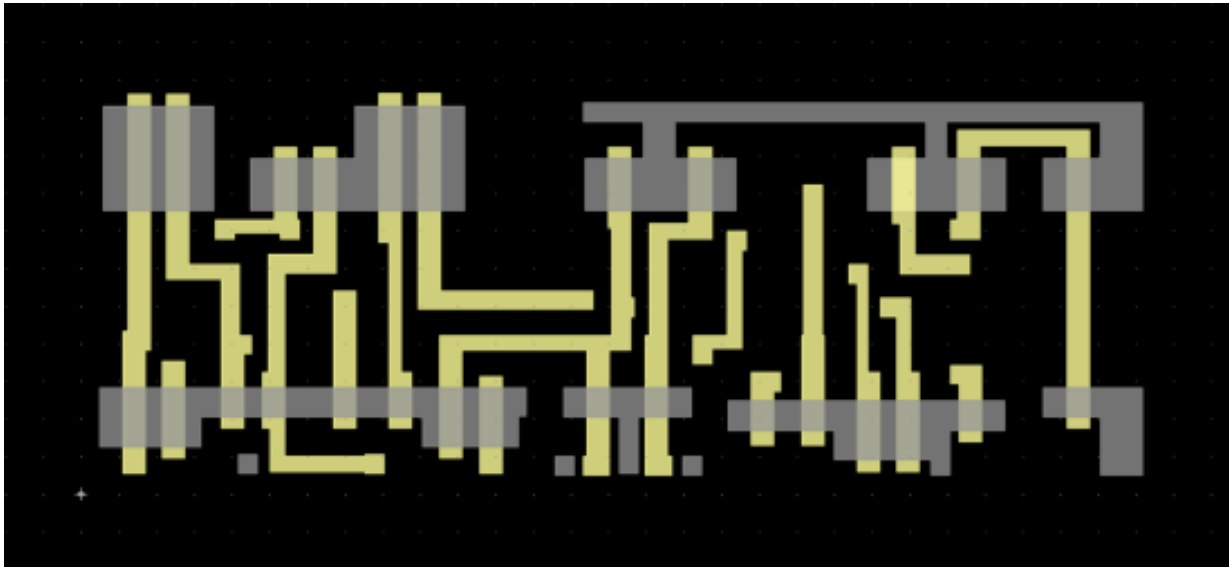
2 Designs are investigated for their criticality in the read-out circuit used by Sofradir in their infrared image sensors

- Modeling of the Flip-Flop circuit at layout level
 - Design extraction from GDS and circuitry development
 - Extraction of collection areas from Sofradir's GDS file
 - Circuit development with Cadence software suite based on the netlist



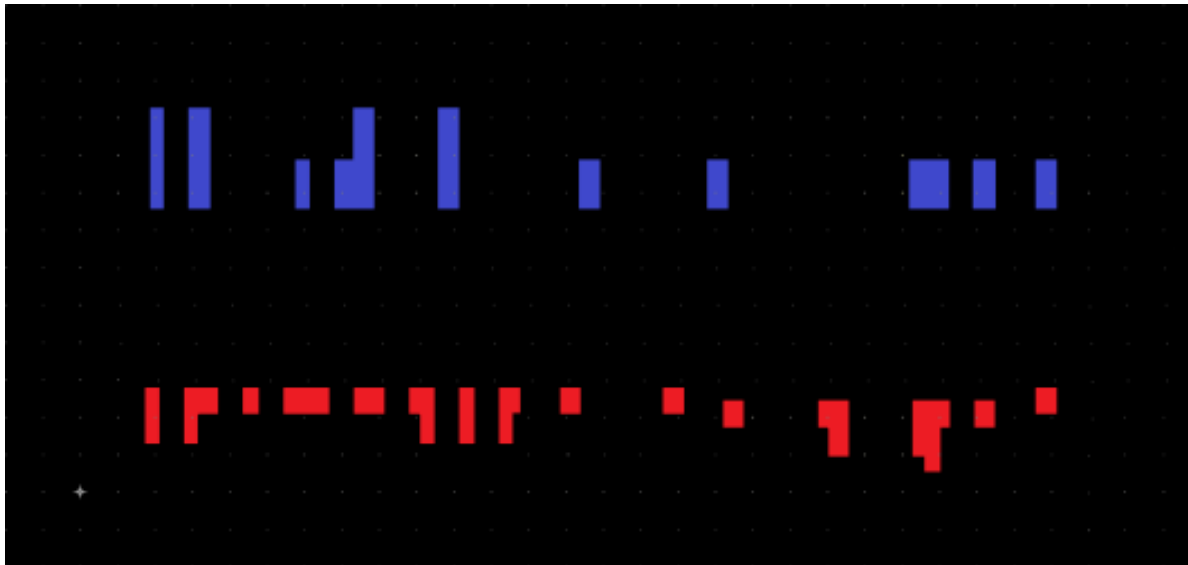
GDS file from Sofradir

- Modeling of the Flip-Flop circuit at layout level
 - Design extraction from GDS and circuitry development
 - Extraction of collection areas from Sofradir's GDS file
 - Selection of relevant BEOL layers (polysilicon and active implants)



GDS file reworked

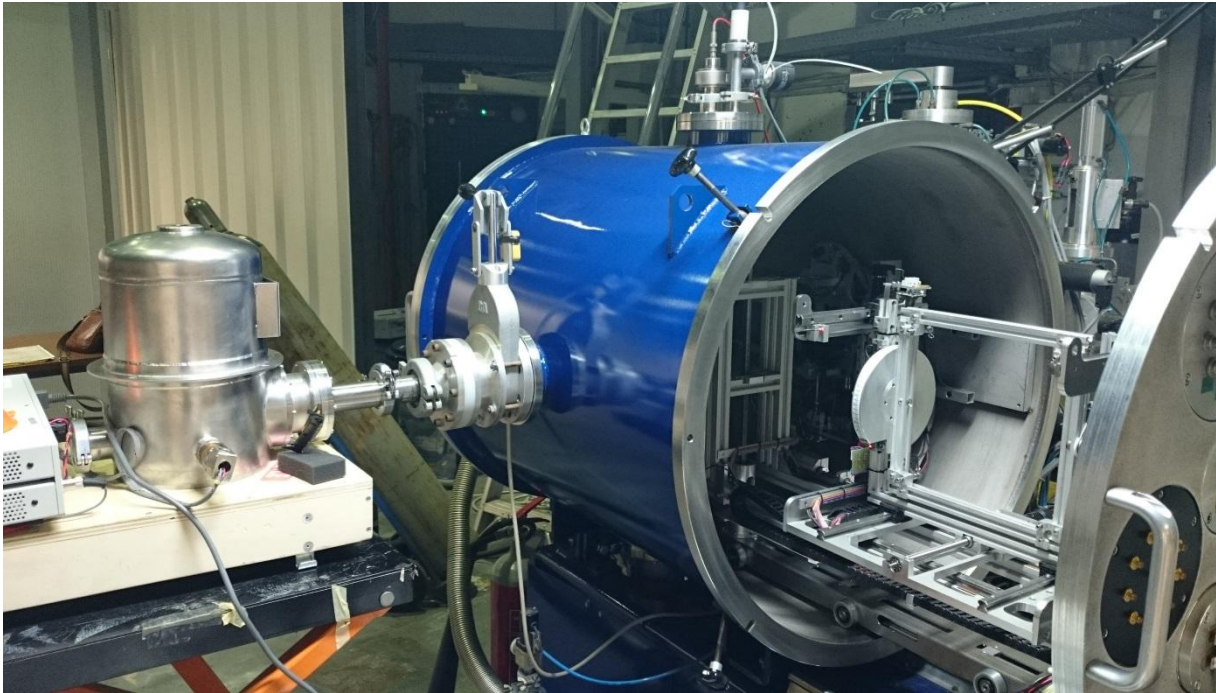
- Modeling of the Flip-Flop circuit at layout level
 - Design extraction from GDS and circuitry development
 - Extraction of collection areas from Sofradir's GDS file
 - Determination of collection area: drains of p-MOS and n-MOS transistors of floating nodes



Extracted Design file

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- Experimental heavy ion irradiations for SEU measurements performed at UCL (Belgium) with CNES cryostat (in June 2014 and May 2015)



Temperature monitoring
and regulation from 300°K
to 80°K

Heavy ion irradiation from
 $6.6\text{MeV.cm}^2.\text{mg}^{-1}$ to
 $67.7\text{MeV.cm}^2.\text{mg}^{-1}$

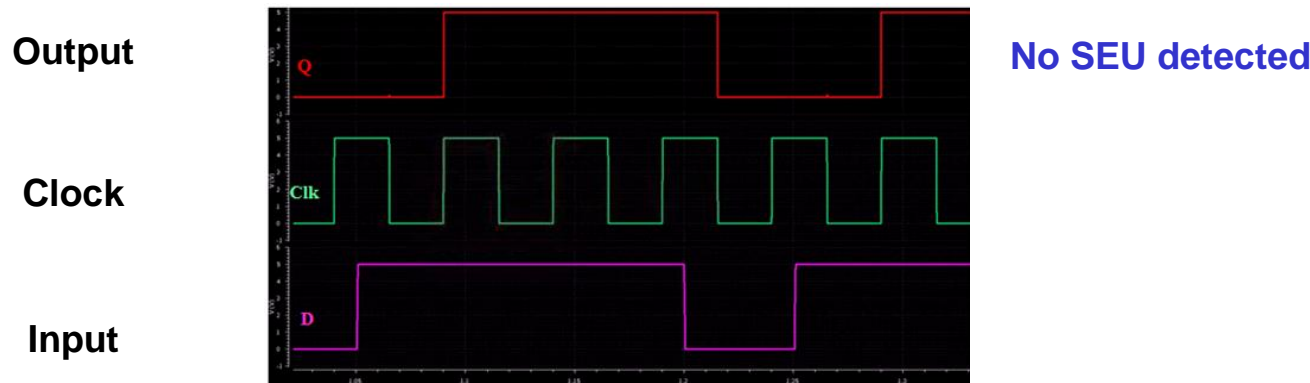


Dynamic SEU testing with TRAD test board using CNES cryostat under heavy ions beam at UCL, Belgium

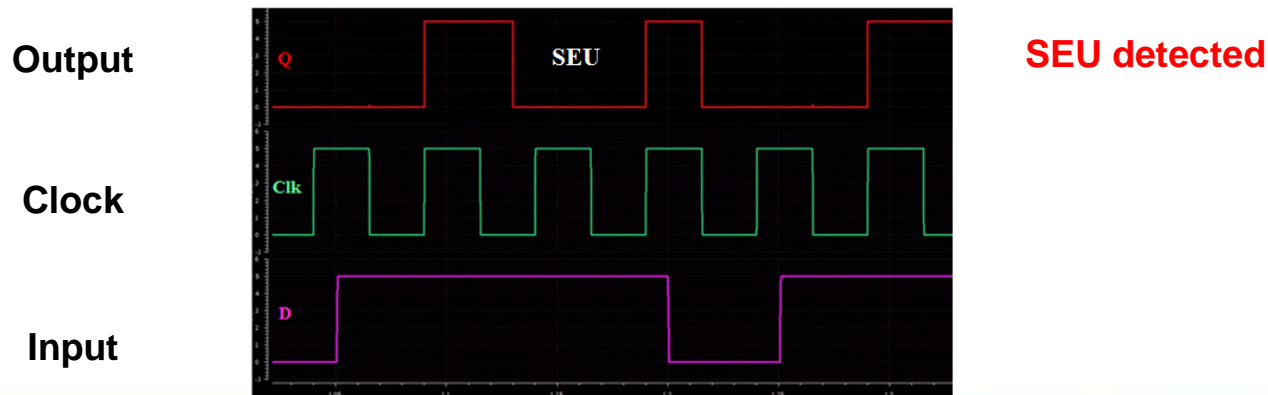


Logic state, temperature are considered depending on LET of heavy ions

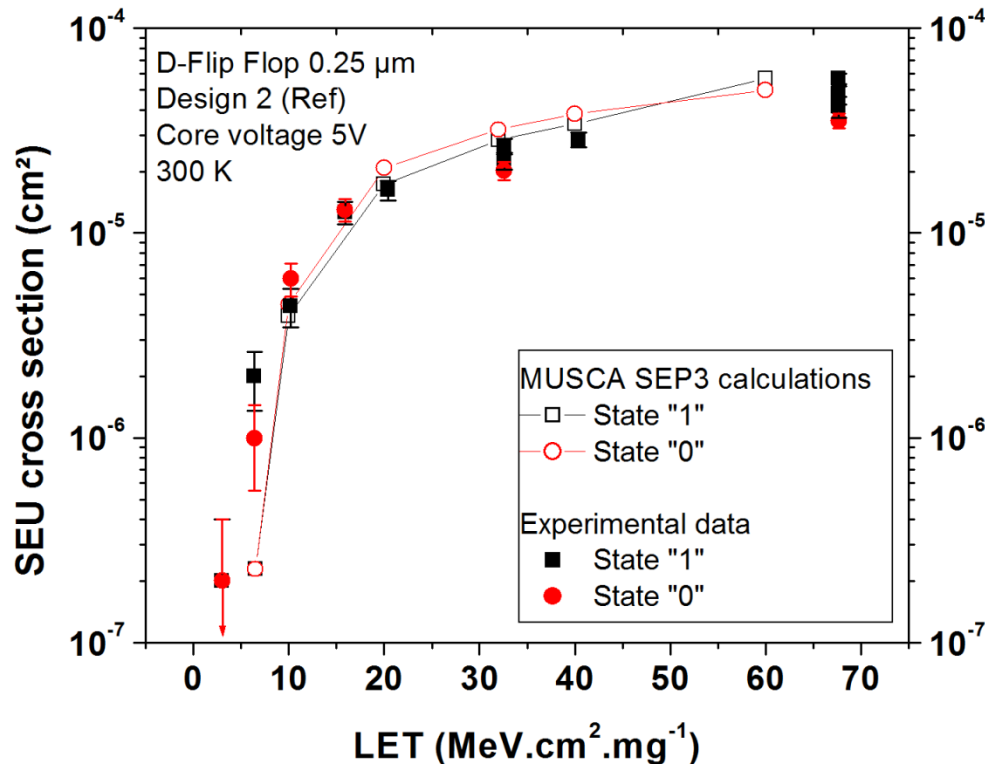
- Detection of SETs in the Flip-Flops (design 1 and 2)
 - Nominal working of the Flip-Flop



- SET/SEU occurrence on the Flip-Flop output

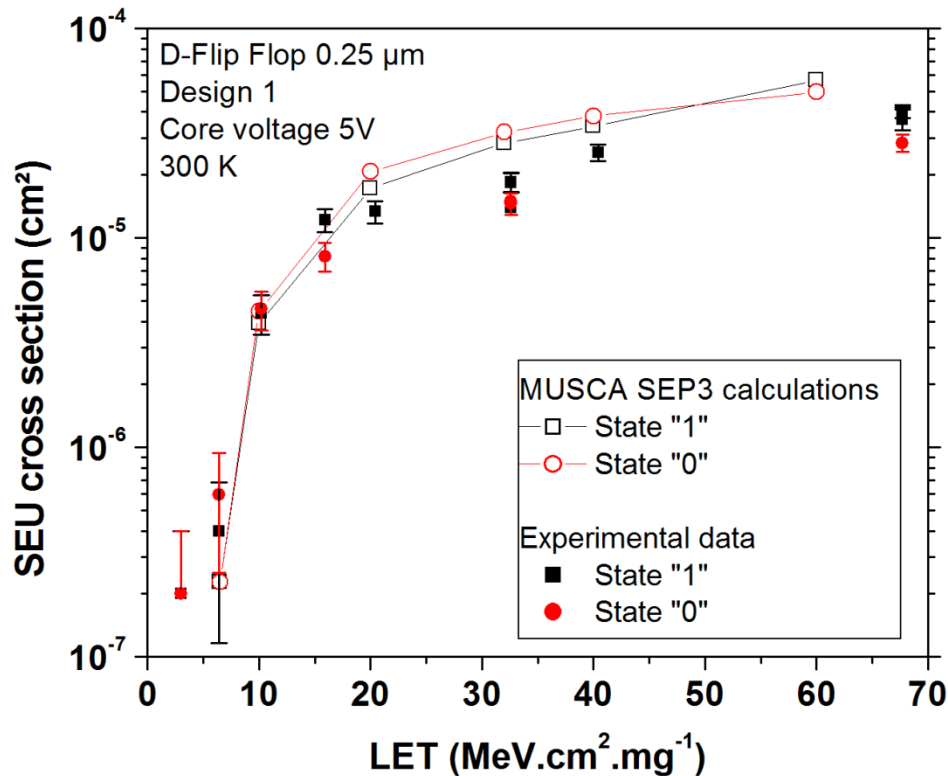


- Estimation of the SEU cross section of the Flip-Flop FDM2QHV (design 2)



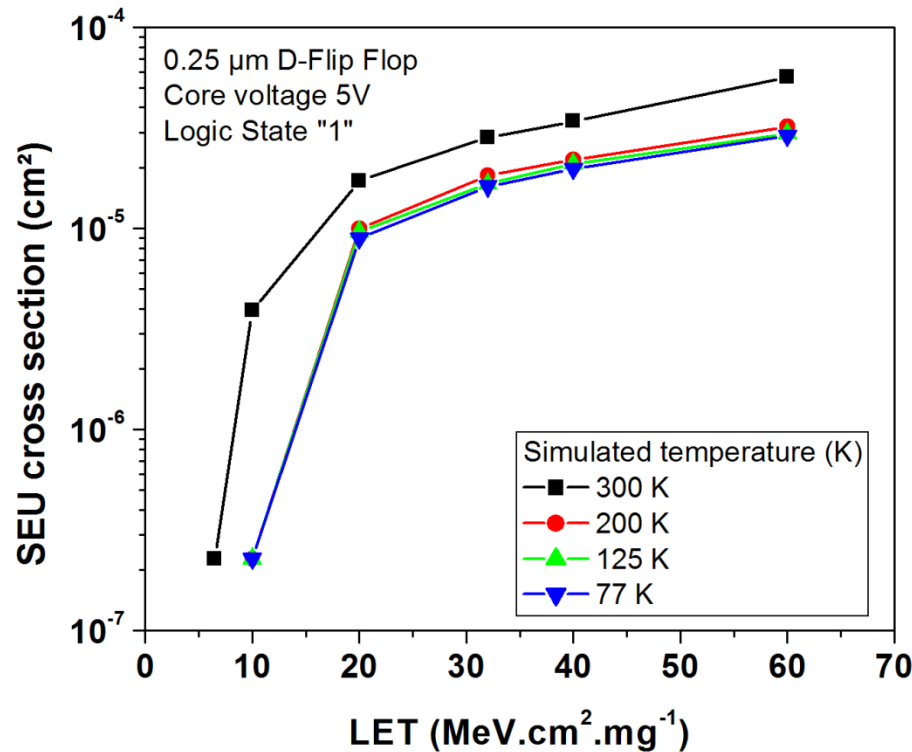
Good correlation of SEU sensitivity between exp. And simulation for the reference design of DFF

- Estimation of the SEU cross section of the Flip-Flop FDM2QHV (design 1)



Good correlation of SEU sensitivity between exp. And simulation for the reference design of DFF

- Effects of low temperatures on the SEU cross section of the Flip-Flop FDM2QHV (design 2)



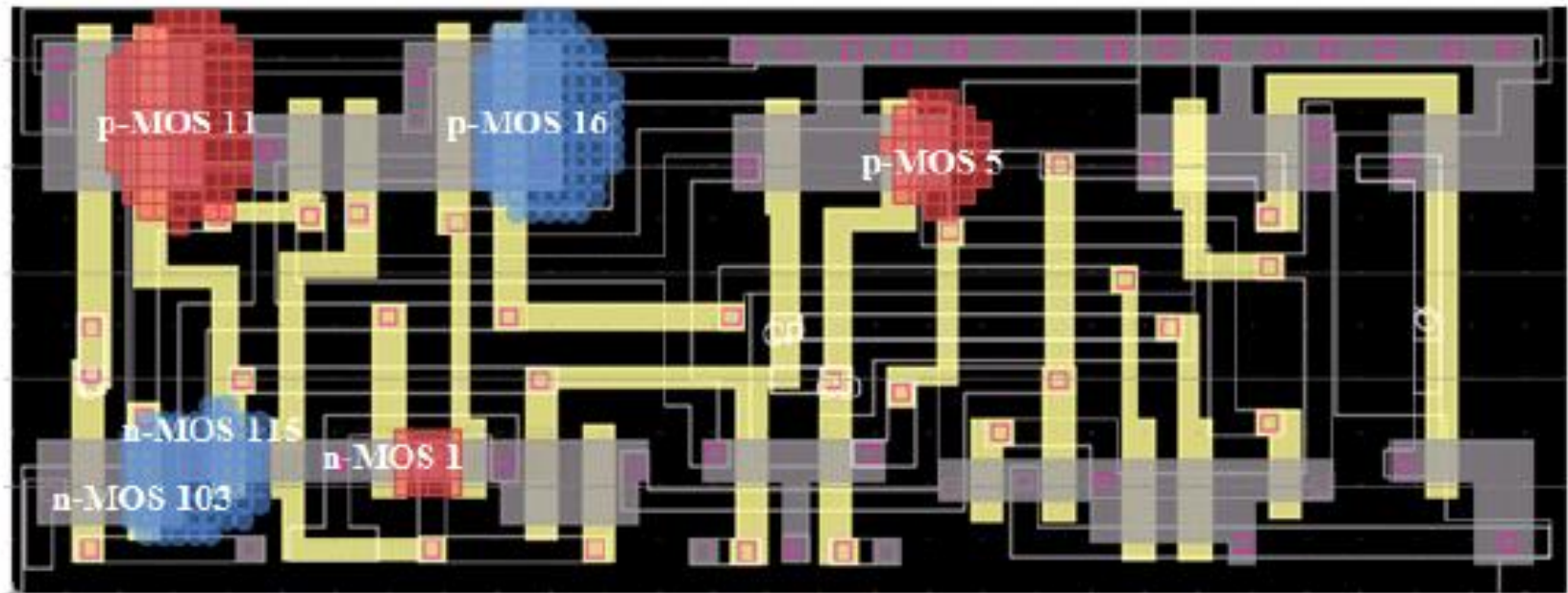
Lower temperatures \rightarrow Lower SEU sensitivity

Saturation of the temperature effects on the SEU sensitivity

- SEU sensitivity maps of DFF design 2 for a LET 58,8 MeV.cm².mg⁻¹ at 77°K

■ State « 1 »

■ State « 0 »

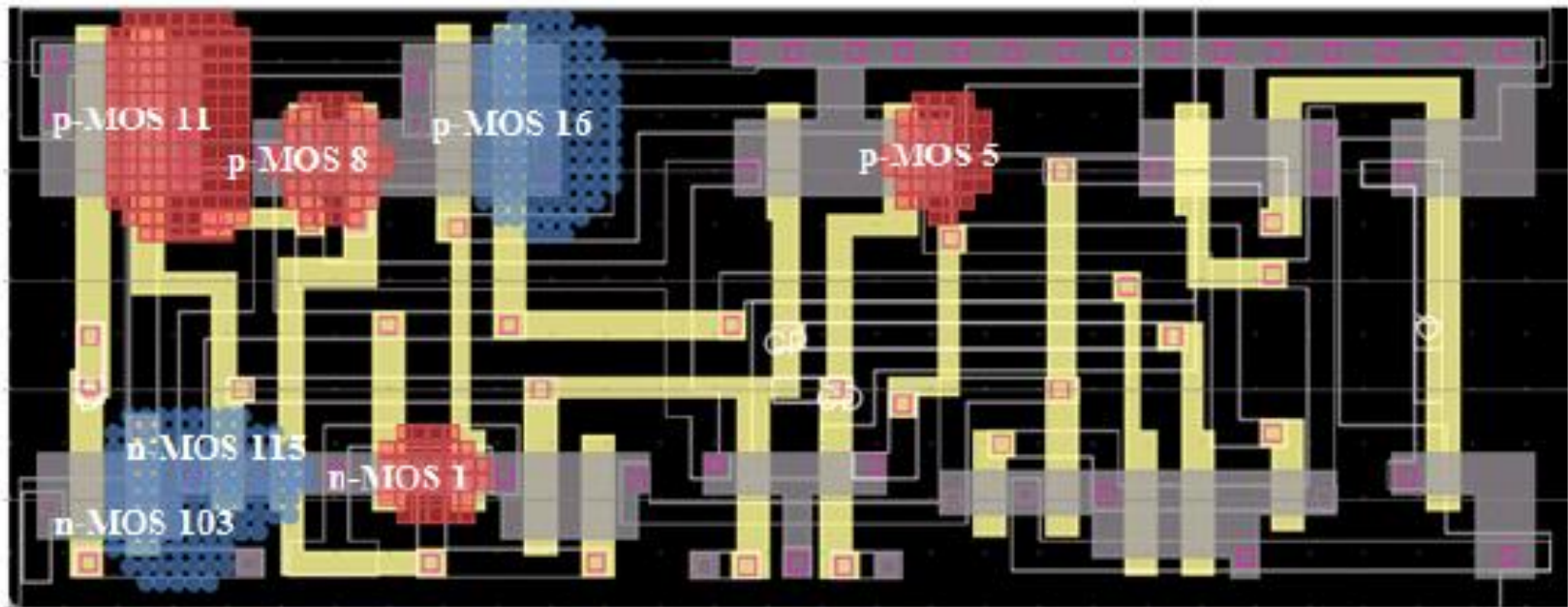


The logic state changes the SEU critical areas of Flip-Flop cell

- SEU sensitivity maps of DFF design 2 for a LET 58,8 MeV.cm².mg⁻¹ at **300°K**

■ State « 1 »

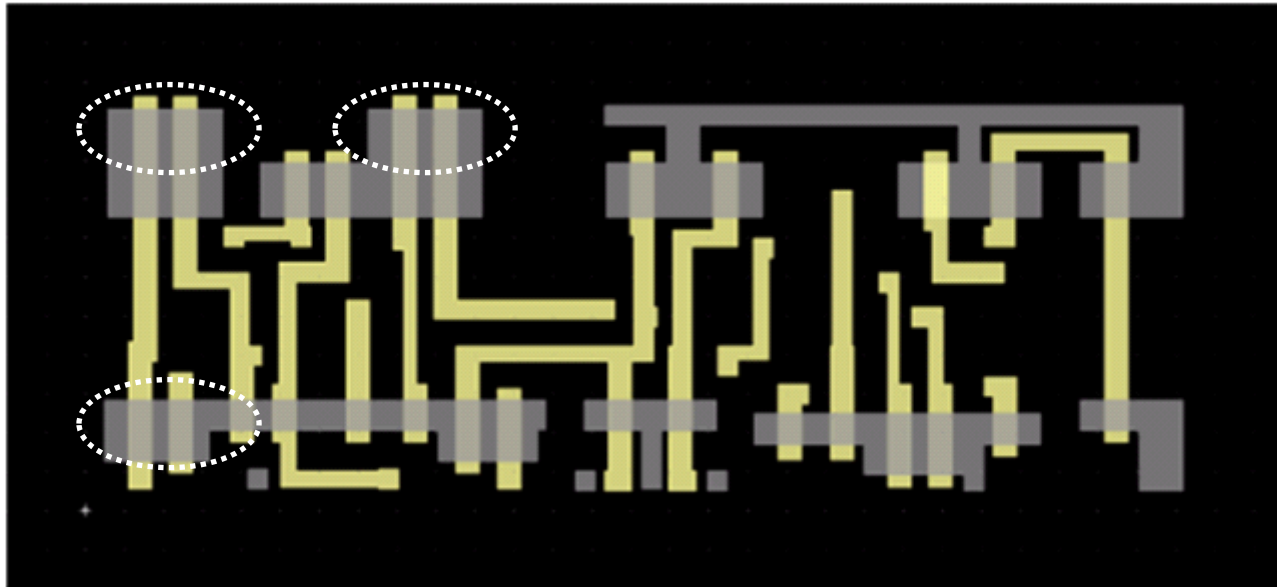
■ State « 0 »



At 300°K → New sensitive transistor (p-MOS 8) → State 1 more sensitive than State 0

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- Decrease the width of the wider sensitive n-MOS and p-MOS transistors

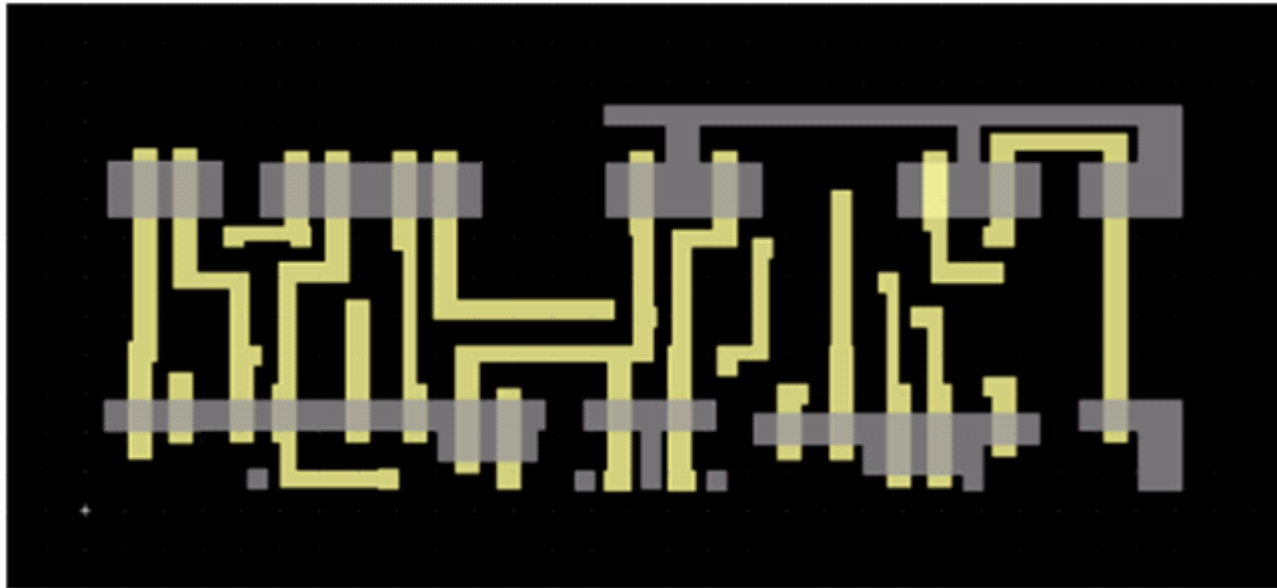


Limitation of the sensitive areas the DFF : 4 p-MOS and 2 n-MOS

Decrease the drive current → Decrease in the power needed

No area penalty

- Decrease the width of the wider sensitive n-MOS and p-MOS transistors

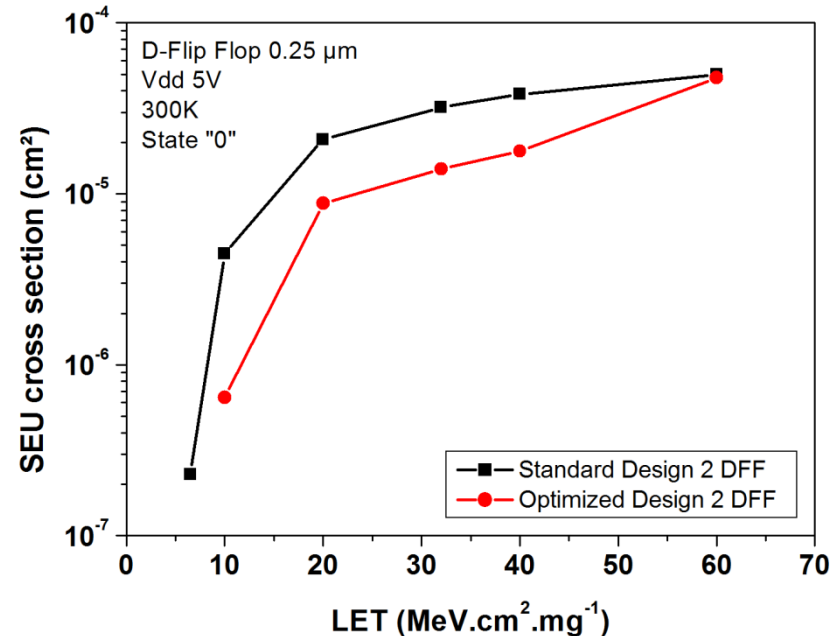
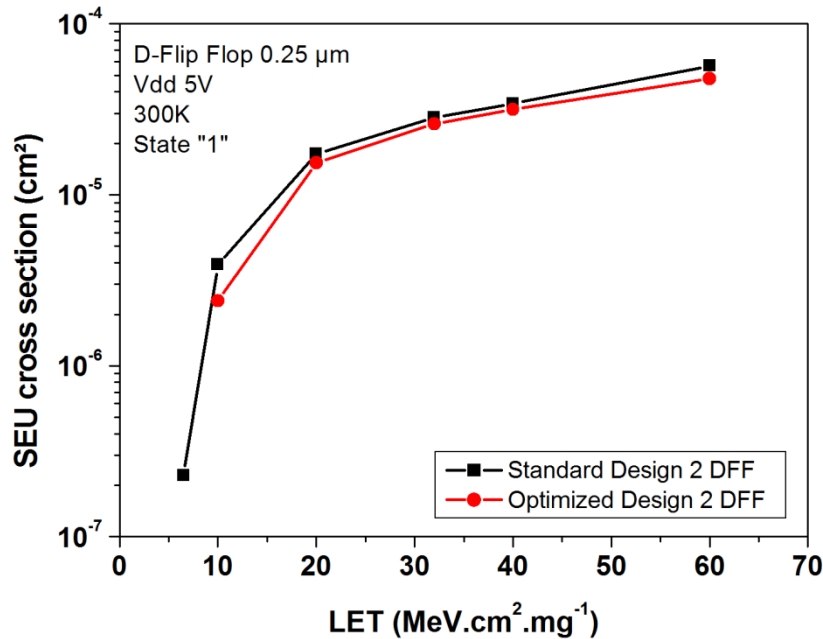


Limitation of the sensitive areas the DFF : 4 p-MOS and 2 n-MOS

Decrease the drive current → Decrease in the power needed

No area penalty

- SEU sensitivity of standard DFF and hardened DFF under heavy ions

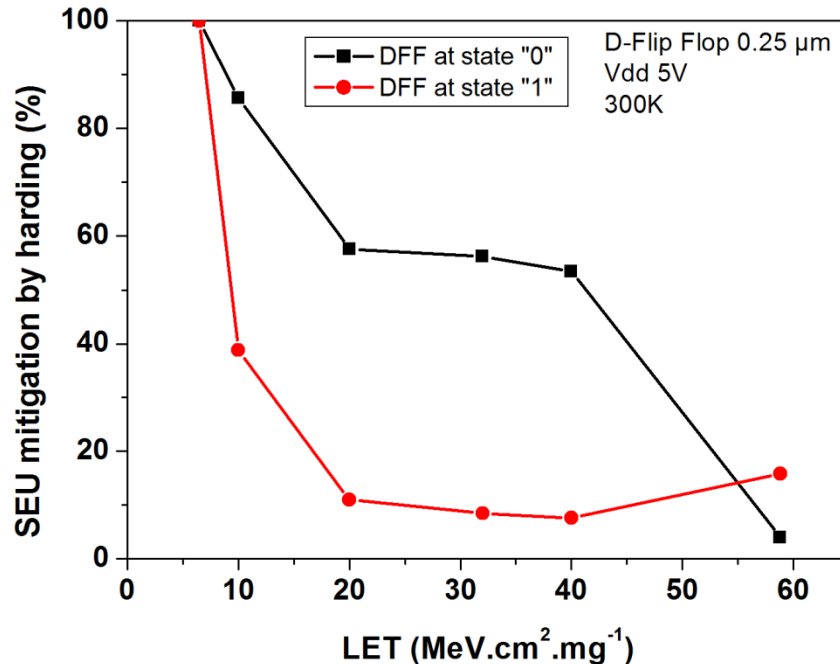


Improvement of the LET threshold of the DFF: increase of 50%



Better mitigation of SEU for "0" stored in the DFF

- SEU sensitivity of standard DFF and hardened DFF under heavy ions



Better improvement for "0" stored in the DFF excepted at the highest LET



Differences of the SEU mitigation are due to the complete immunity of p-MOS-16 at state "0" stored in the DFF

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- Multi-scales modeling (with MUSCA SEP3 tool) leads to estimate the SEU sensitivity of Flip-Flops at 300K and cryogenic temperatures.
- Good correlations of SEU calculations and SEU measurements from 2014 and 2015 heavy ion irradiation campaigns at UCL facility (Belgium)
- The prediction tool allows to propose failure analysis at circuit and layout level useful for harden by design DFF
- The new hardened design of DFF presents a good mitigation ratio with no area penalty and lower power consuming.

→ **Proposition of general hardening guidelines for DFF designs for space applications**

→ **Application of the SEE prediction tool (MUSCA SEP3) and analog mixed signal circuits**