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High Performance COTS based Computer for Regenerative Telecom Payloads

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High Performance COTS based Computer for Regenerative Telecom Payloads

- High Performance Processing Needs
- The High Performance COTS Based Computer Study (HiP-CBC)
- Application to Regenerative Telecom Mission

High Performance Processing Needs

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High Performance Payload Processing Needs

State of the Art

Dedicated ASIC

- High performance
- Specific applications with high non-recurring cost
- Outdated silicon technology (180 nm, 65 nm soon)

Examples: image compression (MCITHI), FFT core (FFTC)

Rad-Hard Programmable Components

- Outdated technology (most)
- High recurring cost

Examples: SCOC3 (GPP), AD-21020 (DSP),
RTAX-2000 (FPGA)

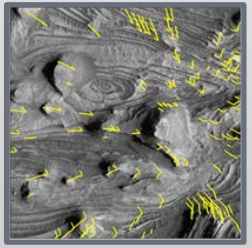
COTS-based Processor Boards

- Medium performance
- High recurring cost and US dependant technology

Example: Maxwell SCS750 (GAIA VPU)

Need for higher on-board processing

- **New opportunities and innovations such as advanced vision based navigation and regenerative telecom payloads**



- **Increase on-board autonomy**
- **Reduce the amount of information to be transferred to the ground segment**

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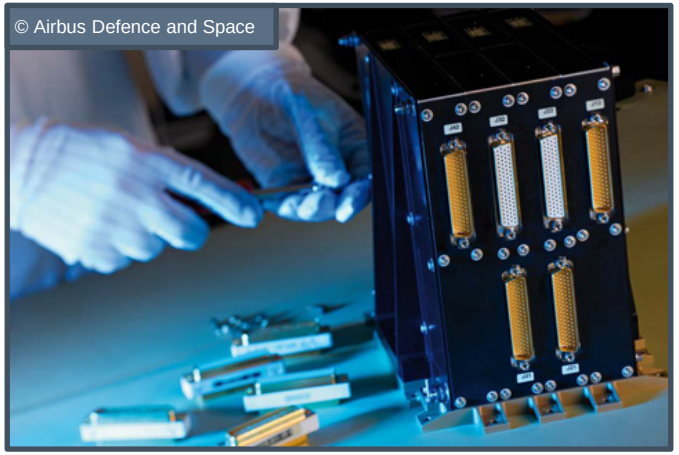
High Performance Payload Processing Needs

- **Payload / Instruments data processing**
  - Data-flow architecture
  - High data rate front-end interface for raw data filtering, pre-processing, and digitalization
  - Mission dependant on-board data processing
  - Data buffering in fast local memory
  - Control loops / latency requirements (in few cases)
  - Data storage in high capacity mass memory
  - Processing performance / power consumption



- **Industrial efficiency requires**
  Lower cost, Modularity, and Flexibility

→ ***Reprogrammable Devices***
FPGAs and micro-processors
ranging from DSPs to end high multi-cores

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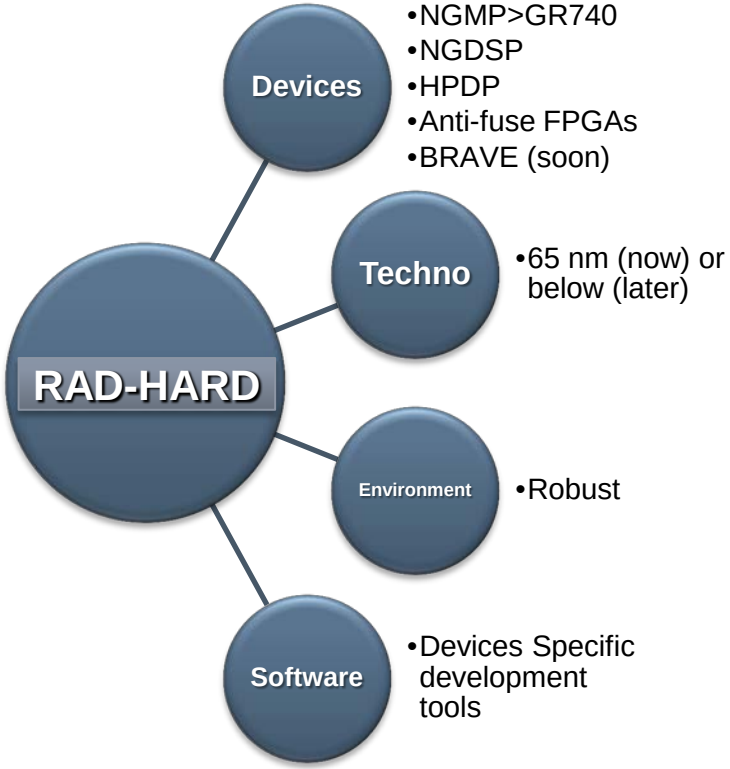
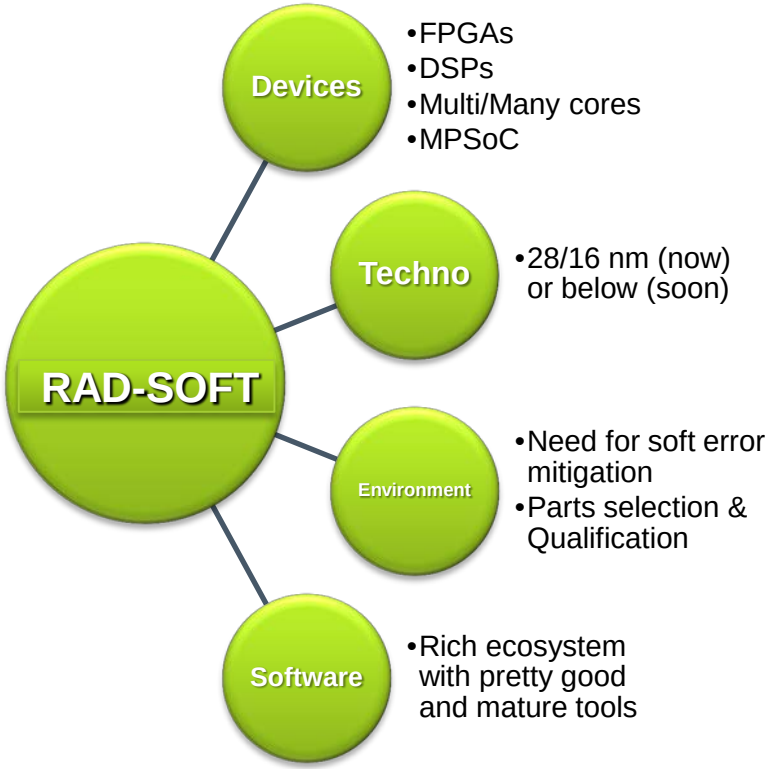
High Performance Reprogrammable Devices

Multi and many cores µ-processors / reconfigurable FPGAs





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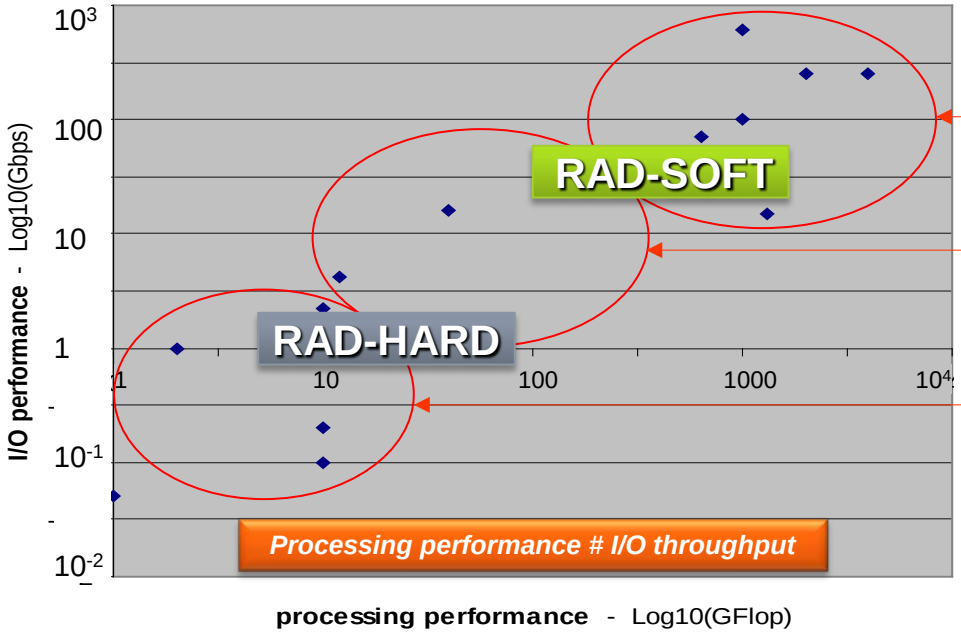
High Performance Processing Classes



Processing Performance classes

High > 100 GFlop
High-end COTS FPGAs

Medium [10 – 100] GFlop
High end many core CPUs or FPGAs

Low 0.5 - 10 GFlop
Multi – many cores µP/DSPs

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Commercial µProcessors and FPGAs

- **Dynamic roadmap with attractive products**
  - µProcessors: DSP6727, PPCs, ARM, ATOM…
  - FPGAs: Virtex (SRAM), ProAsic (Flash)
  - MPSoC: Zynq
- **Manageable radiations issues**
  - Destructive effects
    - Hard error free (e.g. latch up)
    - Total dose acceptable for many LEO missions
    - Some products with “rad-hard” characteristics
  - Non permanent effects require mitigation

RAD-SOFT components
May be used for a wide range of missions
(not for all)

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The High Performance COTS Based Computer Study (HiP-CBC)

High Performance COTS Based Computer (HiP-CBC)

- **Robust architecture for COTS based processing**
  - Use existing COTS devices (DSP, FPGA)
  - Mitigate radiation effects from a robust and programmable external device called **SmartIO**
  - Applications to payload data processing
- **Study priorities**
  - Mission scalability
  - Independence of the mitigation mechanism w.r.t. processing device
  - High data bandwidth standard interfaces
  - Suitable for different types of missions
  - TRL 5-6 demonstrator
    - Mature technology
    - DSP as COTS processor

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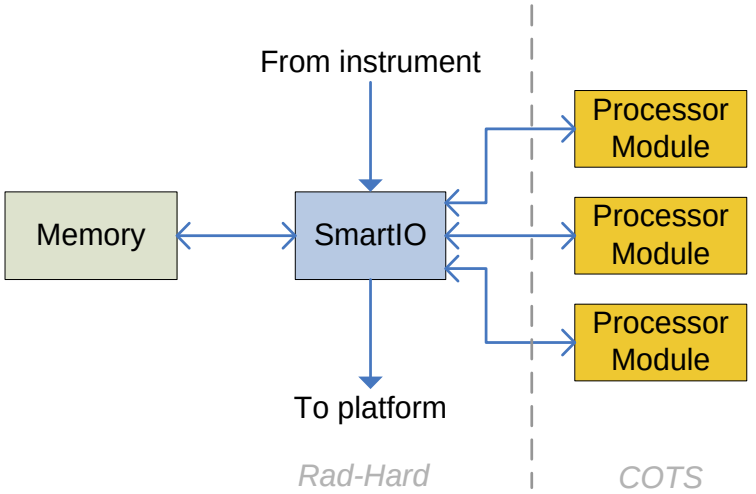
High Performance COTS Based Computer (HiP-CBC)

Concept

- **SmartIO**
  - Rad hard component
    - In charge of the isolation between the COTS world and the “rad-hard” world
  - Controls several COTS components
  - Provides scalable fault mitigation functions
  - Buffers instrument data in a fast local memory, and replays it in case of error
  - Acts as a master
- **Several Processor Modules**
  - Implemented with µProcessor or FPGA
  - Acts as slaves



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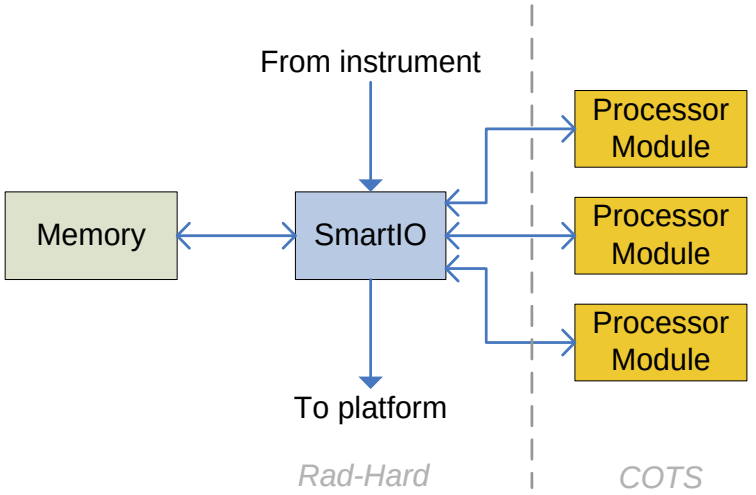
High Performance COTS Based Computer (HiP-CBC)

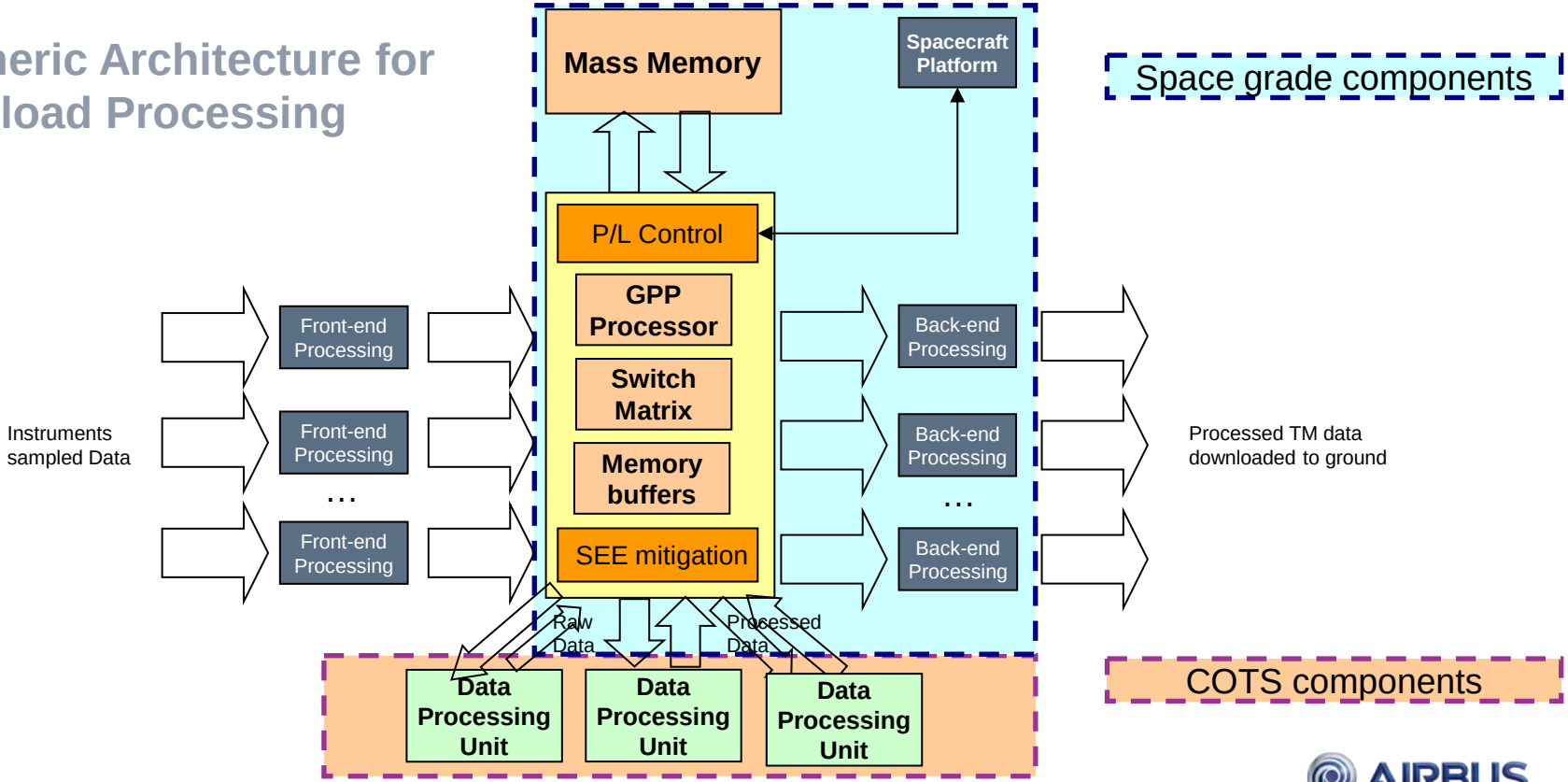
Benefits

- SmartIO / PM link is a standard high speed link such as LVDS, SpW, SpFi, SRIO, PCIe, Gbit Ethernet
  → Flexibility, technological independence
- PMs are slaves of the SmartIO
  → Simplicity of the fault model
- SmartIO in HW+SW to manage fault mitigation
  → Versatility
- Batch processing and result checking with signature
  → Performance
- Scalable architecture
  → Adaptable to mission requirements



High Performance COTS Based Computer (HiP-CBC)

Generic Architecture for Payload Processing



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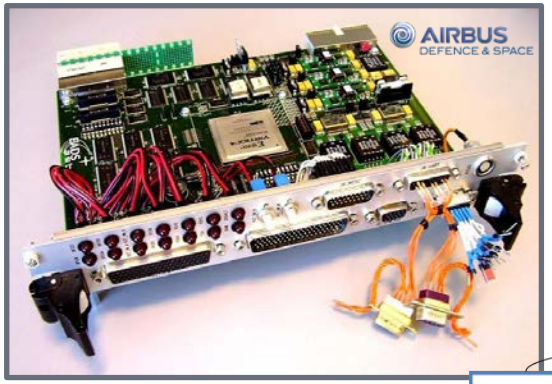
High Performance COTS Based Computer (HiP-CBC)

Demonstrator

- SmartIO with SCoC3 (Leon3) for control, monitoring and reconfiguration
- DSP board developed by OHB_{CGS} in Milano with a DSP 6727 from TI
- Demonstration Software on Smart I/O and Processing Module S/W
- Performance and availability model



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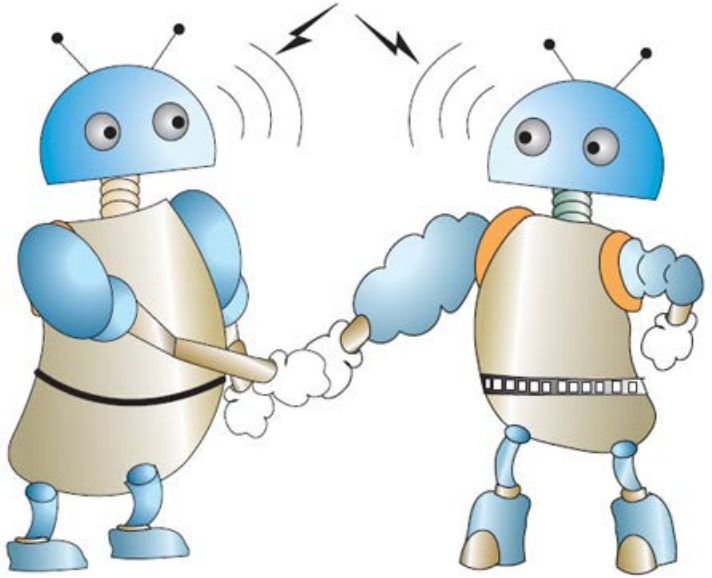
Application to Regenerative Telecom Mission

Context: Machine-to-Machine Communications

- **M2M**
  - Large market and growth potential
  - Increasing needs in the low-cost, low data rate segment
  - Terrestrial system lack of coverage of remote and desert areas



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Context: Machine-to-Machine Communications

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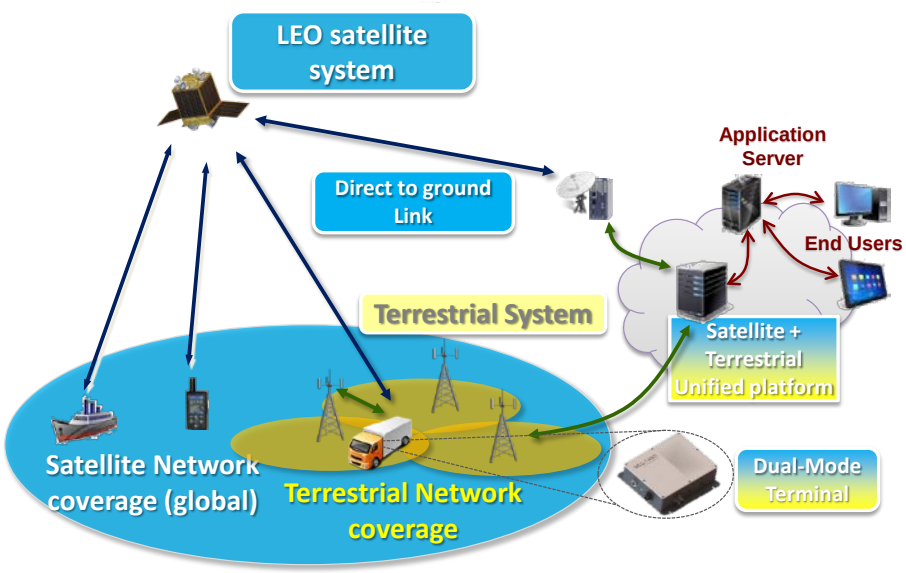
- **Hybrid system**
  - Satellite/terrestrial system for providing global continuous coverage
  - LEO satellite constellations embarking Software Defined Radio (SDR) payloads to reach this goal



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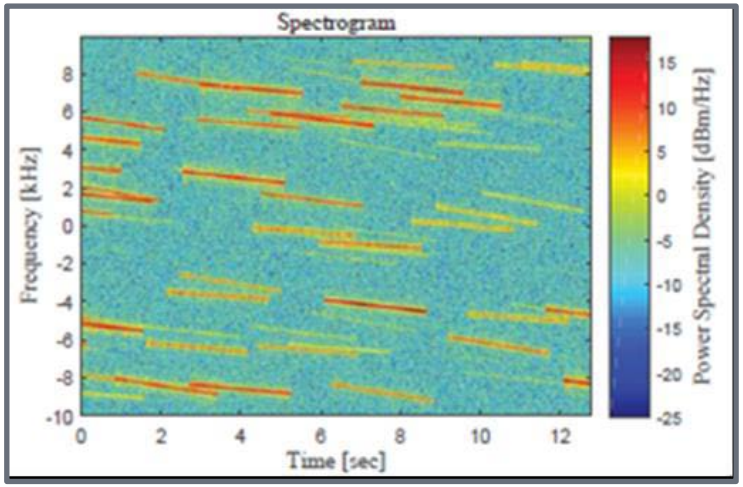
SDR Payload Processing for Low Data Rate M2M

Design Challenges

- Uplink PHY layer are typically based on spread spectrum or Ultra Narrow Band (UNB) technologies using random access techniques
- System can handle hundreds to thousands terminals at the same time
- Doppler drift effect of LEO satellite systems must be compensated



Requires Flexibility

- Protocols Updates (firmware, software)
- To serve other missions
  - ADS-B for air traffic management
  - Spectrum survey (3G, GPS, …)
  - Data collection in general

Very high performance for digital signal processing

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SmartIO G2 for SDR Processing: Trade-off Analysis

- ## Selection of the Processor Module

	SRAM FPGA	Flash FPGA	DSP	Many-cores
Flexibility	+++	- On-line reconfiguration is not recommended	+ Interfaces are not scalable and flexible	+ Interfaces are not scalable and flexible
DSP Performance	++	-- Flash technology is outdated (65 nm CMOS)	+	+++
Capacity	++	- Flash technology is outdated (65 nm CMOS)	++	+++
Power Consumption	+/-	+	++	---
TID Tolerance	+	-	+	?
Soft Error Sensitivity	--	- Configuration memory is immune to soft errors	--	--

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Best trade-off: very high level of flexibility with high DSP performance

The soft error sensitivity is compensated by the efficiency of the SmartIO mitigation

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SmartIO G2 for SDR Processing: Trade-off Analysis

- **Selection of the SmartIO**
  - Instrument is a single or even a multi-port RF front-end providing one or several ADC/DAC LVDS interfaces, with a resolution of samples greater than or to 8 bits
  - Nature of the processing with independent input and output data stream of samples promotes the use of a pipelined streaming architecture

Rad-tolerant FPGA seems to offer the best alternative to offer a sufficient number of I/O pins and bandwidth capacity

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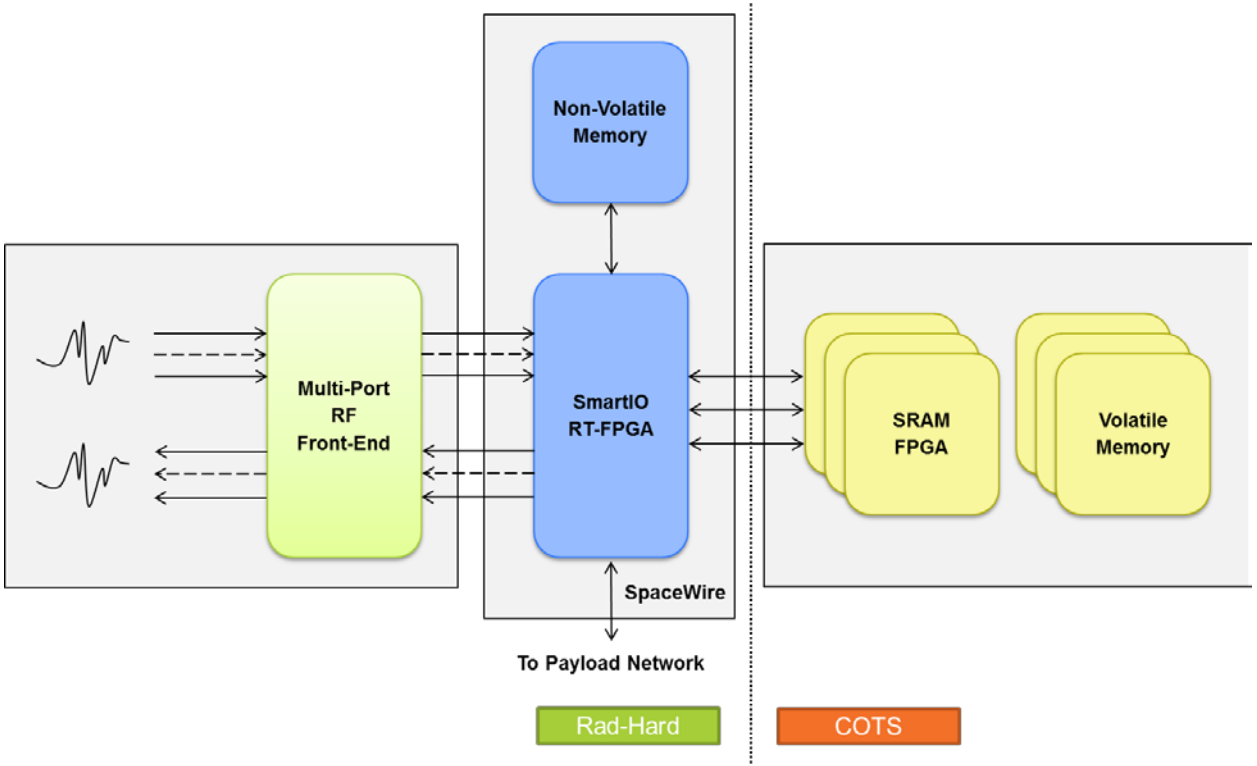
SmartIO G2 for SDR Processing: Typical Architecture



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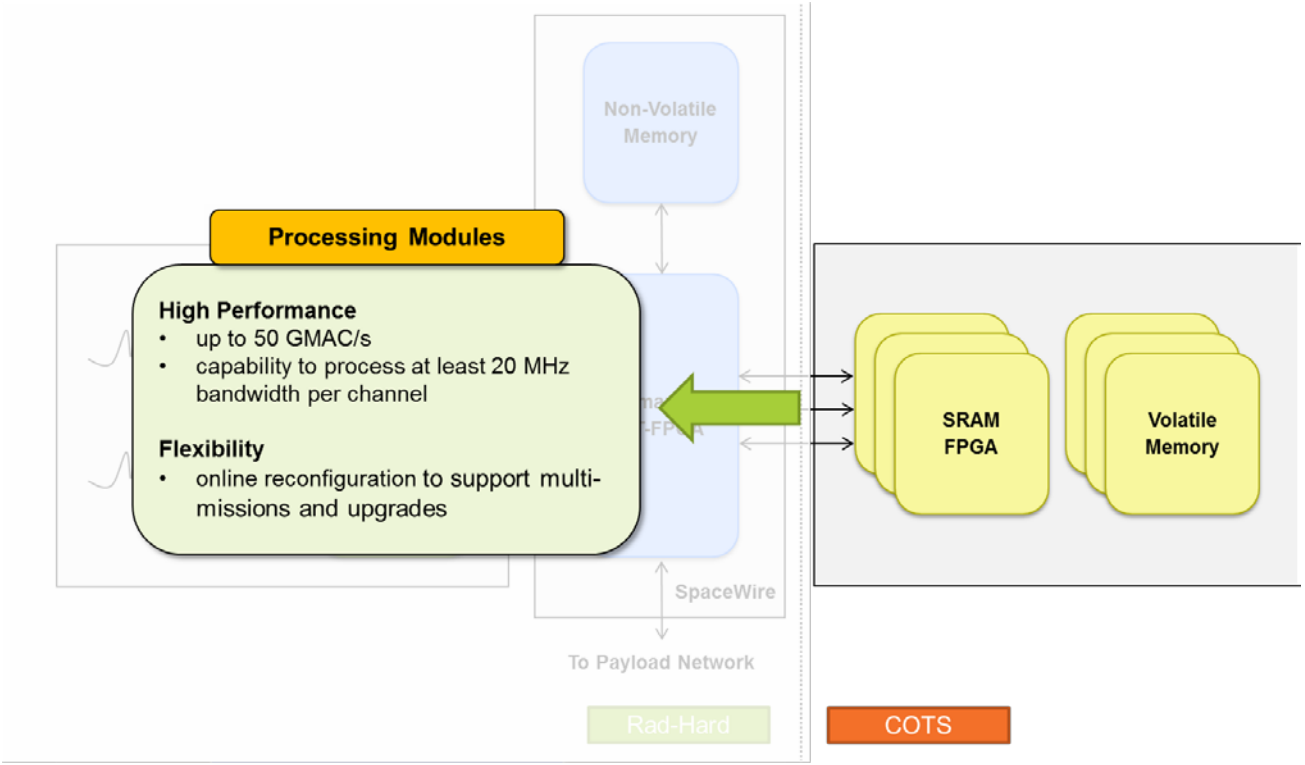
SmartIO G2 for SDR Processing: Typical Architecture



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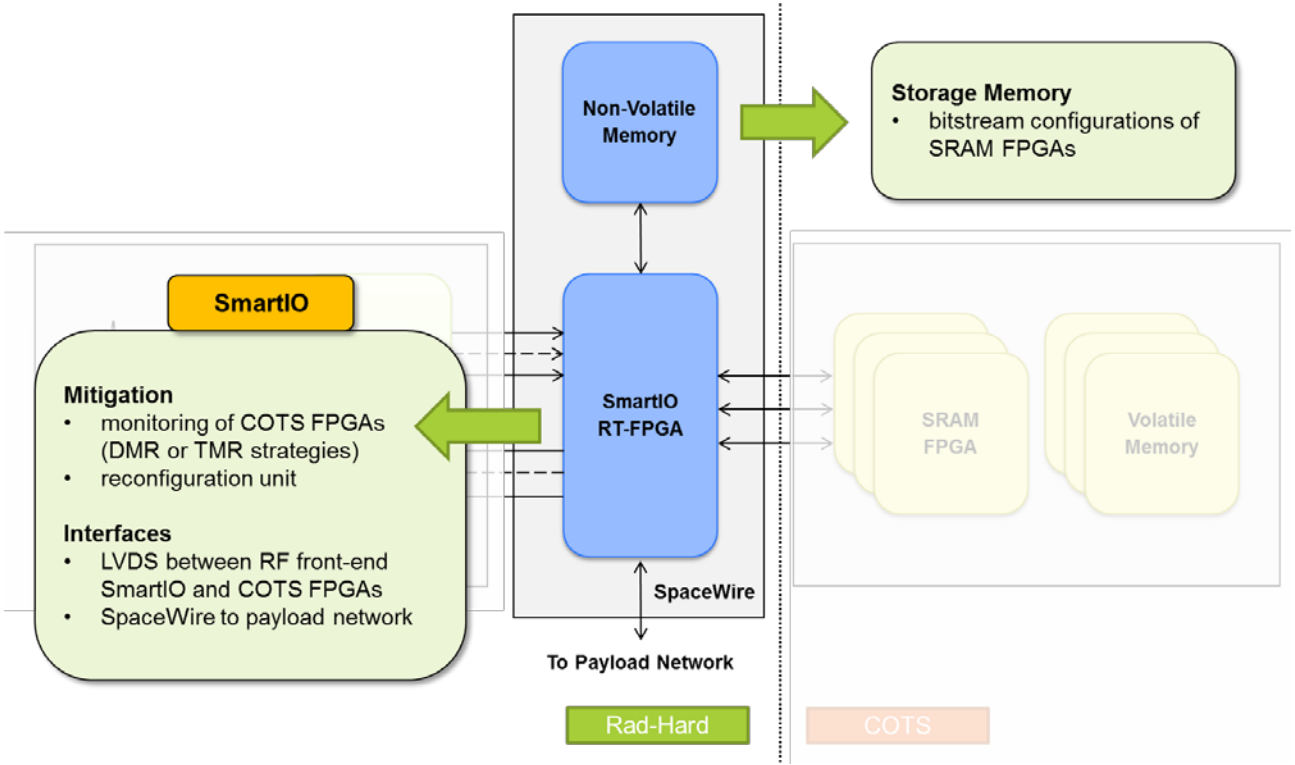
SmartIO G2 for SDR Processing: Typical Architecture



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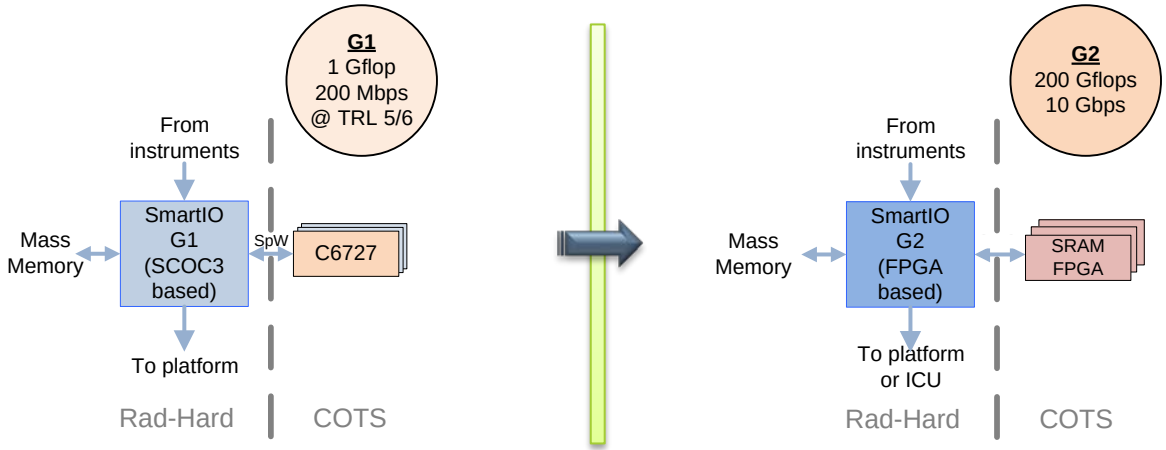
Summary

- **Reprogrammable FPGAs are essential for Payload / Instrument Processing**
- **High performance COTS Based computer study**
  - Demonstration with SCOC3 + DSP C6727
  - FPGA implementation in development for Software Defined Radio with RT-FPGA + SRAM FPGAs



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Thank you for your attention

Questions ?

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