SOI CMOS Frequency Synthesizer for Flexible Communications Payloads

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Abstract

This paper presents designed and measured results of a fractional-N frequency synthesizer in SOI CMOS Technology for next generation flexible communication payload. A tuning range from 4 GHz to 6 GHz is achieved using three integrated voltage-controlled oscillator (VCO), which enables all frequencies generation bellows 6 GHz by frequency division. Using current mismatch compensation circuit in charge pump, in-band phase noise of -93 dBc/Hz is achieved at 100 kHz offset in fractional-N mode. Also, to design radiation hardened Frequency synthesizer, we use design technique such as radiation hardening by design (RHBD), radiation hardening by process (RHBP), and radiation hardening by shielding (RHBS).

I. INTRODUCTION

The COMS payloads, up and down link frequency and the bandwidth are all fixed during the lifetime of the satellite. But increasing satellite lifetimes of more than 15 years, the ability to adapt the payload to new scenarios such as flexibility would be highly advantageous. So an agile-tunable Local Oscillator (LO) is the key components in the next generation flexible payload and needed for the development of the next generation satellite payloads. The agile wide-band frequency synthesizer based on a fractional-N PLL should be able to generate the wanted frequency within the wide-band such as S-band, C-band, and Ku-band.

Spacecraft designed to provide communications require the necessity to generate several LO frequencies for various up/down converters in the payload. The conventional technique of frequency multiplying a highly stable fixed reference signal to generate a number of LO signals will make the spacecraft higher in DC power, size and mass. In order to provide a lower spacecraft mass, size, and DC power, the LO signal generation must be accomplished by miniaturized digital integrated frequency synthesizers based on phase locked loops. Many circuits in Silicon, BiCMOS, Silicon-on-Insulator (SOI), GaAs, and SiGe make it easier to develop systems with frequencies up to several GHz and beyond. [1], [2] Depending on the device technology and manufacturing process, the SEU hardness or total dose tolerance may be such that they may not be suitable for high reliability space applications.

To design radiation hardened frequency synthesizer, these design techniques such as radiation hardening by design (RHBD), radiation hardening by process (RHBP), and radiation hardening by shielding (RHBS) are required. In this paper, we designed SOI CMOS frequency synthesizer using RHBP, and RHBD based on layout technique. And we will adopt the others technique such as RHBS and RHBD such as triple-redundancy technique in current project.



Figure 1: Block diagram of the VCO core

II. DESIGN

A. VCO core design

To increase flexibility in LO, a large frequency tuning range and excellent phase noise characteristics are a critical required in VCO core. First, in order to enhance phase noise characteristic in VCO, the current source is eliminated to reduce 1/f noise from bias line. But this architecture has other problems in VCO performance such as pushing and pulling figure, and process variation. So we use low drop-out (LDO) regulator with 2-bit output voltage control circuit in supply of VCO as shown in Fig. 1. Thus, output power and current consumption in VCO should be changed according to LDO. And this output current should also be fixed according to oscillation frequency and temperature variation to get stable phase noise performance. However, this circuit requires additional die area and noise source from LDO output is not eliminated completely. PMOS cross coupled topology is used for VCO core circuit and using five VCOs to reduce VCO gain variation according to wide range of oscillation frequency from 3.6 GHz to 6.1 GHz. 5-bit switched MIM capacitor array in each VCO is used to cover oscillation frequency of 3.6 GHz to 4.1 GHz, and 4.1 GHz to 4.6 GHz, 4.6 GHz to 5.1 GHz, and 5.1 GHz to 5.6 GHz, and 5.6 GHz to 6,1 GHz, respectively.

Due to stable operation of LDO, phase noise variation is within 2.4 dB over $1.6 \sim 2.0$ V power supply and $-40 \sim 85^{\circ}$ C temperature range. VCO core including LDO draws $2.8 \sim 5.6$ mA according to oscillation frequency from 1.8 V supply voltage. Frequency synthesizer consists of three VCOs, PTAT bias, LO generation block such as divider and buffer (or drive) amplifier, loop-filter and fractional-N PLL.

B. PLL design

Fig. 2 shows the block diagram of the designed frequency synthesizer including 5 on-chip VCOs. The sigma-delta fractional N frequency synthesizer includes a 20-bits sigmadelta modulator of third-order MASH type so that it achieves a fine frequency resolution of about 34 kHz. The charge pump using an analog calibration method with two op-amps eliminates output current mismatch. The external loop filter is used to optimize loop bandwidth each selected frequency bands. To calibrate loop bandwidth, the charge-pump currents are able to control by programmable digital logic according to band selection. The prescaler including true single-phase clocked (TSPC) type D-type flip-flop (DFF) in N dividers has up to 1.5 GHz operations. The feedback divider consists of 10-bit pulse counter and 4-bit swallow counter.



Figure 2: The block diagram of the designed frequency synthesizer including 5 on-chip VCOs.



Figure 3: The chip photograph of the proposed Frequency Synthesizer including VCOs, I2C and PTAT

Fig. 3 shows the chip photograph of the proposed frequency synthesizer. The integrated frequency synthesizer including 5 VCOs, LO generation block, LDO, bias, and I2C, occupies 5.0 mm by 2.5 mm. And this IC is fabricated using 1P4M 0.18 um RF SOI CMOS process.

C. Frequency Synthesizer using External VCO

To overcome the limitation of the phase noise characteristic in on-chip VCO, we added input/output port in designed frequency synthesizer chip to use external low-phase noise VCO. Fig. 4 shows the block diagram of the designed frequency synthesizer using external VCO. Because the operation frequency in the prescaler has up to 1.5 GHz, we use divider-by-8 circuit between VCO output and PLL input. And to control VCO tuning voltage from 0 V to 15 V, active loop filter and level shifter is used in frequency synthesizer module.



Figure 4: The block diagram of the designed frequency synthesizer using external low-phase noise VCO and divider-by-8.



Figure 5: PLL based on on-chip VCO test board and test fixture

III. MEASUREMENT

A. On-Chip VCO measurement

The chip is fabricated in the TowerJazz 0.18 um 1P4M CMOS SOI process as shown in Fig.1. The chip size is 5 mm X 2.45 mm, and all circuit blocks have been successfully integrated on chip, including VCO, bias circuit, and I2C. The chip is measured with a 1.8V supply voltage and consumes 66 mW under maximum current settings, and 61 mW in low-current mode. The measured frequency range is from 3.6 GHz to 6.1 GHz, corresponding to a frequency tuning range of 14%. The measured PLL output spectrum at 10 GHz is shown in Fig. 7, where the phase noise is about -93 dBc/Hz, and -117 dBc/Hz at 100 kHz, and 1 MHz offset frequency. In this work, the VCO frequency tuning range is divided into 8 subbands, and the measured VCO gain (Kvco) is about 80 MHz/V.





Figure 8: Measured PLL using external VCO phase noise at 8.5 GHz



Figure 7: Frequency synthesizer using external VCO test fixture and test setup photograph.

B. External VCO measurement

The PLL module using designed SOI CMOS PLL is fabricated based on Rogers4003C substrate and using Hittite HMC509LP4E VCO, and HMC494LP3 frequency divider as shown in Fig. 2. Fig. 6 shows the PLL module and test set-up. The test fixture size is 100 mm x 94 mm, and all circuit blocks have been successfully integrated on chip, including VCO, bias circuit, and I2C. The frequency synthesizer module is measured with a 5V supply voltage and consumes 1250 mW in typical value. The measured frequency range is from 7.2 GHz to 9.0 GHz. The measured PLL output spectrum at 8.95 GHz is shown in Fig. 7, where the phase noise is about -100 dBc/Hz, -112 dBc/Hz, and -131 dBc/Hz at 100 kHz, 1 MHz, and 10 MHz offset frequency. In VCO, the VCO frequency tuning range is determined by voltage tuning from 0 V to 15 V, and the measured VCO gain (K_{VCO}) is about 100 MHz/V at control voltage of 5 V. Table 1 compares the PLL performance with that of other PLLs designed 10 GHz applications.

IV. CONCLUSION

This paper provides an overview of frequency synthesizer design techniques for Communications Satellite payloads. The proposed flexible LO architecture shows wide-band, lowpower, and low phase noise performance with optimal current consumption for various satellite payload frequency band. Thus, this type of synthesizer can be used in multi-band flexible agile LO.

V. ACKNOWLEDGMENTS

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Ref.	Unit	[3], [4]	[5]	This paper On-chip VCO	This paper External VCO
Frequency Range (GHz)	GHz	8.67 GHz ~ 10.12 GHz (14.3%)	10.1 ~ 11 GHz	3.6 GHz ~ 6.1 GHz	7.2 GHz ~ 9 GHz
Phase noise (1 MHz offset)	dBc/Hz	-102 dBc/Hz	-100 dBc/Hz	-117 dBc/Hz	-112 dBc/Hz
Technology	Nm	TSMC 0.18 um 1P6M CMOS	0.18 um CMOS	TowerJazz 0.18 um 1P4M SOI CMOS	TowerJazz 0.18 um 1P4M SOI CMOS
Power consumption	mW	44mW/70mW	113 mW	66mW	1250 mW (including external VCO, divider)
KVCO	10	~ 300 MHz/V	-	~ 80 MHz/V	~ 100 MHz/V
Chip Size	12	1400 um x 964 um	0.86 x 0.68 mm	5000 um x 2450 um	600 um x 700 um (PLL only)
Reference spurs	dBc	-48	-50	-50	-50

Table 1: Summary table for comparison with other PLLs.