FPGA Radiation Hardening by Design in CMOS65nm

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Abstract

In a radiative environment, when a particle with a given LET (Linear energy transfer in MeV.cm²/mg) hits the substrate of a circuit, it creates electron-hole pairs along its trajectory; this causes current injections between junctions and consequently upsets node voltages resulting in a possible loss of information. Due to technology down-sizing and reduction of supply voltage, circuits become even more sensitive to radiation.

In this work we designed a full custom radiation hardened library for FPGA using ST CMOS 65nm process. In order to improve the reliability of our FPGA, dedicated to the applications in radiative environments, our full custom library has been simulated using IROC software (TFIT). The general methodology and particularly the different steps of a SRAM reliability improvement will be presented.

I. Design Methodology for Hardening

During the hardening process, two kinds of studies were carried out:

- The Single Event Upsets (SEU) that is a direct upset of a sequential logic (SRAM configuration and latches of the Flip Flop (FF)) leading to a bit flip.
- The Single Event Transient (SET)
    - The SET in the clock networks can have 2 effects: jitters that occur at the clock edge and the glitches that occur between the clock edges [1]. These effects can make a bit error to propagate in FF. The design efforts are put on the glitches considering a static clock. In our designs, the jitters are less probable than glitches because the minimum period of a clock is 5ns whereas the SET duration is less than 300ps for a LET less than 58 MeV.cm²/mg in normal incidence as shown in Figure 1. The smallest clock glitch to write in FF is 150ps. Hence the clock glitches longer than 150ps are considered as a SET error.
    - The SET in the reset networks: a glitch longer than 150ps on reset signal can reset a FF storing "1" to "0".

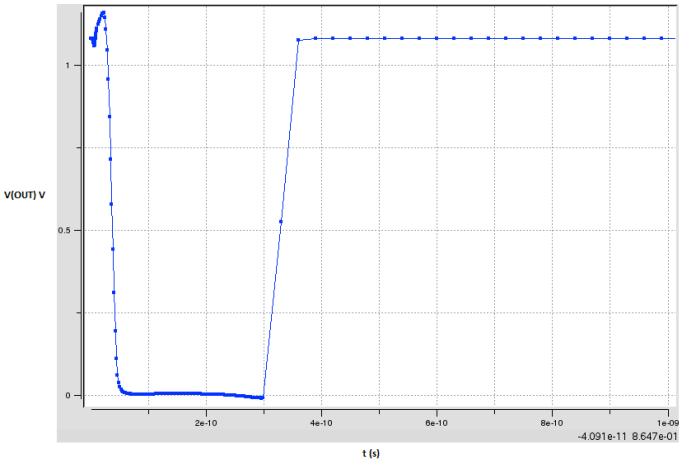


Figure 1: Max duration SET for normal incidence, a LET of 58Mev.cm²/mg

SEU and SET effects are studied and radiation hardening is performed on all the library cells that are sensitive to these effects:

- SEU in configuration memory: configuration memory of our SRAM based FPGA; they are very critical and require a high level of hardening.
- SET on clock/reset buffer and matrix: they propagate clock and asynchronous or synchronous reset into the circuit with a low skew.
- SEU/SET Digital Flip Flop: user register.

For each cell under study, the smallest capacitive load for charge collection in a particle incidence was considered as the worst case.

In order to improve the reliability, design optimizations are made on structure and layout of the library cells. First the structure is hardened by identifying sensitive nodes with a current injection model of particle incidence and then the layout is optimized using TFIT software [2]. TFIT uses a realistic compact model of the technology to calculate current injection and their effect by running electrical simulation for different positions and angles of incidence. By defining an error criterion, TFIT gives the cross section which represents the whole sensitive area (normal to the incidence) through which a particle impact causes a SEU/SET. The simulations are done for normal incidence with a max LET of 58MeV.cm²/mg, 50nm position step, under lowest supply voltage of 1.08V, typical corner and 25°C temperature. Figure 2 shows the sensitive area for normal particle incidence on an unhardened SRAM: for each incidence position TFIT gives

the critical LET for SEU error. The cross section is reduced by putting more distance between sensitive nodes and by bringing the tap closer to them. Other simulations that consider different incidence angles are also done.

II. Step by step hardening of a configuration SRAM in a cell example

For a cell containing a configuration SRAM, different step of hardening were done:

- A first test chip (kipsat3) designed with two version of this cell:
  - with unhardened SRAM
  - with hardened SRAM without layout optimization
- A chip ng_medium designed with a hardened SRAM with layout optimization with TFIT.

At each step the same layout area is kept for this cell.

For each cell TFIT gives the sensitivity map which gives the minimum LET that causes a SEU for normal incidences at each position:

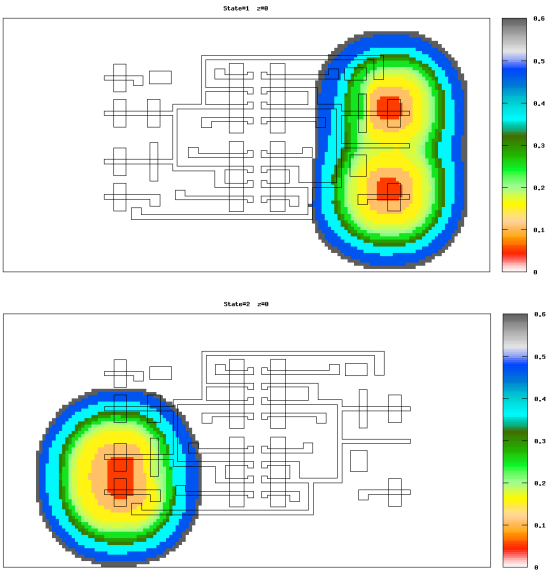
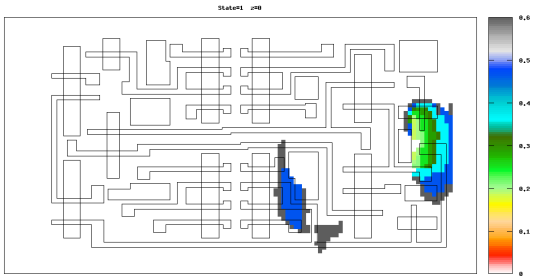


Figure 2: Sensitivity map **unhardened SRAM** LETmin(x,y) pc/um



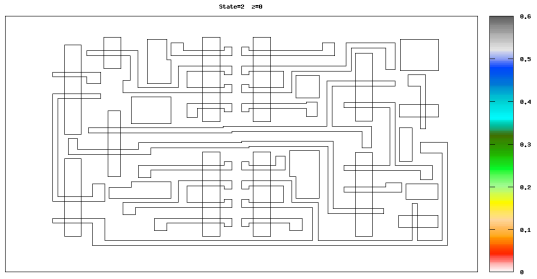


Figure 3: Sensitivity map for **hardened SRAM without layout optimization** LETmin(x,y) pc/um

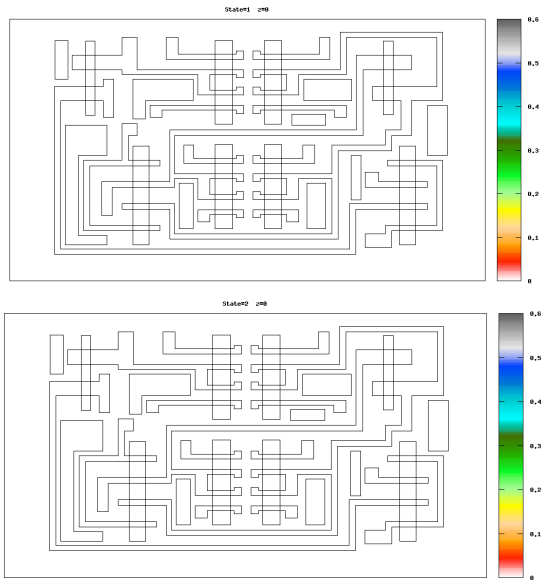


Figure 4: Sensitivity map for **hardened SRAM with layout optimization** LETmin(x,y) pc/um

The unhardened cell contains the N tap and there is a P tap cell that is placed every 3 cell at maximum. The hardened cell without layout optimization has a tap cell placed exactly every 6 cell. Whereas the hardened cell with layout optimization has its own N/P tap.

III. SRAM Structure hardening

A first state of art has been performed using a double exponential current injection model for a particle impact [3] that give an approximation of the current injection through source/bulk or drain/bulk junction (diffusion), as show on the Figure 5.

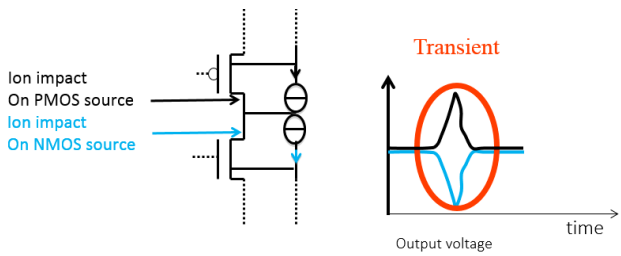


Figure 5: Single event effect on circuit and voltage

The double exponential model [3] calculates the current as follow for a given LET: $I_{rad}(t) = \frac{Q_c}{\tau_d - \tau_r}\left(e^{-\frac{t}{\tau_d}} - e^{-\frac{t}{\tau_r}}\right)$.

With [4]:

τ_r: Collection time of junction ≈ 200ps,

τ_d: Ion track time constant ≈ 50ps,

Qc the total amount of charge created by the ion track:

$Q_c = q\frac{\rho \cdot LET \cdot d}{E_g}$.With d~1um depending on technology, very difficult to be estimated.

Even if this model gives an estimation of the current wave and has difficulties to relate charge and LET, it shows the MOS junction through which a current injection could make a bit flip, and it give the minimum/critical charge that makes SEU. The unhardened structure based on 6T SRAM can have SEU by upsetting only one of the two nodes as show below:

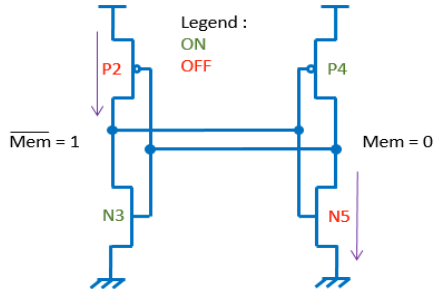


Figure 6: Unhardened SRAM schematic

Table 1: Unhardened SRAM critical charge with double exponential model.

MOS sensitive junction	Critical charge (fC)
P2	21
N5	9

Our hardened SRAM based on the DICE structure [5] can have a bit flip only if the current is injected through several junctions. This has been simulated by considering that the current is divided between the junctions with a sweep on the ratio. Table 2 gives the min critical charge for the injections in junction couples:

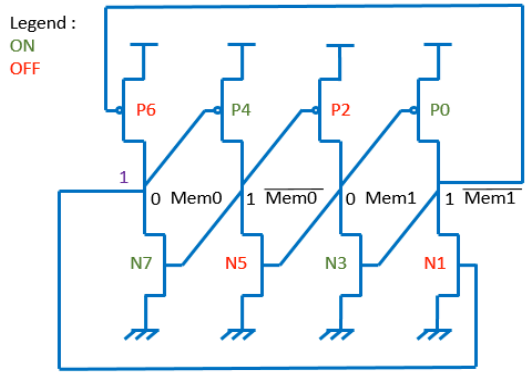


Figure 7: Hardened SRAM critical charge with double exponential model for multiple node injection

Table 2: Hardened SRAM critical charge with double exponential model for multiple node injection

MOS sensitive junction couples	Critical charge (fC)
P2 - P6	42
N5 - N1	21
P6 - N5	11
P2 – N1	11

The DICE structure can only be upset by some of the couples among the P2, P6, N5 and N1 junctions when storing a 0, whereas the other junction helps to retain the data, they will be called retaining junction. These junctions should be placed between sensitive nodes in layout. For the other state this is the opposite : P2, P6, N5 and N1 are the retaining junction whereas some of the couples among the other junctions, are sensitive.

IV. SRAM Layout Optimization

The hardened SRAM is a redundant structure which can only have SEU by upsetting certain diffusions couples depending on the state. In order to optimize the layout for a given state, the distance between the diffusions of each sensitive couple is maximized and the diffusion that help to retain the data, are put between them. The following diagram show that the critical distance is multiplied by four after the layout optimization.

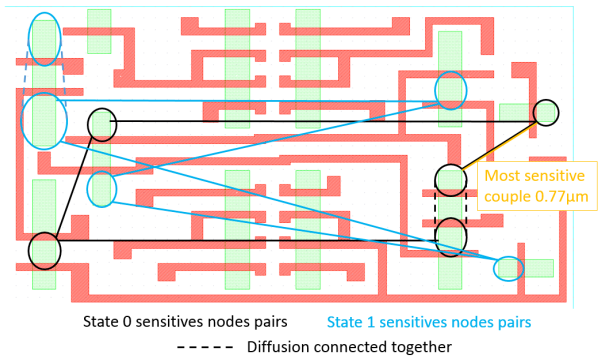


Figure 8: Distance between sensitive and retaining junctions for **hardened structure without layout optimization**

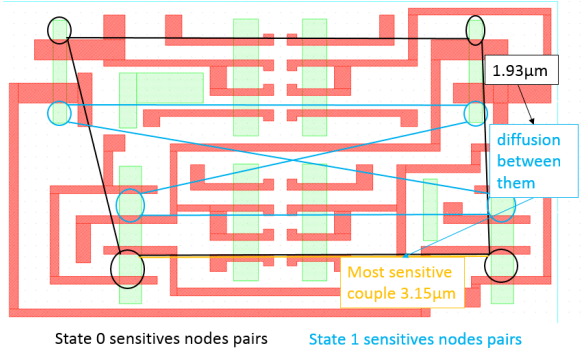


Figure 9: Distance between sensitive and retaining junctions for **hardened structure with layout optimization**

V. Results

A. Simulation

For normal incidence of a particle with a LET of 58MeV.cm²/mg as in Figure 12, the normal cross section is reduced by a factor of 6 by using the hardened structure without layout optimization.

For the hardened structure with layout optimization, the normal cross section is zero. Since the redundant DICE SRAM cross section has a high angular dependency [6], the structure has been simulated for 3 tilt angles (33.6°, 60°, 80.4°) 8 rotation angles with 45° step. For a tilt of 80.4° and a rotation of 180° the hardened structure shows a cross section as in the Figure 10 below. In comparison with the Figure 9, the sensitive area on Figure 10 is on trajectories between the sensitive node couples.

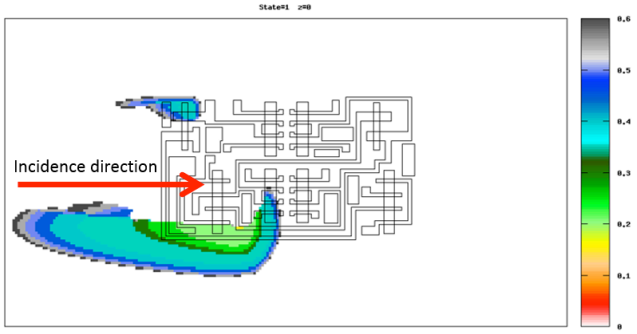


Figure 10: hardened structure with layout optimization: layout projected cross section for state0 tilt 80.4° rot 180

As shown on the Figure 11, for a given LET and position, the solid angle for which the structure is sensitive is reduced by putting distance between sensitive node couples.

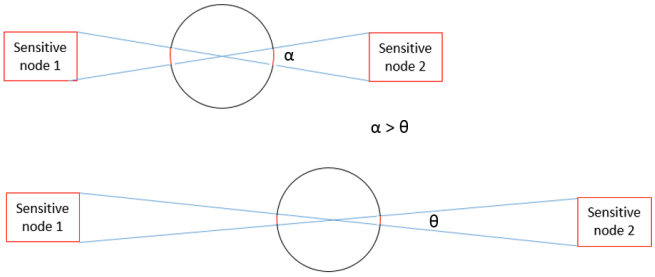


Figure 11: angular cross section dependency with sensitive nodes couple distance

VI. Measurements

The unhardened SRAM and the hardened SRAM were tested. The radiation tests were performed at the Cyclotron Resource Centre located in the Université Catholique de Louvain (UCL) at Louvain-la-Neuve, Belgium. We used their Heavy Ion Irradiation Facility (HIF).

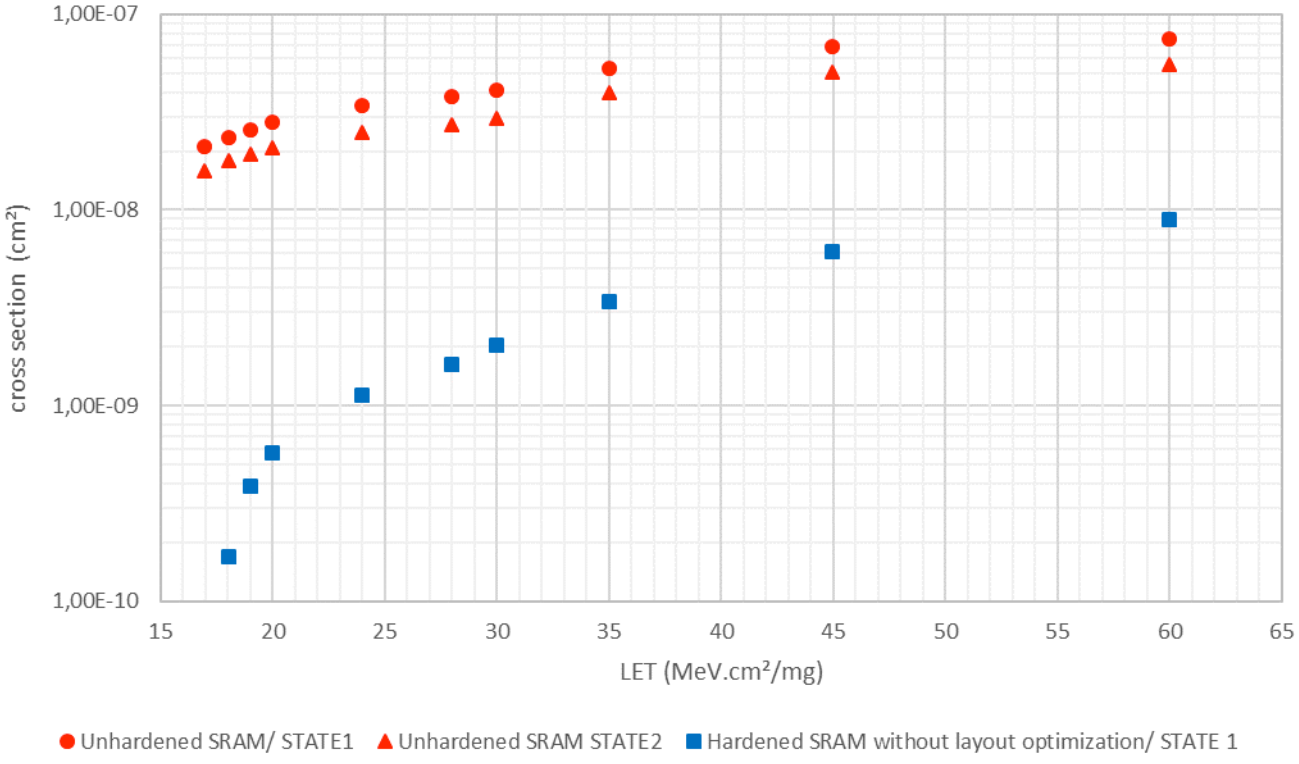


Figure 12: Simulation results of SEU normal cross section

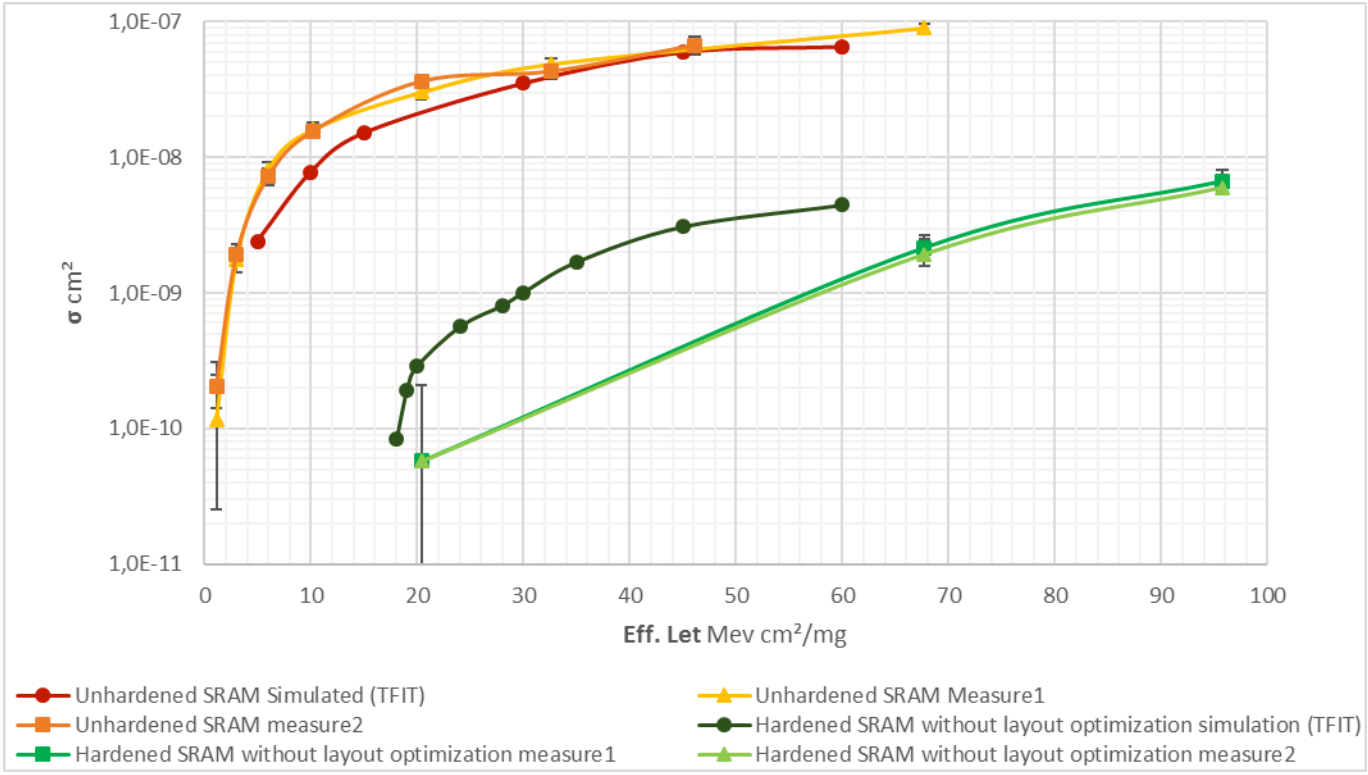


Figure 13: Measure and simulation results of normal cross section (average of the 2 states)

Figure 13 shows a good fitting between measurement and simulation for the 6T unhardened SRAM

At a LET of 60MeV.cm²/mg the two state average simulated cross section is divided by 15 for the hardened structure regarding to the unhardened structure; the reliability improvement is confirmed by the measure that show that the cross-section is divided by 40 for a LET of 67MeV.cm²/mg. The gap between measures is due to dependency with tap distance that can vary in the layout while TFIT considers a tap distance of 2μm for each transistor.

The Hardened SRAM with layout optimization will be measured in the next campaign.

CONCLUSION

In order to improve the reliability of our FPGA in radiative environment, we developed a hardening methodology and applied to one of the configuration SRAM. The first step was on the structure choice. Using the redundant DICE structure, it was measured, during the radiative tests, that the cross section was reduced by more than 40 for LETs between 0 and 60MeV.cm²/mg. An additional improvement is done on the layout by moving the sensitive diffusion couple away from each other and by placing junctions that help retain data, between the sensitive ones. This last improvement will be measured in the next campaign.

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