First S-Band Capable Dual 12-bit 1.5 GSps ADC in Flip-Chip Hermetic Technology

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Abstract

In partnership with CNES, a new ADC has been developped to meet the high dynamic range as well as channel integration requirements of telecommunications payloads.

It is a dual channel single core 12bit 1.5GSPS designed by e2v on ST Microelectronics BiCMOS9 technology which features 0.13μm CMOS and SiGeC NPN HBT bipolar technology (Ft/Fmax = 166/175GHz).

The device is built in a hermetic flip-chip package using Aluminum Nitride material in order to reach optimized thermal performance and higher pin density.

A new European Flip-Chip assembly line is being used for this device.

I. CONTEXT

The challenge of telecommunication payload manufacturers is to respond to the demand of telecom operators in terms of flexibility and performance. Those requirements are reached thanks to Digital Transparent Processors (DTP) architecture whose performance is highly dependent on analogue-to-digital (ADC) and digital-to-analogue (DAC) converter performance.

Furthermore, in order to enlarge product acceptance and profitability, e2v is looking for synergy with adjacent markets such as Defence and Industrial ones. e2v ambitions to be the leader in Europe and world-wide in developing and manufacturing such converters, giving Europe a strategic independence for such key components.

This drives the context of developing a new ADC able to meet high dynamic range and high bandwidth as well as channel integration requirements of telecommunication payloads and defence applications, in partnership with the French Space Agency (CNES) [1] and French Department of Defence (DGA). It is a dual channel single core 12-bit 1.5 GSps ADC based on ST Microelectronics BiCMOS9 technology featuring 0.13 μm CMOS and SiGeC NPN HBT bipolar technology (Ft/Fmax = 166/175 GHz) [2].

II. MARKET NEEDS

This new device targets primarily telecommunications payloads and earth observation synthetic aperture radar (SAR) payloads such as the Sentinel-1 series and similar programmes.

Future generations of telecommunications payloads aim to make intensive use of antenna array techniques for more flexibility through dynamic beam control (dynamic beam focus, power adjustments, TDMA beam hoping) [4], [5], [6]. This ADC has been designed with features such as chained synchronization to further extend the electronically steerable antenna array capabilities using software beam control.

SAR payloads such as Sentinel-1 operating in C-band ([7], [8]) can take advantage of this ADC input bandwidth for direct digitization of the SAR signals without the use of frequency down-conversion.

III. PRODUCT OVERVIEW

The device is built on two kinds of packages using flip-chip assembly for higher pin density and better RF performance.

EV12AD550A is a dual 12 bit 1.5GSps ADC featuring low latency LVDS parallel output with a built in selectable 1:2 or 1:1 DEMUX to compromise between power consumption and ease of interfacing. It is built into a hermetic package realized in Aluminum Nitride (AlN) material in order to reach optimized thermal performance and comply with ESCC9000 quality grade level.

EV12AD500A is a dual 12 bit 1.5GS/s ADC featuring selectable serial output on 4 (or 2) lanes per ADC core, with a data rate at twice the master clock rate, or a selectable parallel output LVDS in 1:1 mode. It is built in a non-hermetic ceramic package realized in High Temperature Coefficient of Expansion (HiTCE) by Kyocera [3]

The two channels can operate in phase or in opposition, thus allowing synchronous or interleaved sampling. Each channel is composed of a single core ADC sampling at up to 1.5GSps. Based on an innovative architecture without interleaving, it provides high spectral purity. It offers an analog input bandwidth of up to 4.3GHz with 2 selectable configurations to optimize SNR performance when working in lower Nyquist zones or linearity performance in higher Nyquist zones. It also features a novel synchronization method to ease the synchronization of a large number of ADCs. The device is controlled through an SPI interface. All sensitive areas of the device have been triplicated to increase

robustness. This includes, but is not limited to, clock circuitry and SPI registers.

Both the EV12AD550A and EV12AD500A are based on the same die but they offer different data output options as well as different package.

This paper will focus on EV12AD550 ADC (cf. Figure 1) which is dedicated to space applications with hermetic package.

Figure 1: Picture of EV12AD550 (before and after hermetic sealing)

IV. FEATURES AND TARGETED PERFORMANCE

- Dual channel 12 bits 1.5GSps ADC
- Single core architecture ADC
- Differential analog input voltage: 1Vppd
- Full Power Input bandwidth (-3dB): 4.3GHz
- Differential clock input
- Power consumption: 2.3W / channel
- Power supplies: Single Rail 3.4V or Dual rail 3.4V/2.5V
- Output interface: LVDS DEMUX 1:1 or 1:2
- Package: Hermetic CCGA323 21x21mm / 1mm pitch, Aluminum nitride material, Six Sigma columns and LGA.
- SPI configuration with space protection control.
- Multiple ADC chained synchronization.
- Test mode: ramp, flash, PRBS.
- Control bit: parity, in-range, trigger.

PERFORMANCE

- 4.3GHz analog input bandwidth (-3dB)
- 50 dB measured NPR over 1st Nyquist
- 48 dB estimated NPR over 3rd Nyquist
- 71 dBFS SFDR at 100MHz, -1dBFS
- 73 dBFS SFDR at 1900MHz, -8dBFS
- 73 dBFS SFDR at 3730MHz, -12dBFS
- TBD SFDR at 5300MHz, -12dBFS

V. SYNCHRONIZATION OF MULTIPLE HIGH-SPEED DATA CONVERTERS

A novel method for synchronizing multiple data converters is proposed. It is based on a daisy chain approach between data converters and one or multiple processing units, i.e. Field Programmable Gate Array (FPGA) or Application Specific Integrated Circuit (ASIC). A synchronization pulse is propagated between data converters. The Figure 2 shows a diagram of the interface between multiple data converters and a processing unit.
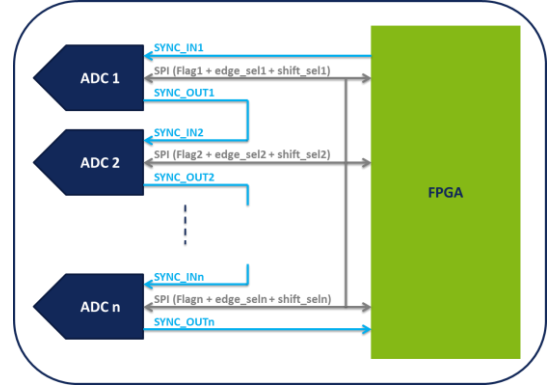

Figure 2: Multiple-device synchronization system overview

Three settings are necessary to manage or configure each ADC:

- Flagx: this signal indicates whether the synchronization pulse is in a meta-stability zone in regards to the clock of the data converter;
- Edge_selx: this signal is configured to choose which edges of the clock of the data converter is used to recover the synchronization pulse;
- Shift_selx: this signal is configured to add a certain number of clock cycle delays to the synchronization of the device after the pulse has been recovered by the data converter

The SYNC_OUT is a copy of the SYNC_IN that is sampled on the reference clock common to all data converters to ensure repeatability of the timings between power-ups and each time the synchronization process is started. Using the three settings, and a training of the system, the different data converter can be synchronized.

Calibration procedure and first measurement results are shown in [9].

This synchronization process brings multiple advantages to systems having very large count of channels:

- The parameters are accurate between power-ups, synchronization process and printed circuit board based on the same design. This is useful to develop industrial scale system, as the determination of the parameters can be done during prototyping only;
- This method relaxes all layout constraints on the SYNC signal. This means that it can be propagated on one board, or between multiple boards through a backplane which is unavoidable when systems have hundreds of channels to synchronize;
- This method is also compatible with different implementation. The daisy chain shown in Figure 2 is one of them but a tree configuration is possible as

well as any hybrid between the two. This brings flexibility to the system;

- Finally, this method does not impact the sampling clock performance. This is essential as some synchronization method adding delays on the sampling clock can degrades its jitter and thus degrade the SNR (Signal to Noise Ratio) performance of the data converters. Communication and wideband radar are two applications which performances are limited by SNR.

In terms of limitations, there are still layout constraints on the reference clock that needs to be time aligned at the input of all the data converters which is not easy to achieve. However, method exists to help either through digital processing or using a slow reference and PLLs to generate the fast clock fed to the high-speed data converters.

Speed wise, this method is limited by the setup and hold time and jitter achievable compared to the reference clock.

VI. Package technology

For EV12AD550, the option of FlipChip technology appeared naturally. The benefits of flip chip are very interesting in terms of performances, package size, thermal dissipation through top of lid and Thermal Interface Material(TIM). Also, hermeticity was mandatory and hermetic flip chip qualification had never been qualified before in Europe. In addition, standards are required for Space applications.

e2v is a key player in Europe acting as prime contractor of a cooperative project to develop a European Flip Chip hermetic assembly process (cf. Figure 3) in collaboration with Thales Alenia Space, ATMEL, AIRBUS and funded by ESA. also e2v works with other European partners on the evolution of the ESCC9000 and ESCC2269000 to take into account specific requirements of hermetic FlipChip assembly process [10]. As a consequence, EV12AD550 has been developed using flip-chip assembly technology to improve performance and size (cf Figure 4 and Figure 5).

Aluminum Nitride (AlN) material has been chosen in order to achieve the best possible thermal performance with Rth < 4°C/W and only 4.7°C/W from junction to soldering joints, and reduced thermal expansion mismatch between silicon and substrate. The selected supplier of AlN material for EV12AD550 is Kyocera.

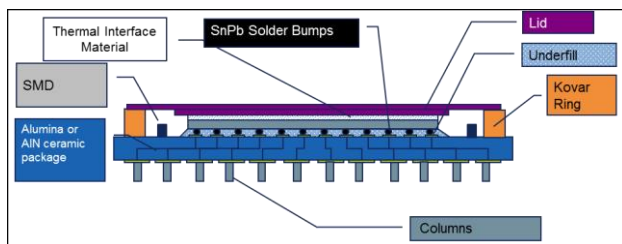Extensive RF and electromagnetic simulations have been performed to secure the target performances.

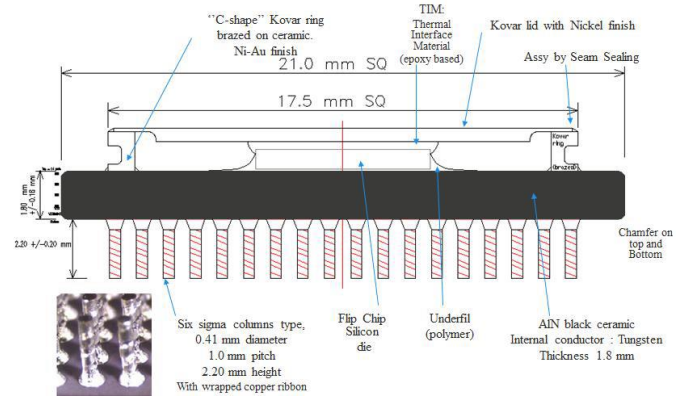

Figure 3: Hermetic FlipChip Package drawing for space

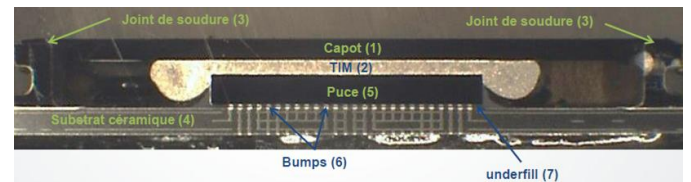Figure 4: EV12AD550 Package drawing cross section

Figure 5: EV12AD550 Package cross section

VII. Radiation hardening

ST BiCMOS9 technology does not propose rad hard library. A radiation campaign performed on a similar product - same type of product designed in the same technology and using a similar architecture - without any design rad hard protection has allowed giving a first level of confidence in intrinsic technology and architecture robustness.

Designing EV12AD550 a lot of special cares both in product architecture, cells designs, layout implementation have been done in order to either limit the impact of radiation event and/or decrease the event occurrence by increasing the required critical charge threshold to trig an event.

A. Layout for radiation considerations

Specific implementation rules have been defined and adapted case to case to limit ionization leakage current propagation into parasite path.

Some examples of adopted rules:

- NMOS transistor isolation with a P+ guard ring.
- Bulk tie have largely been implanted in order to limit leakage current between transistors.
- Minimization of bulk resistance by placing bulk tie as close as the active device.

For the prevention of latchup, special rules as the following have been used:

- A deep NWELL NISO is used to isolate the digital blocks (cf. Figure 6).
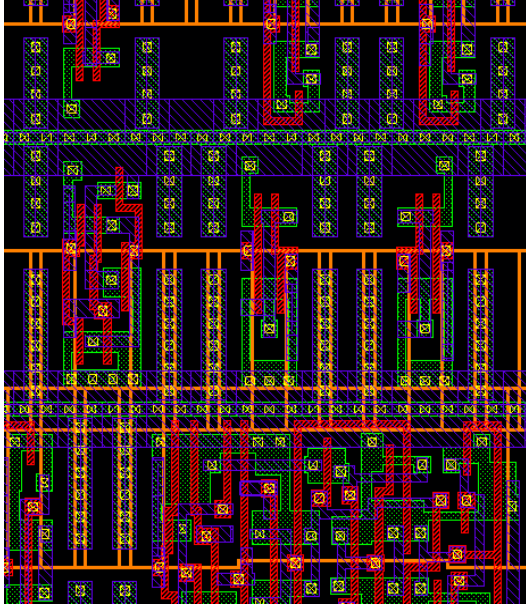
Figure 6: Detail of digital block circuit

- Enlarge minimum space between p and n zones in all analog part by adding deep trench isolation, isolated bulk including rail power supplies.
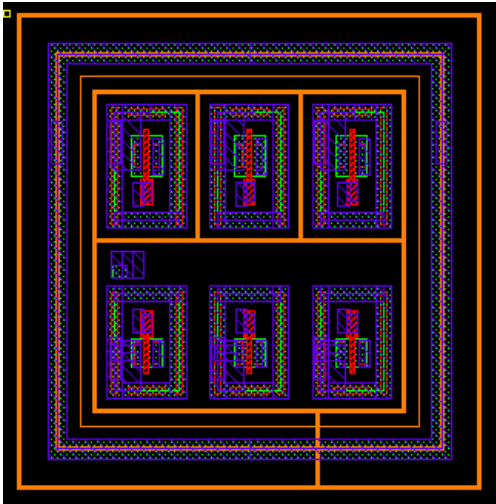

Figure 7: Detail of analog block circuit

- Reduce the serial resistance of the parasite thyristor to prevent from activation.
- Multiply the number bulks and substrates ties
- Larger of guard ring should not be too much resistive ie it is mandatory to not open them.
- Increase minimum distance between guard ring.
- Between NWELL and PWELL it is necessary to put a double guard ring connected to VDD/VSS.

Specific tools such as DRC (Design Rules Check, fault injection,…) have been developed by e2v for superior automation.

B. Design protection approaches

Design protection techniques to prevent occurrence of events include: large drive current of transistors, large transistors, large capacitance.

1) Analog architecture

When possible, analog redundancy has been used. That consists of parallelizing "n" times a circuit and connecting replicated nodes to a common node. So that the perturbation effect is divided by "n".

Analog Filtering is recommended to reduce SET. In order to increase node time constant and then increase the parasite critical charge required to produce a SET, Miller capacitance and/or resistance have been used.

2) Digital architecture

The protection of digital blocks is one of the most challenging topics as no rad hard library are available. In addition to the layout protection listed above, architecture will be optimized by implementing:

- TMV (triple redundancy voting)
- Antiglitch structure.
- A special mode (SE Protect) has been implemented to strengthen the radiation immunity to Single Event Functional Interrupt (SEFI).

However the drawback of all those protections is that they constrain the performances in terms of power consumption, speed, and size. That is why a specific study has been done on each block in order to protect the most critical nodes.

VIII. MEASUREMENTS

In this section we present some of the measurement results in terms of electrical performance and radiation test results.

A. Electrical performance highlights

Achievements of targeted performance are demonstrated in the figures below (cf. Figure 8, Figure 9, Figure 10, Figure 11). These measurements have been made on first silicon run leading to conclude the design is a first time right achievement.

B. Radiation results highlights

Preliminary Total Ionizing Dose (TID) measurement results are available at dose rate of 180 Rad(Si).h^{-1}. A complete radiation test will be published on the manufacturer webpage when available [11]. No significant drift is observed up to 150 kRad (cf. Figure 12 and Figure 13).
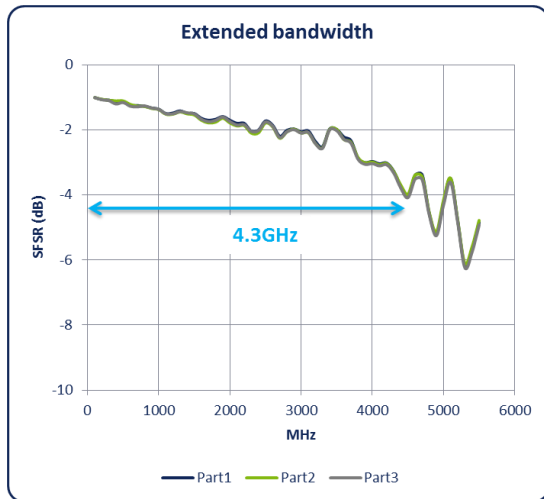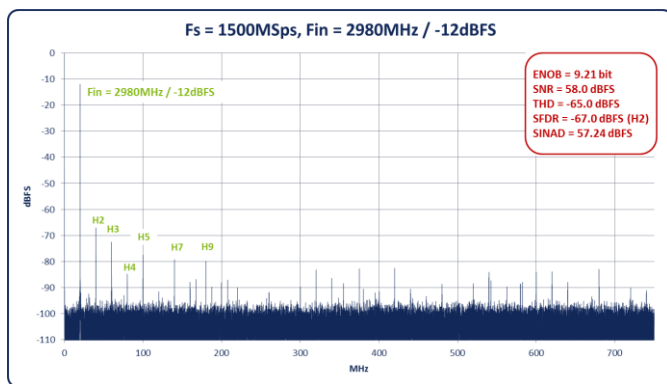
Figure 8: Analog input bandwidth

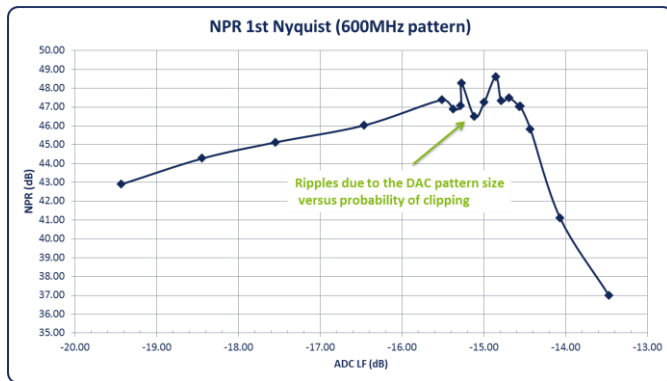Figure 9: Typical spectrum in 4th Nyquist zone

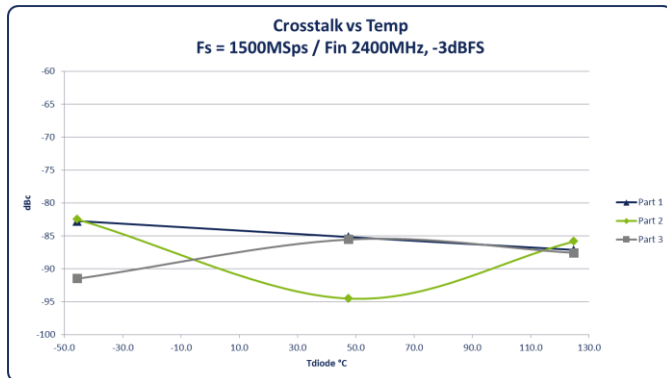Figure 10: NPR measurement in 1st Nyquist

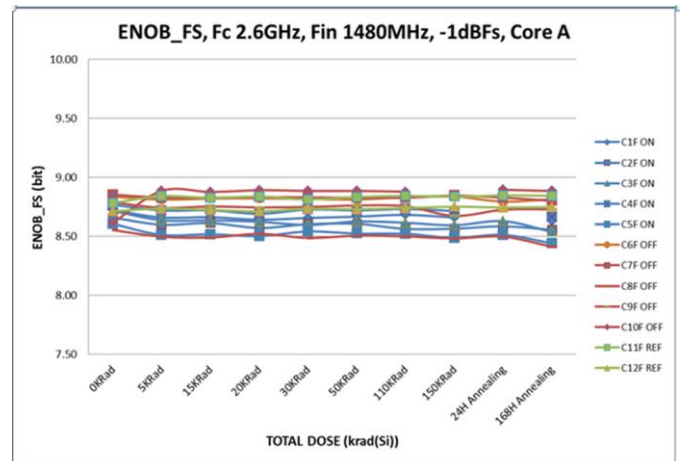Figure 11: Crosstalk measurement versus temperature

Figure 12: TID results (ENOB vs Total Dose) Fclock = 2.6 GHz
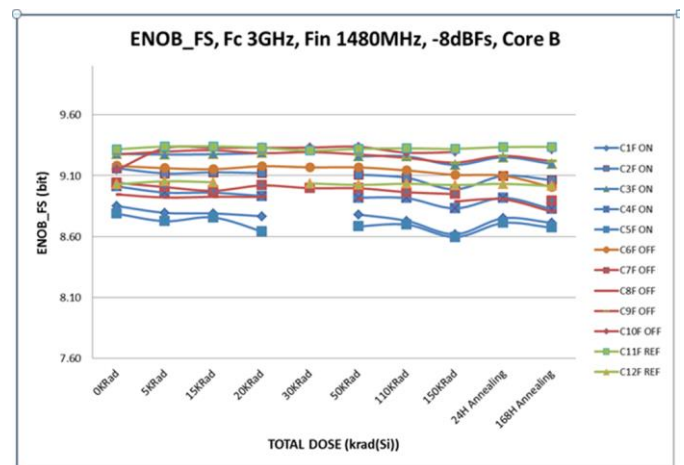

Figure 13: TID results (ENOB vs Total Dose) Fclock = 3 GHz

IX. CONCLUSION

- This product demonstrates a successful combination of innovations (hermetic flip chip in AlN, Rad Hard product on STM BiCMOS9 technology, Single rail operation, first time S-band digitization on dual channel with solid crosstalk performance in only 21x21 mm^2 hermetic package

- As of today first time right design demonstrated by early measurements on silicon.

- R&D works to reach further optimization are on-going.

- Industrialisation & ESCC evaluation and Manufacturer Qualification works are in progress.

- Performance improvement works are also expected thanks to the implementation of embedded algorithms from e2v's newly acquired Sweden-based team at SP Devices - Linköping.

X. REFERENCES

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