SpaceWire and SpaceFibre Interconnect for High Performance DSPs

S.M. Parkes[a] , B. Yu[b], A. Whyte [b], C. McClements [b], A. Ferrer Florit [b], A. Gonzalez Villafranca [b],

[a]University of Dundee, Dundee, DD1 4EE, UK
[b]STAR-Dundee, Dundee, DD1 4EE, UK

s.m.parkes@dundee.ac.uk

Abstract

STAR-Dundee with the University of Dundee has recently designed several high performance DSP units each using SpaceWire or SpaceFibre interfaces to provide an input/output performance in-line with the capabilities of the specific DSP processor.

The first DSP unit is for the High Processing Power Digital Signal Processor (HPPDSP) project, which is an ESA funded project led by AirbusDS with STAR-Dundee Ltd and CG Space. It aims to build a high performance, programmable DSP processor suitable for spaceflight applications. STAR-Dundee was responsible for the hardware, FPGA and low level software development. The HPPDSP is designed around the TI TMS320C6727B processor which is available as a space qualified part. The DSP processor connects to external SDRAM via its EMIF (external memory interface) bus. Peripherals that are directly controlled by the DSP processor are attached to the EMIF bus via an FPGA. Other peripherals that are able to access DSP memory and registers in parallel with the DSP processor are attached to the UHPI (Universal Host Processor Interface) bus of the DSP processor via the FPGA. A board has been designed incorporating the TMS320C6727 processor, SDRAM memory and a Xilinx Virtex 4 FPGA. The FPGA includes EDAC for the SDRAM memory, memory management, SpaceFibre and SpaceWire interfaces, and other general purpose interfaces. A high sample rate ADC/DAC interface is also included.

The second DSP project is a high performance FFT processor for a THz Radiometer. Implemented in various FPGA technologies this Wideband Spectrometer (WBS) is able to perform 2k point complex FFTs at a sample rate of around 2.4 Gsamples/s in radiation tolerant technology, a total processing power of more than 200 GOPS. Each FFT board processes a 2 GHz wide band to a resolution of around 3 MHz. SpaceWire is used to gather the data from several of these spectrum analysers to handle up to 12 GHz bandwidth.

The third DSP project is the Ramon Chips RC64 Many Core DSP processor, where STAR-Dundee provided the SpaceWire and SpaceFibre technology for this very powerful programmable DSP processor.

The paper focuses on the HPPDSP architecture, the FPGA design and the board design. It will give an overview of the WBS system and present the latest implementation of this high performance DSP system. A brief summary of the RC64 processor will be provided. In each case the role of SpaceWire and SpaceFibre in the different systems will be described.

I. SpaceFibre

SpaceFibre [1] [2] is a very high-speed serial data-link and data-handling network technology designed by the University of Dundee (UoD) and STAR-Dundee (STAR), which supports high data-rate payloads. SpaceFibre operates over fibre-optic and electrical cable and provides data rates of 2.5 Gbits/s in current radiation tolerant technology. It aims to complement the capabilities of the widely used SpaceWire on-board networking standard [3][4][5]: improving the data rate by a factor of 12, reducing the cable mass by a factor of two and providing galvanic isolation. Innovative multi-laning improves the data-rate further to tens of Gbits/s. SpaceFibre provides a coherent quality of service (QoS) mechanism able to support priority, bandwidth reservation and scheduling. It also provides fault detection, isolation and recovery (FDIR) capabilities. SpaceFibre enables a common on-board network technology to be used across many different mission applications resulting in cost reduction and design reusability. SpaceFibre uses the same packet format as SpaceWire, enabling simple connection between existing SpaceWire equipment and SpaceFibre. The SpaceFibre interface is designed to be implemented efficiently, requiring substantially fewer logic gates than other interface technologies like Gigabit Ethernet and Serial RapidIO. SpaceFibre is currently being prototyped and designed into a range of on-board processing, mass memory and other spacecraft applications by international prime, equipment and chip manufacturers.

II. HPPDSP

The HPPDSP processor board is shown in Figure 1 and a block diagram of the board and FPGA is given in Figure 5 at the end of this paper.

Figure 1: HPPDSP Prototype Unit

A. HPPDSP Overview

The HPPDSP board uses the TI TMS320C6727B DSP processor [6], which is Texas Instruments' high-performance 32-/64-bit floating-point digital signal processors. It has on-chip RAM and ROM as unified program/data memory, and for external memory it has External Memory Interface (EMIF) which supports a single bank of SDRAM and a single bank of asynchronous memory. The Universal Host-Port Interface (UHPI) is a parallel interface through which an external host, i.e. Control FPGA, can access memories on the DSP. The Control FPGA is a Virtex-4 device.

The DSP can boot either directly from a FLASH-based boot PROM, or over a SpaceWire/SpaceFibre interface accessing other resources on a network. The PROM stores the boot and DSP program data, which can be uploaded from a SpaceWire/SpaceFibre network. A simple Error Detection and Correction (EDAC) technique is utilised to protect data in the PROM. These functionalities are covered by the Boot Management module.

For fast access to program and data, a 32-bit wide large SDRAM memory block is attached to the EMIF interface. An EDAC function is also included, inside Memory Management module, to protect data integrity in the SDRAM memory, which is susceptible to SEU events. The Memory Management also controls which SDRAM regions are allowed for a task to access. When a task performs an access to a region which is not allowed, the SDRAM data masks are turned on to prevent further data access.

The Memory Management module has control over the DMA Bus *B*, from which it can access DSP memory via a DMA controller. It also can access the DSP peripheral Bus, which allows the DSP processor to access various memory mapped registers, along with Slave Access and Checker modules. The Slave Access and Checker Modules are used to exchange information and share memory data between the primary HPPDSP unit and the redundant HPPDSP unit when necessary. Both the Slave Access and Checker modules have access to an RMAP Initiator attached to SpaceFibre Master/Slave interface, so can start a RMAP transaction to the other unit of the Master/Slave pair.

SpaceFibre interface 1 and SpaceFibre interface 2, each have four Virtual Channels (VCs). VC0, connected to a RMAP Target accessing the Configuration Bus, is used to configure/control all modules attached to this Bus, which includes configuring the SpFi and SpW operating parameters. The rest of VCs, from VC1 to VC3, are connected to DMA Bus *A* for DMA data in-to/out-of DSP memory via the DMA controller. These two SpaceFibre interfaces can be configured to work as a prime/redundant pair to achieve dual redundancy.

The SpaceFibre Master/Slave interface has eight VCs. VC0 is used for configuration/control purposes. The rest of the VCs, from VC1 to VC7, are connected to DMA Bus *A* for sending a copy of any incoming IO data stream to the slave HPPDSP unit.

All these SpaceFibre interfaces use STAR-Dundee SpaceFibre Codec IP, which has direct interface to connect with an external serialiser/de-serialiser (SerDes) device, i.e. TI TLK2711[7] in this design.

There is a five port SpaceWire Router on the Control FPGA, with two external SpaceWire ports and three internal ports. Two of the internal ports are connected to DMA Bus *A* for DMA data in-to/out-of DSP memory, and the other internal port is connected to an RMAP Target accessing the Configuration Bus so that it can configure or control modules attached to this Bus.

There are many occasions where the Control FPGA needs to interrupt the DSP processor, for instance when a data error is detected by the EDAC circuit for SDRAM data and the error is not a one-bit error i.e. not self-correctable. All interrupts are gathered from their sources and then an interrupt signal is connected to a pin of UHPI interface which can be configured as an interrupt input pin to the DSP processor.

B. SpaceWire Router

A five port SpaceWire router is provided on the HPPDSP unit. It has two SpaceWire ports (ports 1 and 2), two ports connected to the DMA Bus *A* inside the Control FPGA (ports 3 and 4) and a configuration port (port 0) connected to the Configuration bus inside the Control FPGA. If nominal and redundant ports are required the two SpaceWire ports may each be given a nominal and redundant external LVDS driver/receiver. The SpaceWire Router is illustrated in Figure 2.

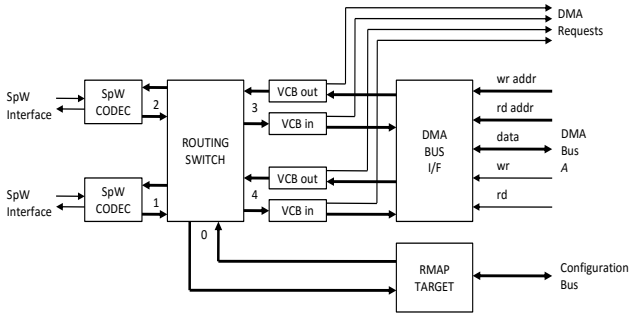

Figure 2: SpaceWire Router

The two SpaceWire interfaces are connected to a routing switch as ports 1 and 2. Ports 3 and 4 are attached to pairs of VCBs which are connected to the DMA Bus *A*. Port 0 is attached to an RMAP Target attached to the Configuration Bus. Configuration of the SpaceWire interfaces (e.g. link speed) and router (e.g. routing tables) is performed over the Configuration Bus. They can therefore be configured by any of the SpaceFibre or SpaceWire interfaces.

C. SpaceFibre Interfaces

There are three SpaceFibre interfaces on the HPPDSP. Two of them, SpFi 1 and SpFi 2, are for connecting to instruments or other HPPDSP units operating in parallel. Each of these SpaceFibre interfaces has three VCs that can be used for data transfer to/from DSP memory. These VCs are connected to the DMA Bus *A*. A fourth VC is used for configuration/control purposes and is connected to an RMAP Target that is attached to the configuration bus. The VC

attached to the RMAP Target provide a means of configuring the HPPDSP system remotely over SpaceFibre.

The SpaceFibre interfaces use external SerDes devices (TI TLK2711) which are available in space qualified version.

A block diagram of the SpaceFibre interfaces is given in Figure 3.

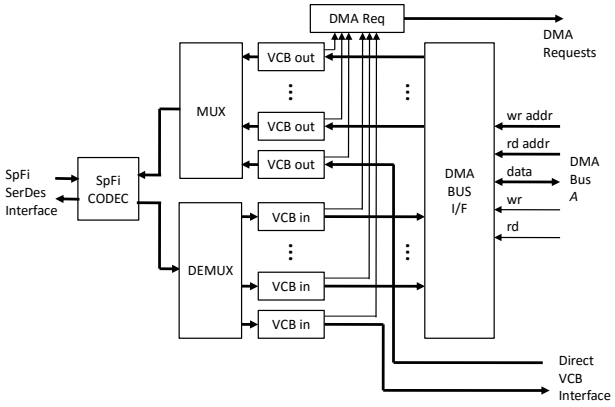

Figure 3: SpaceFibre Interface Block Diagram

D. DMA Controller

The DMA Bus interface connects the DMA Bus *A* to the input and output VCBs in the SpaceFibre interface. When writing to a SpaceFibre interface the output VCBs are addressed. When reading the input VCBs are addressed. The output VCBs are multiplexed by the MUX into a single stream of SpaceFibre data frames into the SpaceFibre CODEC. The SpaceFibre CODEC encodes the data frames, adding any link control characters that are required and passes the resulting symbol stream to the external SerDes for 8B/10B encoding and transmission. Symbols received from the SerDes device are passed to the SpaceFibre CODEC and the data frames are extracted and passed to the DEMUX for writing into the appropriate input VCB. The data in the input VCBs are taken out when the DMA Controller reads the VCB.

There is an input and output pair of VCBs that are not attached to the DMA Bus *A*. These are connected to an RMAP Target and used for configuring and controlling the HPPDSP unit.

SpFi 1 and SpFi 2 each have four pairs of VCBs (three attached to the DMA Bus *A* and one pair to an RMAP Target) and SpFi M/S has eight pairs (seven attached to the DMA Bus *A* and one pair to an RMAP Target).

The DMA Controller takes DMA requests from DMA Bus *B*, for a small amount of data access at any memory location.

The DMA Controller also manages transfer of data from the SpaceFibre, SpaceWire, to and from DSP memory. It does this under control of the DSP i.e. the DSP processor determines where in DSP memory the data is to be placed and how much data is to be read in a burst.

In a Master HPPDSP unit, the DMA Controller copies the data being read to the SpaceFibre master/slave interface. This is done at the same time as the data is being read out of one of the interface by the DMA controller by providing a concurrent write strobe and IO write address that specifies where the data is to be copied to. In this way the data is read from one of the interfaces, written to DSP memory and concurrently written to the SpaceFibre master/slave interface for transferring to the slave HPPDSP.

For Slave unit, the DMA Controller accesses the SpaceFibre master/slave interface in place of the SpaceFibre, and SpaceWire interfaces. It DMAs data from VCBs in the SpaceFibre master/slave interface as if it were coming from VCBs in the SpaceFibre, SpaceWire interface. For slave unit, if the DSP processor requests to write data to a SpaceFibre or SpaceWire interface via the DMA Controller it simply discards the information.

The DMA Controller contains several channels each channel may be programmed by the DSP processor to perform the required data transfer.

III. FFT PROCESSOR

In this section the FFT Processor being developed for the THz Radiometer is described. A block diagram of the FFT Processor is provided in Figure 4. The FFT Processor system comprises a Control Processor board and one or more FFT Processor boards.

A Control Processor which is responsible for controlling the FFT Processor, gathering data from the FFT boards formatting that data and sending it to the downlink telemetry system. The control processor board uses an ARM Cortex-M1 processor chip implemented on a Microsemi RTG4 FPGA. This FPGA comprises an ARM Cortex-M1 processor, on-chip memory, an off-chip memory interface, three SpaceWire protocol engines which offload the processor from communication intensive tasks, a SpaceWire router with eight external ports, and various other input/output interfaces including SPI. EDAC protected DDR memory will be provided on the processor board. A reference clock generator and reset distributor will be included on the Control Processor. The reference clock will be a 10 MHz low jitter reference clock. The reference clock generator will be configured by the ARM processor on the RTG4 FPGA via an SPI interface. The processor board is connected to each FFT board via separate SpaceWire link, reference clock and reset for each FFT board.

One or more FFT boards that take in analogue signals sampled by two ADC chips at 2.4 Gsamples/s and compute the power spectrum of those signals. This board is controlled by the control processor via a SpaceWire link and passes accumulated power spectra back to the control processor via that SpaceWire link. Each FFT board can be programmed to process 2 GHz bandwidth signals acquired using the two ADCs as an in-phase and quadrature pair, or to process 1 GHz bandwidth signals acquired separately as real signals from each ADC. Each FFT board contains its own voltage controlled crystal oscillator (VCXO) and clock generation/distribution chip. This allows for very low jitter

clock generation with the ADC clocks being locked to the 10 MHz reference signal from the Control processor board.

The number of FFT board can be adjusted to help trade-off bandwidth vs power consumption. The prototype system will have one FFT board owing to the cost of components.

IV. RC64

The RC64, is a novel rad-hard 64-core digital signal processing chip, with a performance of 75 MACS, 150 GOPS and 38 GFLOPS (single precision) and low power consumption, dissipating less than 10 Watts. The RC64 integrates sixty-four advanced DSP cores, a hardware scheduler, 4 MBytes of multi-port shared memory, a DDR2/DDR3 memory interface, and twelve 3.125 Gbps full-duplex, high-speed SpaceFibre serial links, four of which can also support serial Rapid IO.

The RC64 architecture is illustrated in Figure 6. A central scheduler assigns tasks to processors. Each processor executes its task from its cache storage, accessing the on-chip 4MByte shared memory only when needed. When task execution is done, the processor notifies the scheduler, which subsequently assigns a new task to that processor. Access to off-chip streaming channels, DDR2/DDR3 memory, and other interfaces happens only via programmable DMA channels. This approach simplifies software development and it is found to be very useful for DSP applications, which favour streaming over cache-based access to memory. Hardware events, asserted by communication interfaces, initiate software tasks through the scheduler. This enables high event rates to be handled by the many cores efficiently.

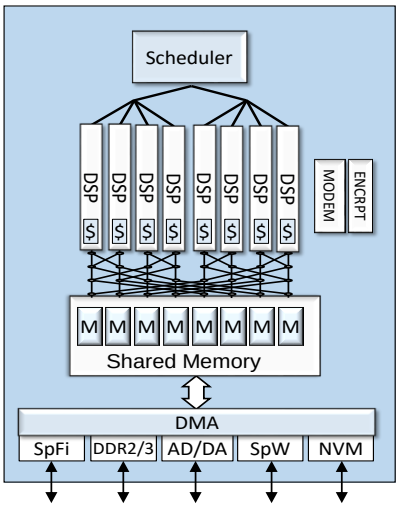

Figure 4: RC64 Architecture (only 8 DSP processors are shown)

The RC64 is implemented as a 300 MHz integrated circuit on a 65nm CMOS technology, assembled in a hermetically sealed ceramic CCGA624 package and qualified to the highest space standards. Supported communication applications include frequency multiplexing, digital beam forming, transparent switching, modems, packet routing and higher-level processing.

V. CONCLUSIONS

This paper described the use of SpaceWire and SpaceFibre to provide input and output facilities for high performance DSP systems. Three examples are provided: the ESA funded High Processing Power DSP (HPPDSP) which uses a radiation tolerant DSP from TI, a spectrometer which implements a high performance FFT in an FPGA, and the Ramon Chips RC64 Many Core programmable DSP which incorporates 12 SpaceFibre interfaces.

VI. REFERENCES

[1] S. Parkes, A. Ferrer and A. Gonzalez, “SpaceFibre Standard”, Draft H, August 2015.

[2] S. Parkes et al, “SpaceFibre: Multi-Gigabit/s Interconnect for Spacecraft On-board Data Handling”, IEEE Aerospace Conference, Big Sky, Montana, 2015.

[3] ECSS Standard ECSS-E-ST-50-12C, “SpaceWire, Links, Nodes, Routers and Networks”, Issue 1, European Cooperation for Space Data Standardization, July 2008, available from http://www.ecss.nl.

[4] S. Parkes, P. Armbruster and M. Suess, “SpaceWire On-Board Data-Handing Network”, ESA Bulletin, Volume 145, pp 34-45, February 2011.

[5] S. Parkes, “SpaceWire Users Guide”, ISBN: 978-0-9573408-0-0, STAR-Dundee, 2012.

[6] Texas Instruments, “TMS320C6727B Floating-Point Digital Signal Processors – Data Sheet,” SPRS370E, September 2006.

[7] Texas Instruments, “TLK2711A 1.6 TO 2.7 GBPS TRANSCEIVER”, SLLS908A, September 2009.

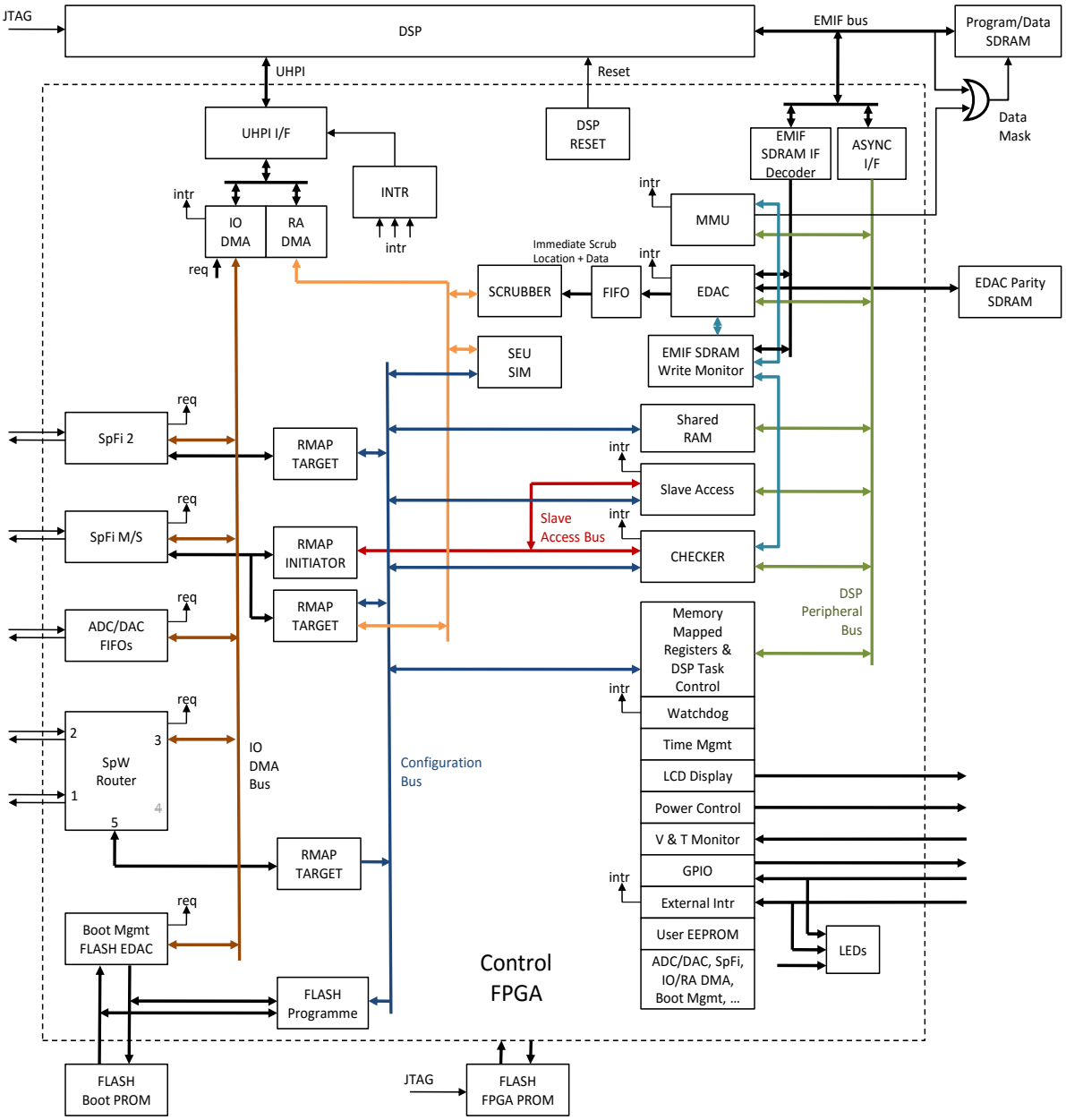

Figure 5: Block Diagram of HPPDSP FPGA Architecture

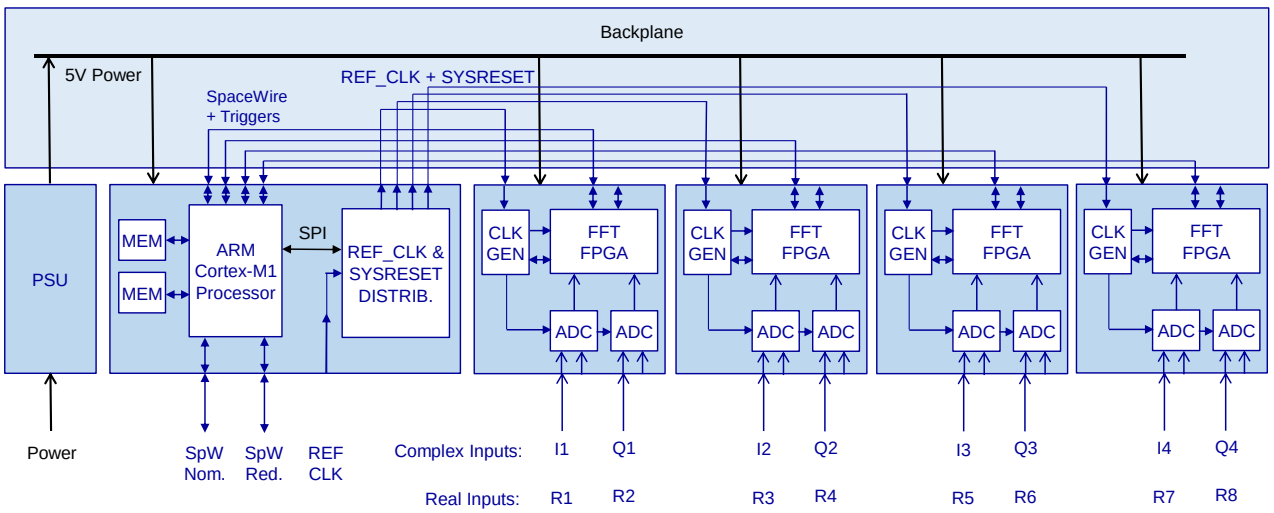

Figure 6: WBS V Architecture