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# SpaceWire and SpaceFibre Interconnect for High Performance DSPs

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- Next Generation SpaceWire: SpaceFibre
- SpaceFibre Reference Architecture
- High Processing Power DSP
- RC64
- FFT Processor
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# Next Generation SpaceWire: SpaceFibre

# Driving Applications for SpaceFibre

- High data-rates for SAR and high-resolution multi-spectral imagers require:
  - 10s Gbits/s data rates
- High performance mass memory units require:
  - Multi-Gbit/s network interconnecting memory modules
- Integrated control and payload data handling requires:
  - Deterministic data delivery for AOCS/GNC
  - Concurrent with asynchronous payload data delivery
  - Simple configuration
  - Galvanic isolation
- Space transportation and human space flight requires:
  - Long distance (100m)
  - Deterministic data delivery – safety critical
  - Carry video traffic without interfering with deterministic traffic

# Other Requirements for SpaceFibre

- Backwards compatible with SpaceWire
- Address issues inherent in SpaceWire
  - Packet blocking in networks
  - Limited common mode voltage tolerance
  - High cable mass
  - Limited maximum length
  - No quality of service (QoS)
  - No deterministic data delivery
- All these issues are resolved in SpaceFibre

# STAR-Dundee SpaceFibre

- SpaceFibre is
  - A spacecraft on-board data link and network
- SpaceFibre runs over
  - **Electrical** and fibre optic cables
- SpaceFibre designed specifically for spaceflight
  - Integrated Quality of Service (QoS)
  - Integrated Fault Detection, Isolation and Recovery (FDIR) capabilities
  - Simple configuration
- A substantial improvement on SpaceWire
  - Performance x10 to x100 (multi-lane)
  - Power per bit x0.2
  - Lower mass x0.75 electrical, x0.5 fibre per cable
  - Robustness: galvanic isolation, FDIR
  - Capabilities: virtual links, virtual networks, time distribution, event signalling, deterministic data delivery

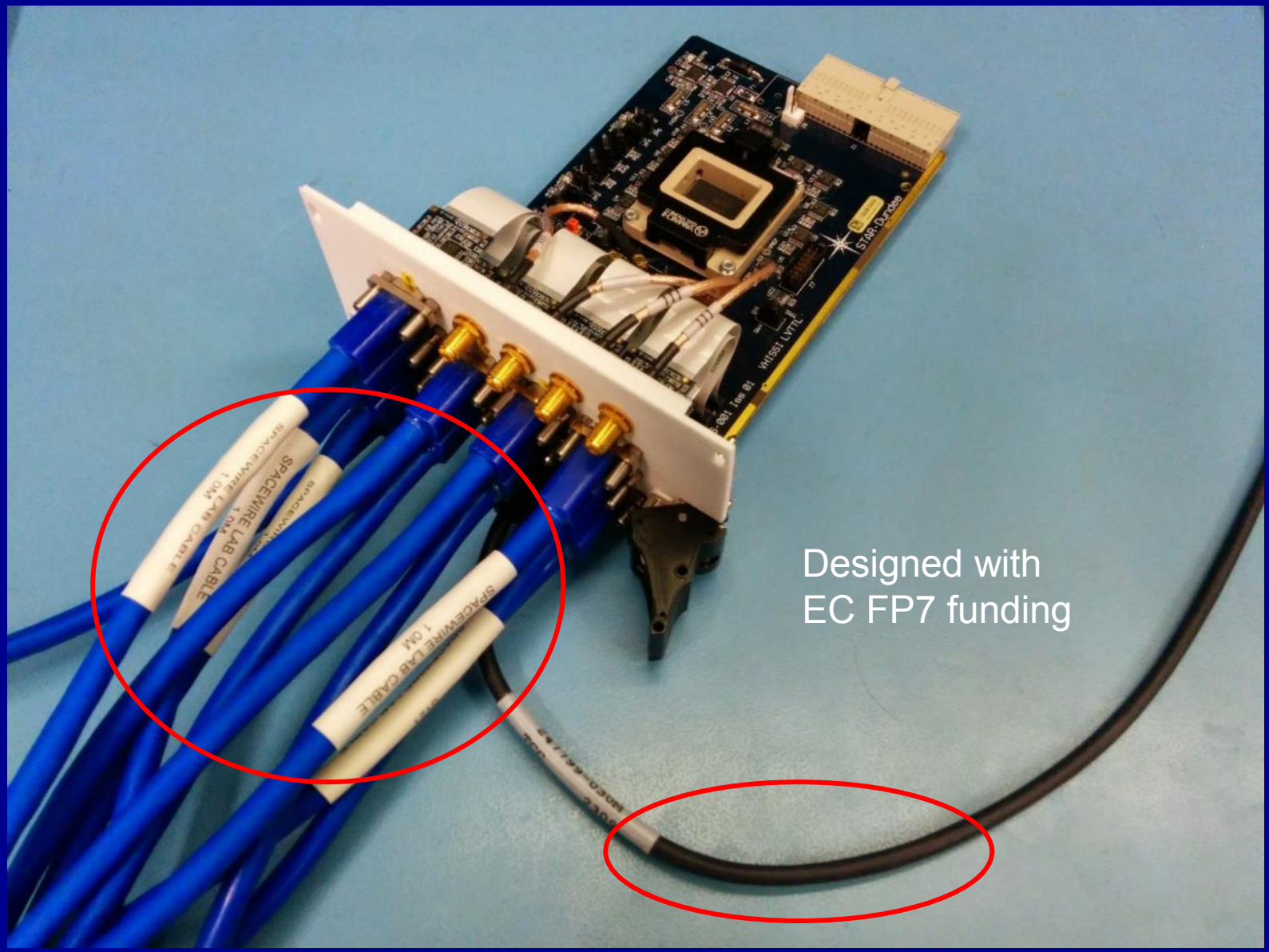
# SpaceFibre Key Features

- High performance
  - 2.5 Gbits/s current flight qualified technology
  - 3.125 Gbits/s soon (6.25 Gbits/s coming)
  - Multi-laning of up to 16 lanes (40 Gbits/s)
- Integrated QoS
  - Priority
  - Bandwidth reservation
  - Scheduling
- Integrated FDIR support
  - Transparent recovery from transient errors
  - Error containment in virtual channels and frames
  - “Babbling Node” protection
- Low latency
  - Broadcast messages
- Compatible with SpaceWire at packet level

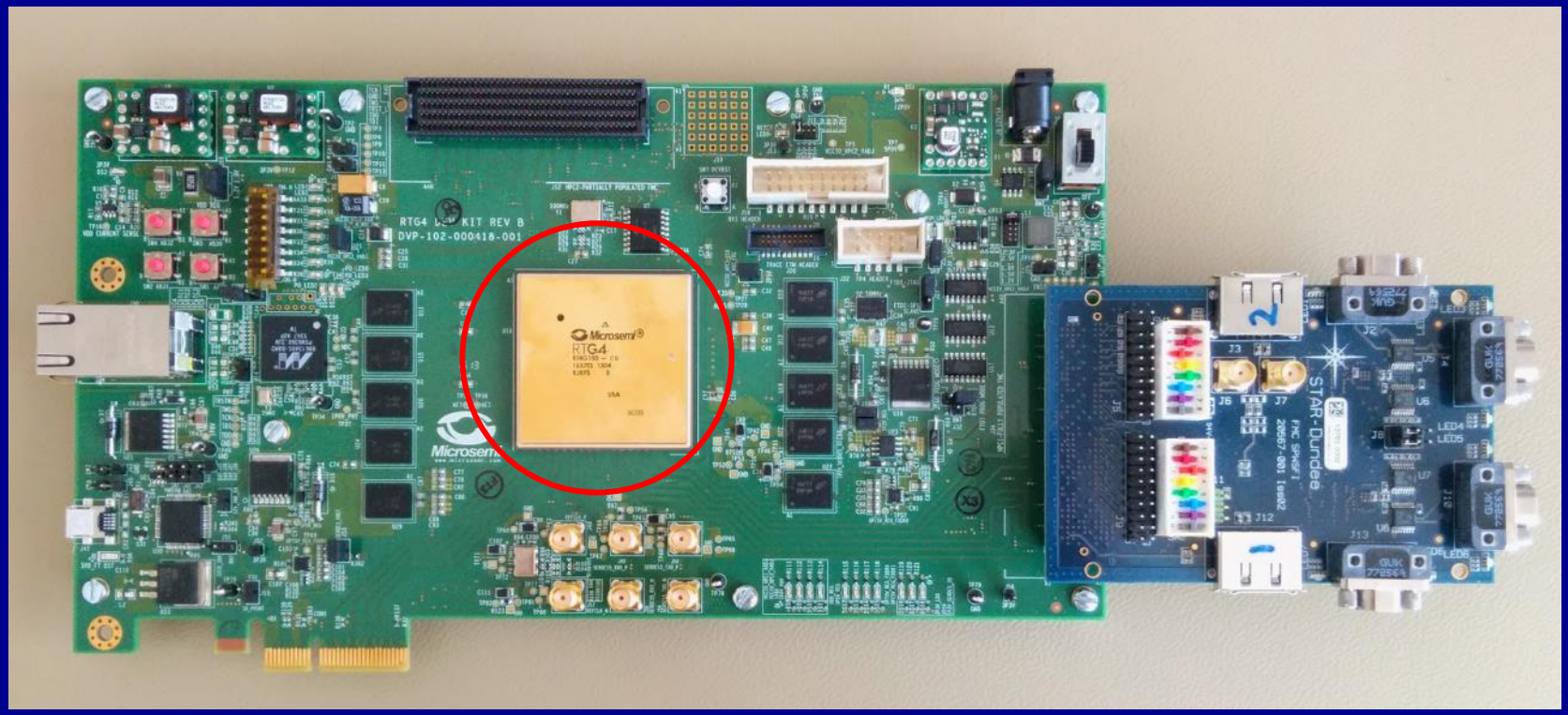
# Integrated Network

- Single integrated network
  - Carrying
    - Instrument data
    - Configuration and control information
    - Deterministic traffic
    - High resolution time information
    - Event signals
  - Improves reliability, mass, cost, reuse
  - Backwards compatible with existing SpaceWire equipment
- Ideal for interconnecting DSP units

# Radiation Tolerant SpaceFibre ASIC



# SpaceFibre on Microsemi RTG4




- RTG4: New powerful FPGA from Microsemi
- Integrated SerDes running at 3.125 Gbits/s
- Perfect for SpaceFibre
- SpaceFibre interface 3% to 6% of RTG4 (2 to 8 VCs)
- SpaceWire interface 1%, RMAP Target 2% of RTG4

# SpaceFibre Development Status

- Open technology
- Result of work from many companies
  - In different member states
  - With funding from
    - National agencies, ESA, and EC (FP7)
- ECSS standardisation ongoing
  - Out for public review 3Q2016
  - Working group with representatives from industry across Europe
- TRL 4/5 approaching 6 on radiation hard FPGAs
- IP cores available
- Ready for implementation in European chip technologies


# HPPDSP

## High Processing Power Digital Signal Processor


# Background

- High data rate payload, requiring DSP with
  - High processing power
  - High throughput
- DSP processor
  - TI SMV320C6727B-SP, 250-MHz, Floating-Point
    - Total Ionizing Dose tolerance (TID 100Krad)
    - Single Event Latch-up immune (SEL 117 MeV $cm^2$/mg)
  - 2000 MIPS/1500 MFLOPS at 250MHz
- High throughput using SpW and SpFi interfaces

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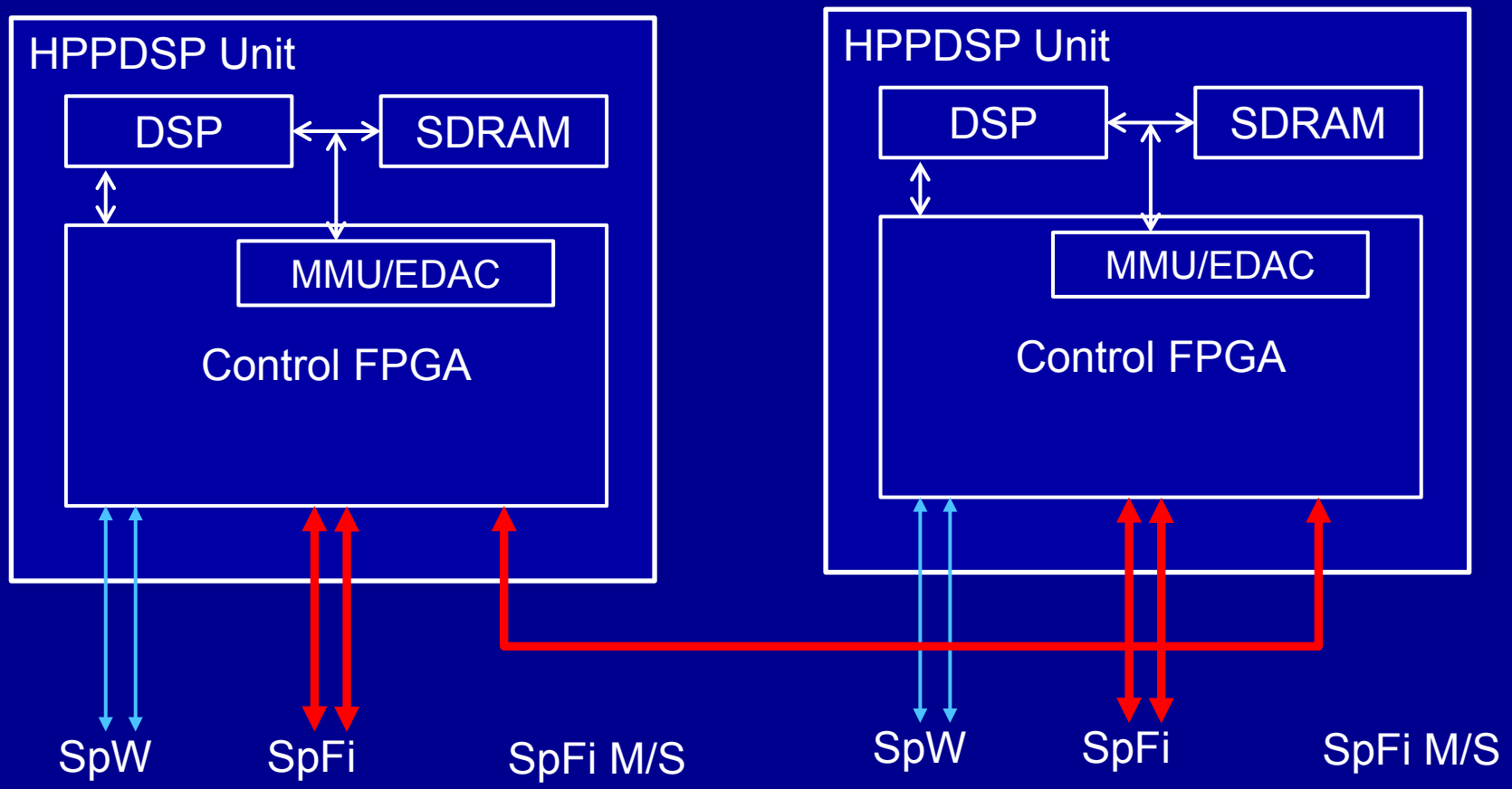
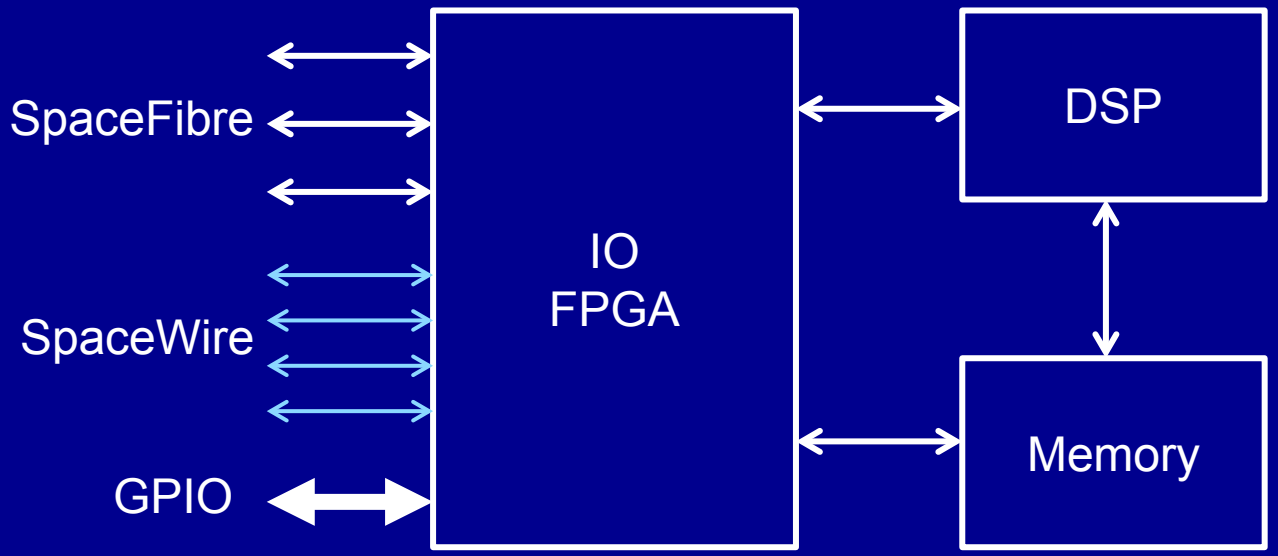
# System Architecture Design



# STAR-Dundee High Processing Power DSP

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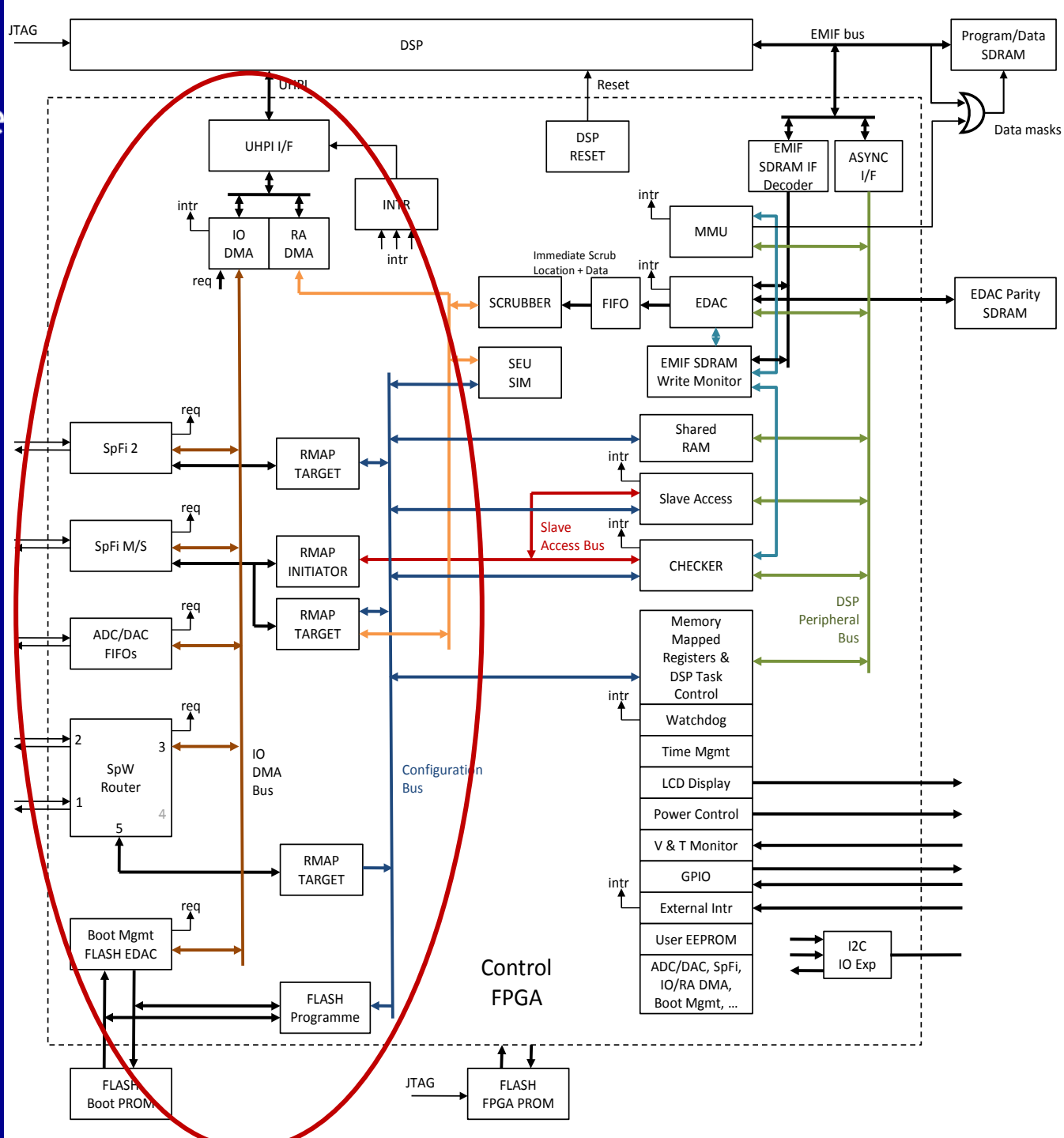
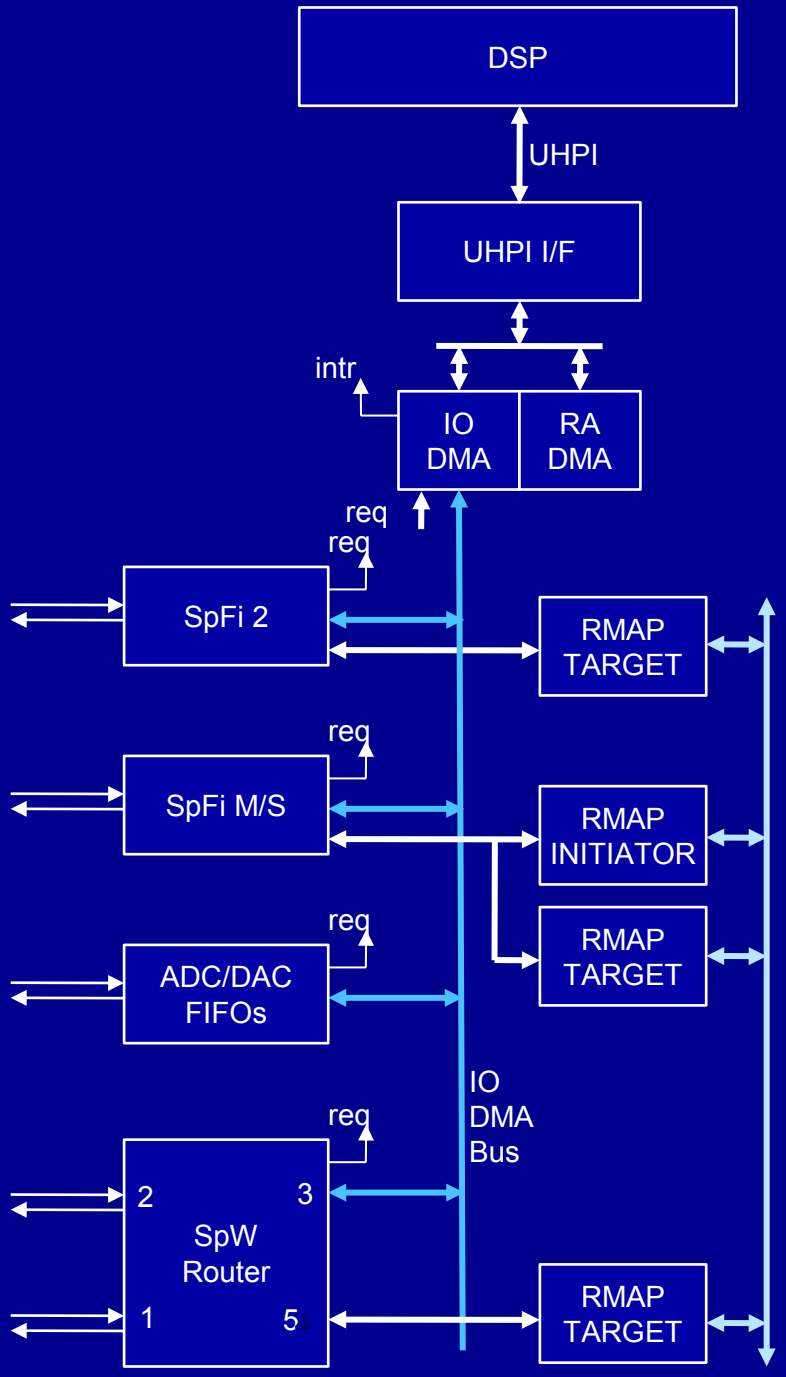
# Block Diagram of the FPGA Design



# IO DMA

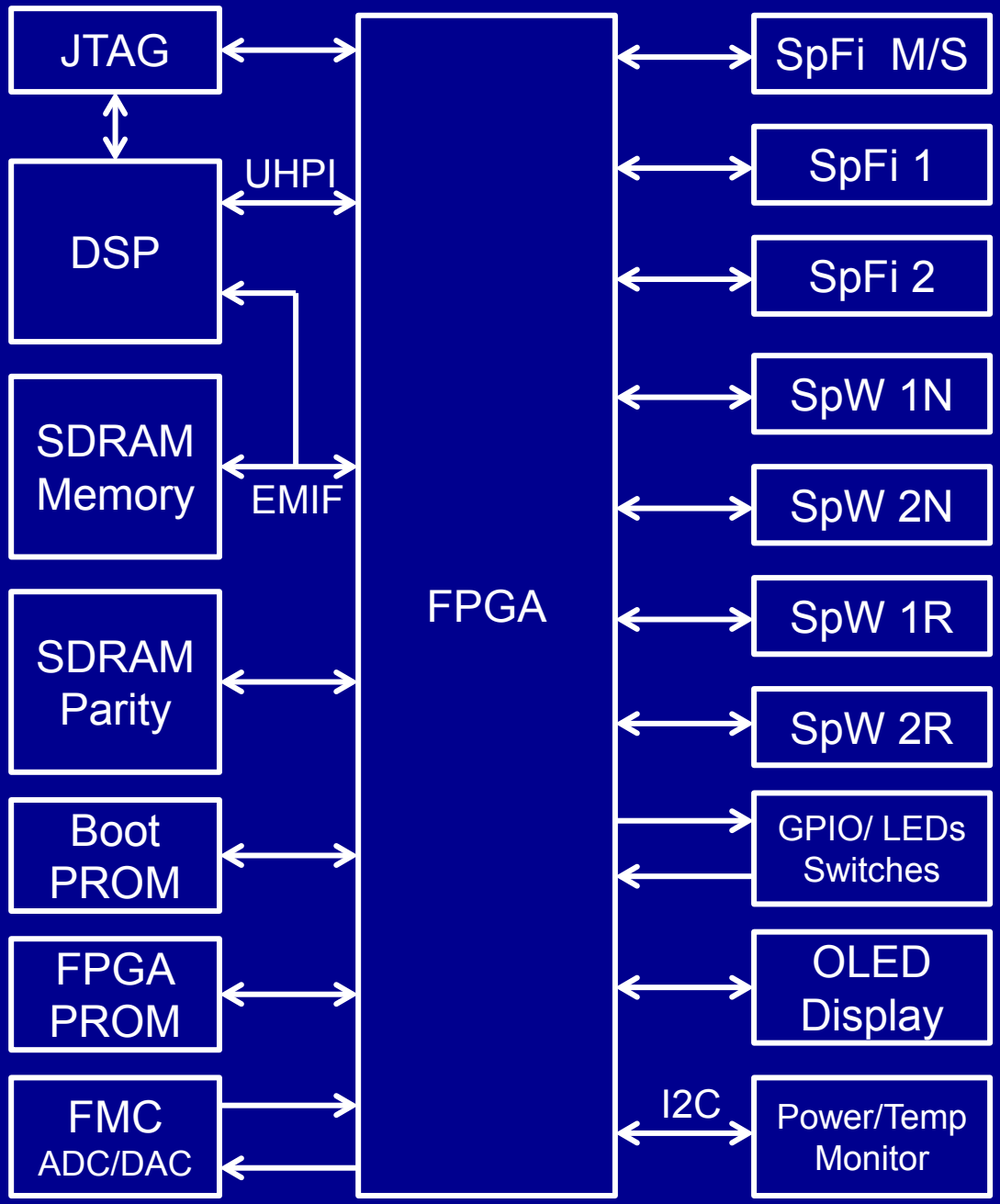
- DMA data between DSP memory and:
  - SpaceFibre
  - SpaceWire
  - ADC/DAC
- Different operations for Normal, Master, and Slave mode
- When a IO DMA is completed, an interrupt is generated
- IO DMA and RA DMA compete for access to UHPI
- Boot management also goes through IO DMA
- On master board all data transfers are copied to SpFi M/S



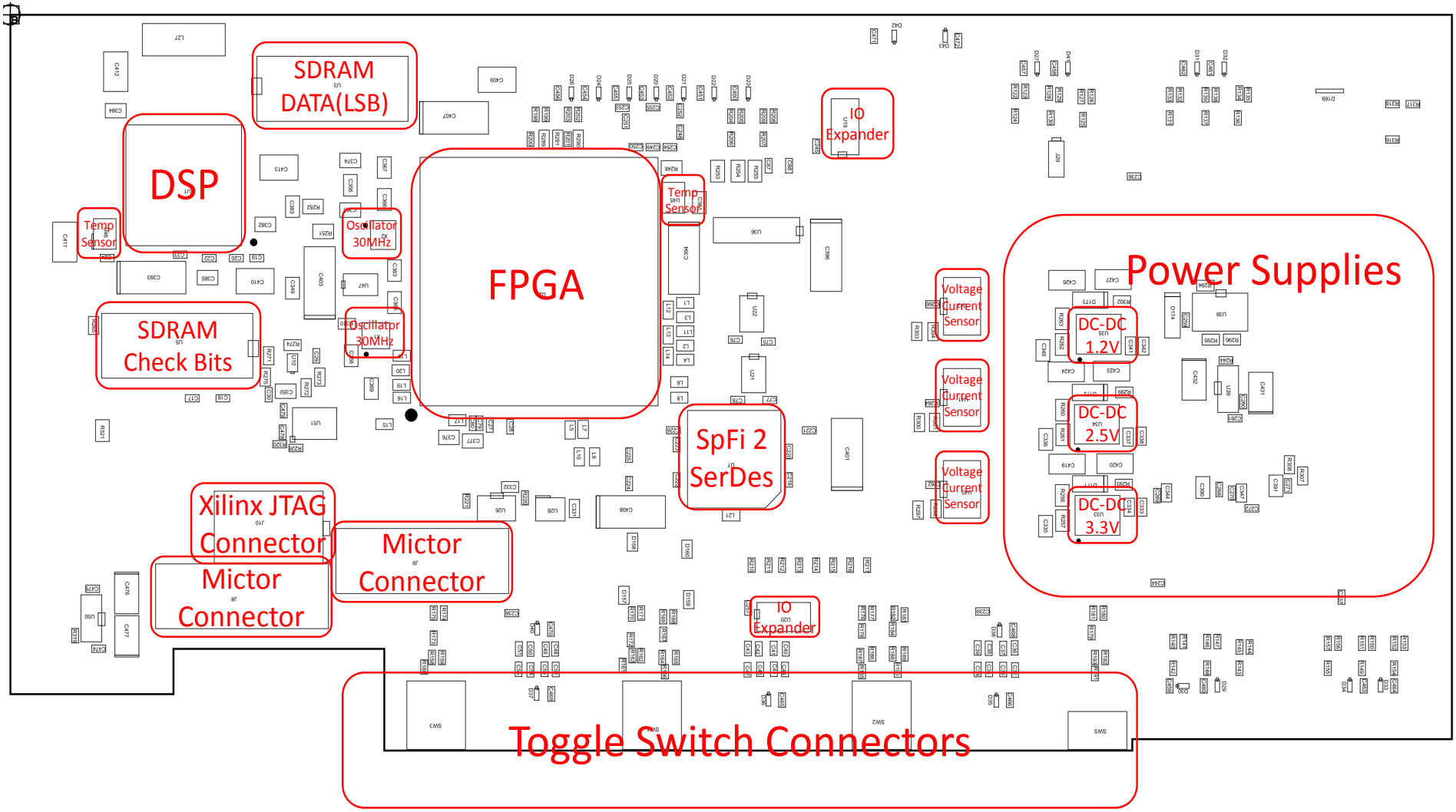
# SpaceWire and SpaceFibre IO

- SpaceWire
  - Internal SpaceWire Router
    - 2 ports to external LVDS drivers/receivers
    - 2 ports to IO DMA bus
    - 1 port to RMAP Target
- SpaceFibre
  - Two interfaces each at 2.5 Gbits/s
  - Two different SerDes (Xilinx MGT and TI TLK2711)
  - Master/Slave
    - For connecting to second HPPDSP
    - 4 virtual channels
  - SpaceFibre 2
    - For high speed IO
    - 2 virtual channels

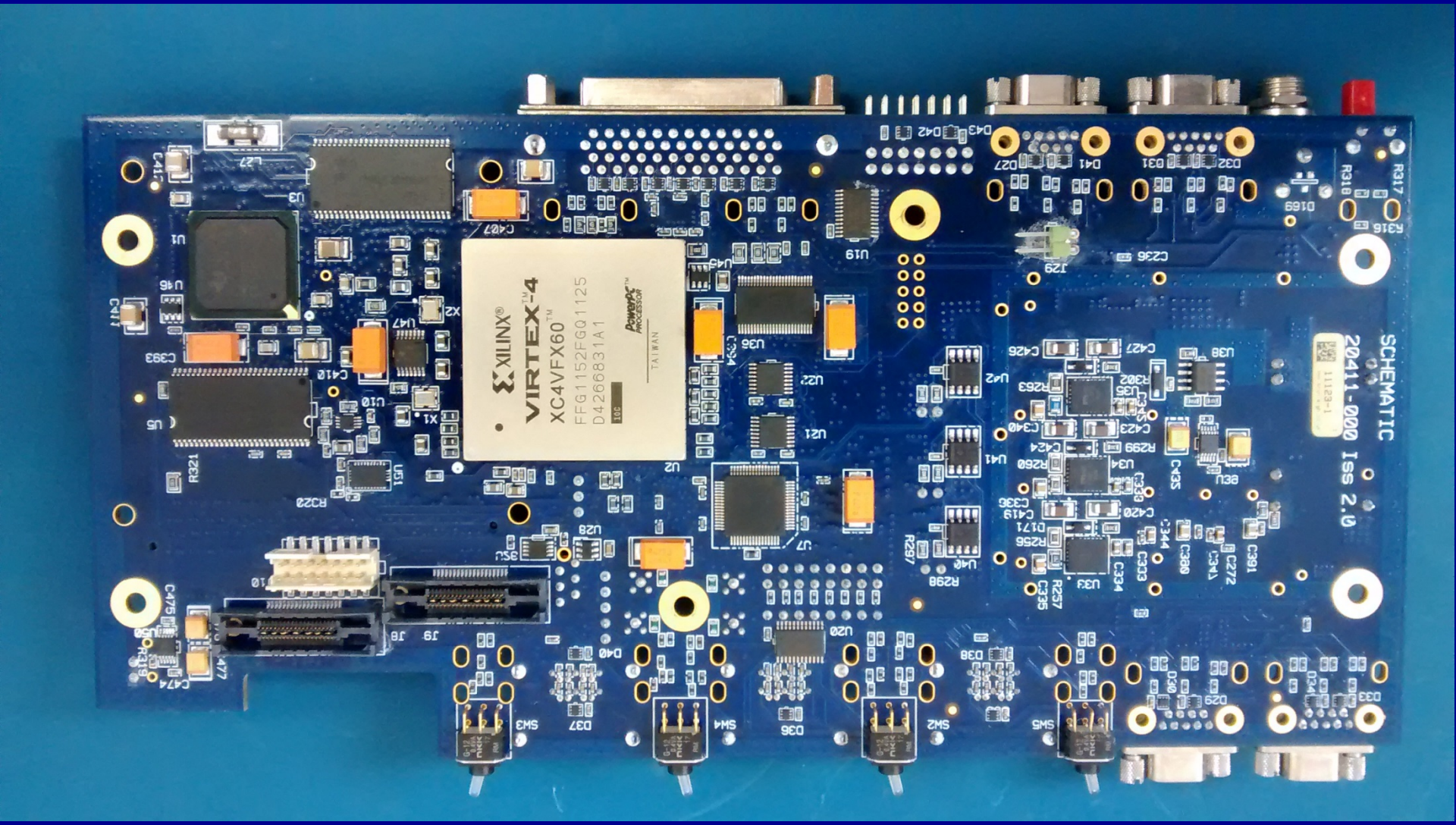
# HPPDSP Board



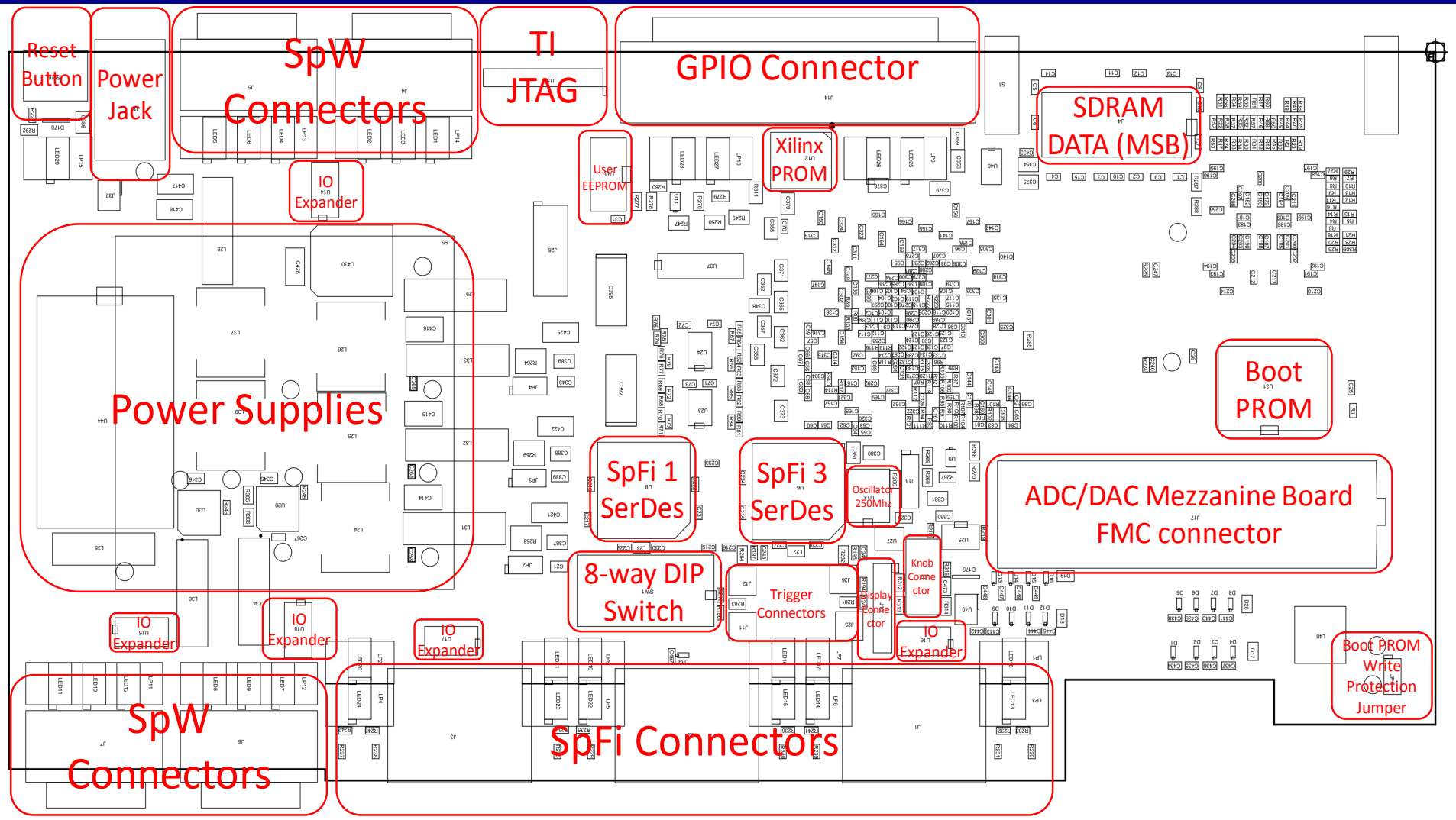
# PCB Layout – Bottom Side



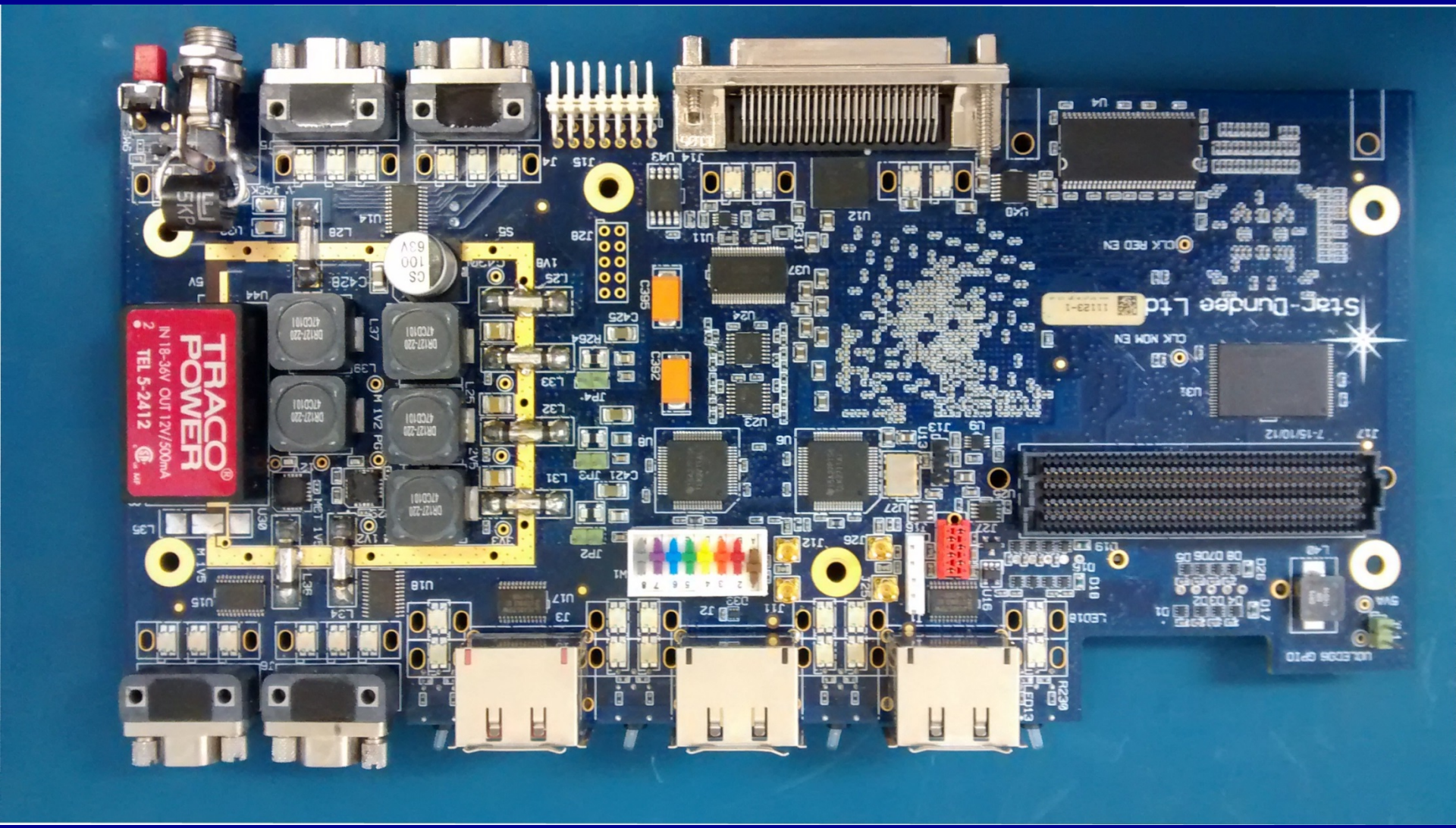
# HPPDSP – Bottom Side



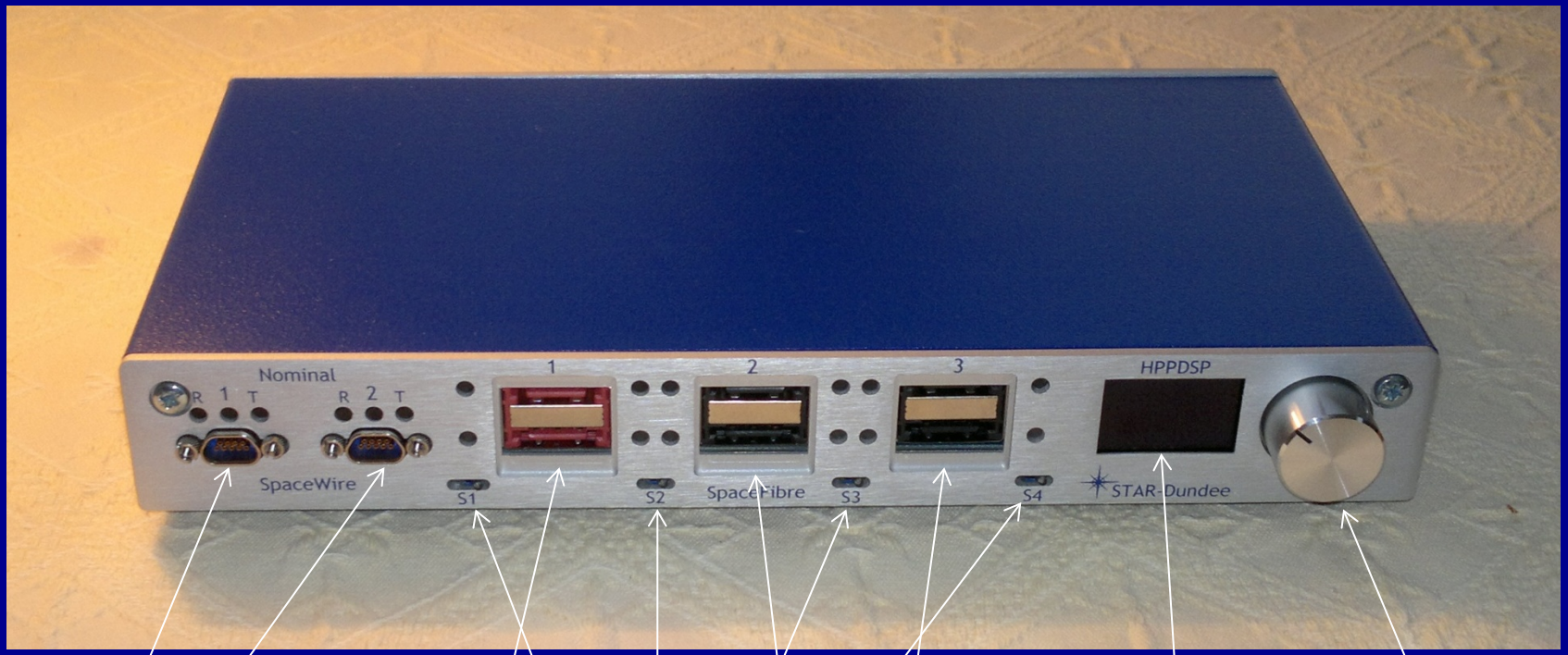
# PCB Layout – Top Side



# STAR-Dundee HPPDSP – Top Side



# HPPDSP Front Panel




SpaceWire Nominal Ports 1 & 2

SpaceFibre M/S

Switches

SpaceFibre

Display

Push Button/ Knob

# HPPDSP Rear Panel


ADC/DAC FMC Board

Triggers

GPIO

DSP JTAG

SpaceWire Redundant Ports 1 & 2

Power

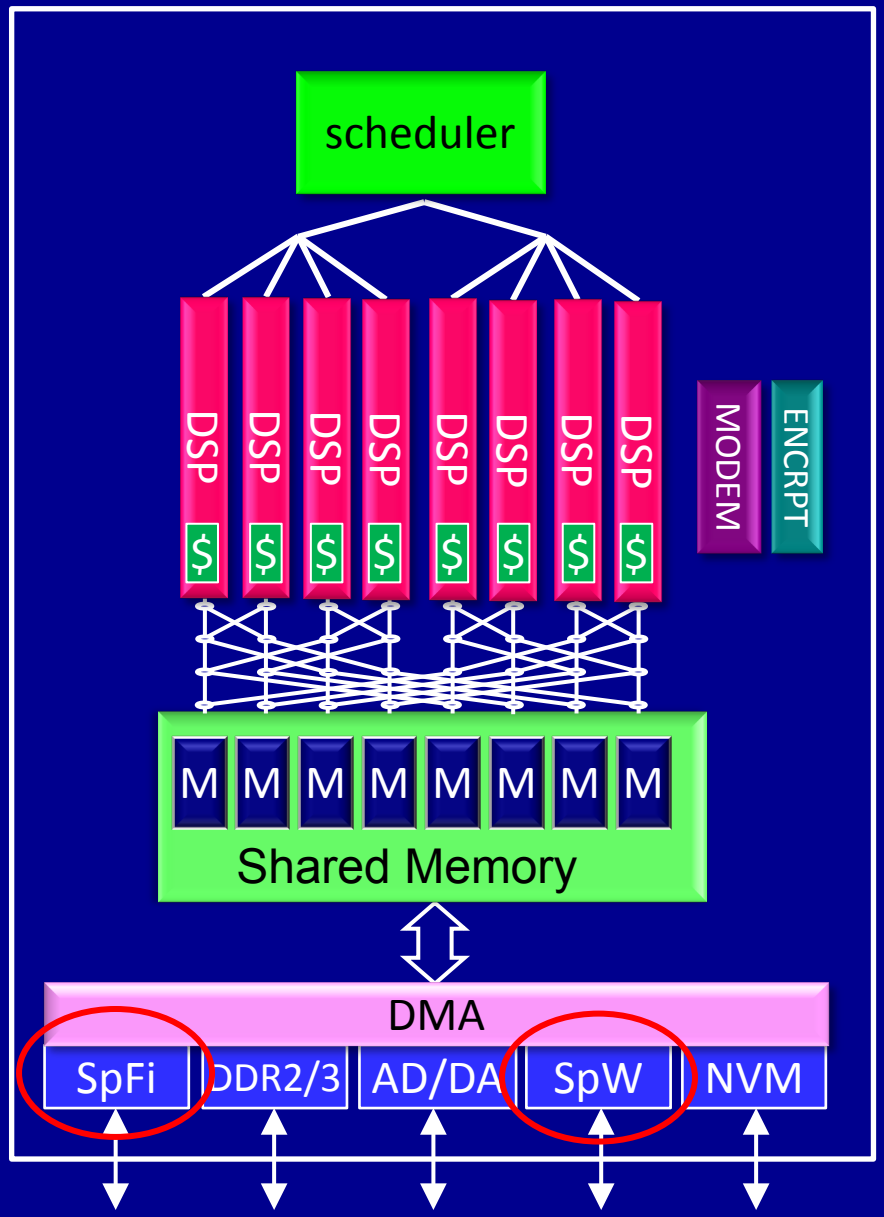
Reset


# Ramon Chips RC64

# STAR-Dundee RC64 Many Core DSP Processor

Ramon Chips

- 64 fast CEVA X1643 DSP with FP extension and HW scheduler
  - 300 MHz
  - 40 GFLOPS, 384 GOPS
- Modem and Encrypt accelerators
- 4 Mbyte on-chip shared memory
- Fast I/O
  - 12x SpaceFibre, SpaceWire
  - DDR3, AD/DA LVDS I/F, NVM
- Rad-Hard, for space
- Advanced technology
  - TSMC 65nm LP
  - CCGA / PBGA / COB
  - 10 Watt
- Modular
  - Payloads can employ many RC64
- Versatile
  - Designed for all space missions
  - Planned for 2020—2050
- Re-programmable in space

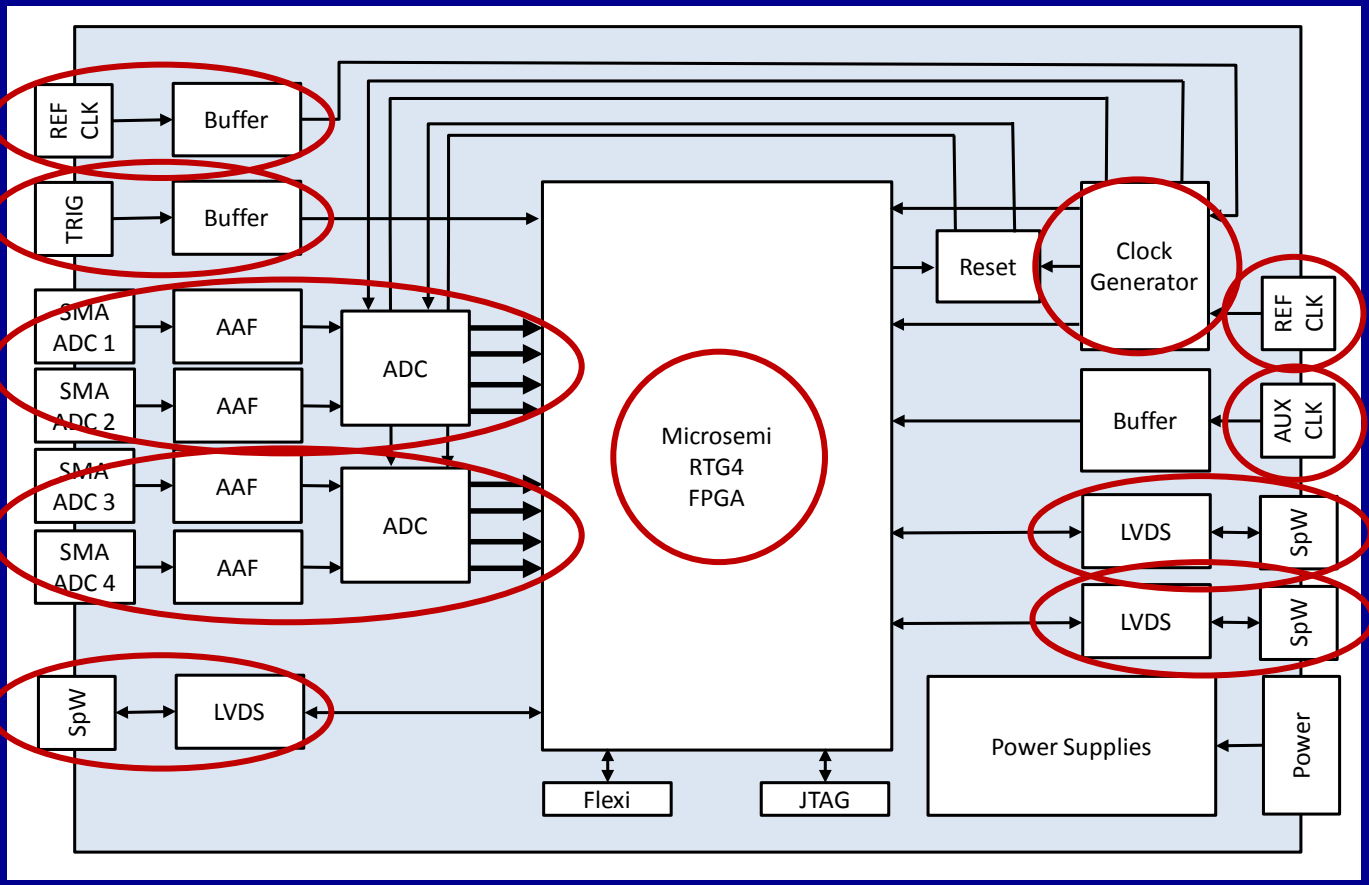



# FFT Processor


# FFT Processor

- FFT board
  - I & Q ADCs each running at 2.4 Gsamples/s
  - 2 GHz bandwidth
  - 1.5 MHz spectral bins
  - 2048 point complex FFT
  - Processing power of 300 GOPS
- Rack
  - Up to 6 FFT processors in a rack
  - 12 GHz bandwidth
  - 1.8 TOPS

# STAR-Dundee EM FFT Board




- Connections to nominal/redundant control processor via back plane
- ADC interface on front panel
- Currently under development

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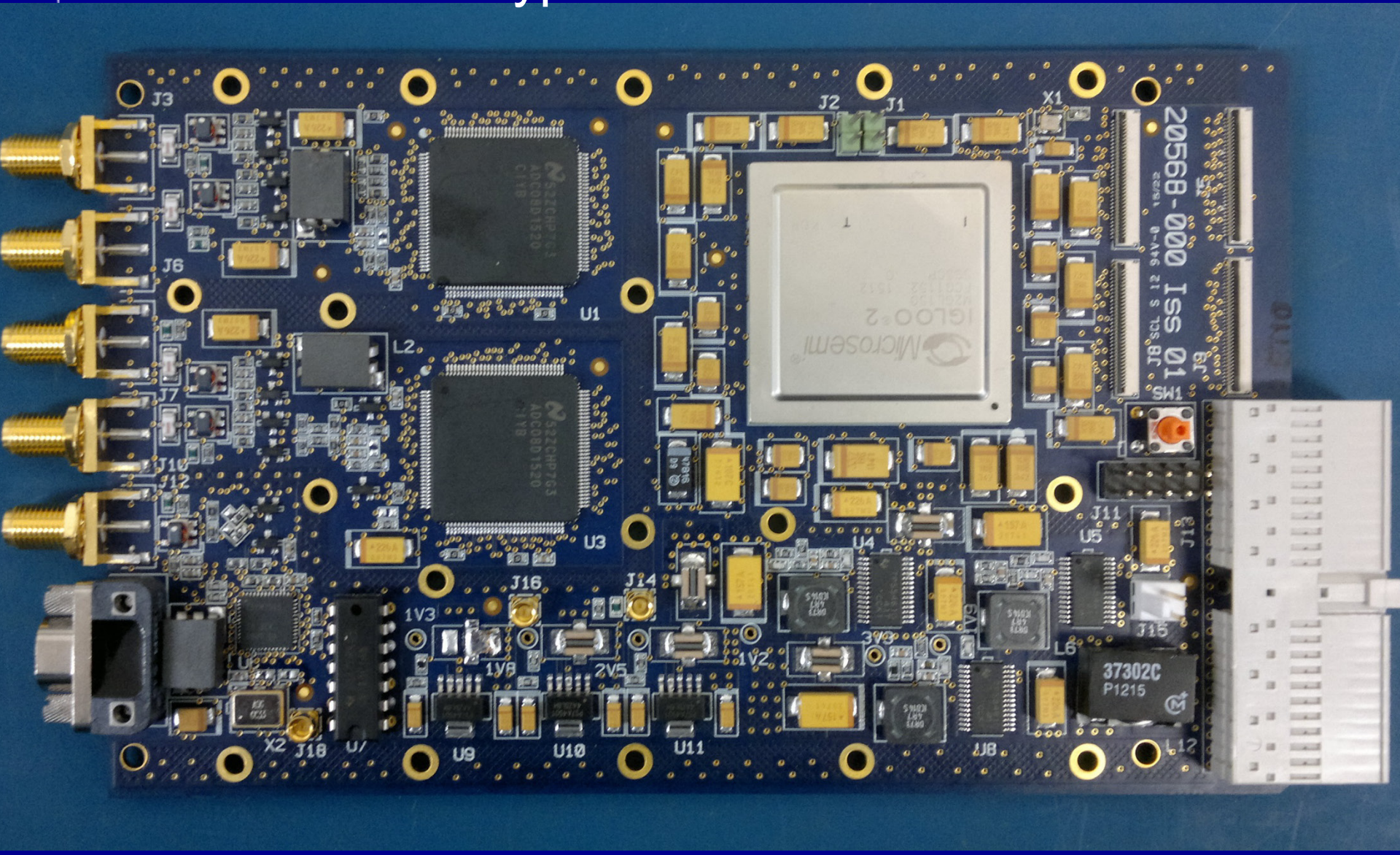
# Prototype FFT Board



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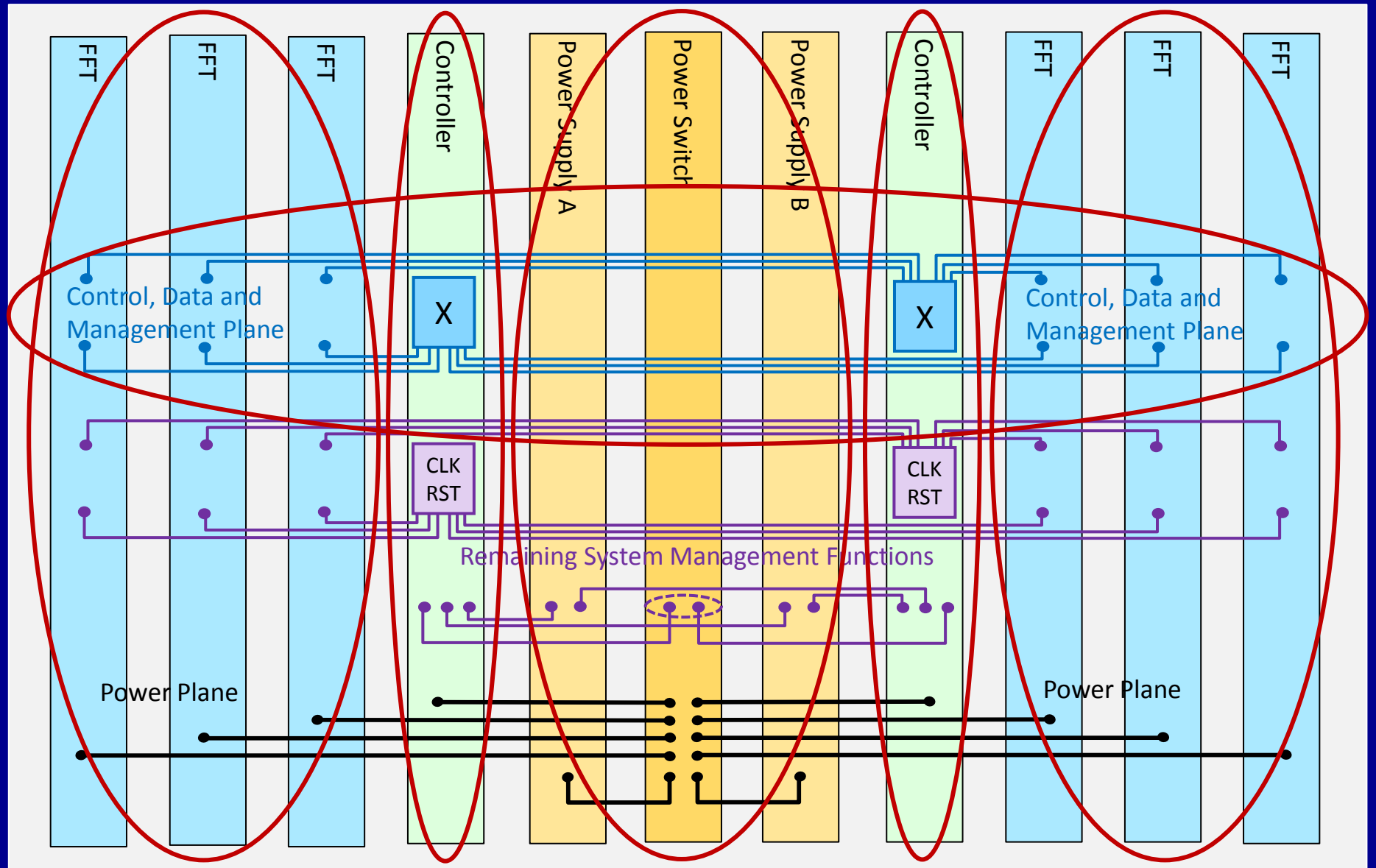
# SpaceVPX FFT Payload Processor



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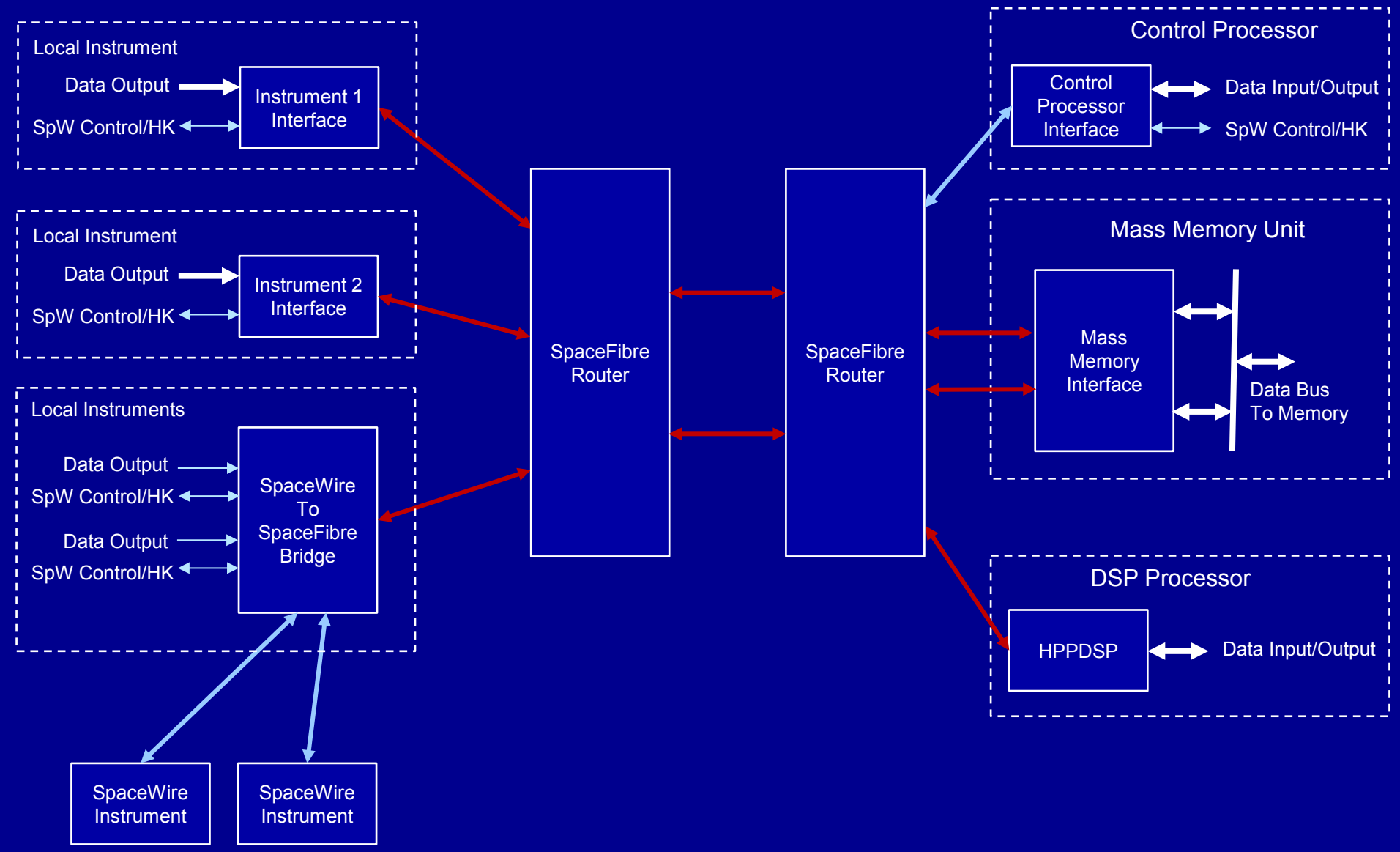
# Demonstration

# Reference Architecture (Demonstrator)



# Reference Architecture (Demonstrator)


SpaceFibre Router

SpaceFibre Router

Control Processor

Control Processor Interface

Data Input/Output

SpW Control/HK

Mass Memory Unit

Mass Memory Interface

Data Bus To Memory

Local Instruments

Data Output

SpW Control/HK

Data Output

SpW Control/HK

SpaceWire To SpaceFibre Bridge

Downlink Telemetry

Downlink Telemetry Interface

Data Output

SpW Control/HK

SpaceWire Instrument

SpaceWire Instrument

Remote Instruments

# Reference Architecture (Demonstrator)


SpaceFibre Router

SpaceFibre Router


Control Processor

Control Processor Interface

Data Input/Output

SpW Control/HK

Local Instruments

Data Output

SpW Control/HK

Data Output

SpW Control/HK

SpaceWire To SpaceFibre Bridge

Downlink Telemetry

Downlink Telemetry Interface

Data Output

SpW Control/HK

SpaceWire Instrument

SpaceWire Instrument

Remote Instruments

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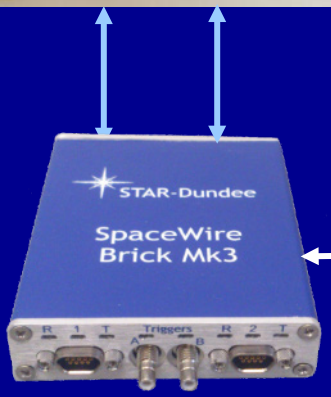



SpaceFibre Router

SpaceFibre Router


Control Processor

Control Processor Interface

Data Input/Output

SpW Control/HK

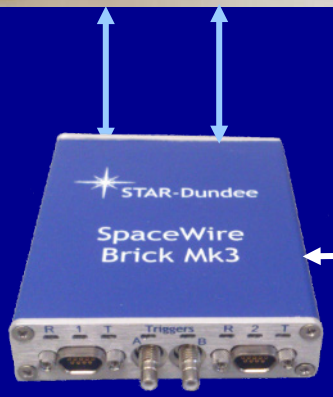
Downlink Telemetry

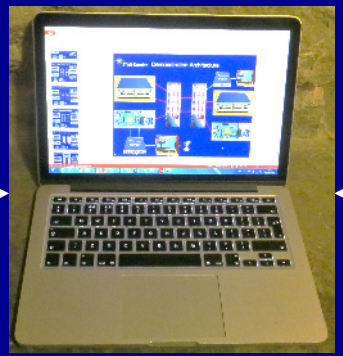
Downlink Telemetry Interface

Data Output

SpW Control/HK

# Reference Architecture (Demonstrator)

SpaceFibre Router

SpaceFibre Router

Control Processor

Control Processor Interface

Data Input/Output

SpW Control/HK


# Reference Architecture (Demonstrator)


SpaceFibre Router

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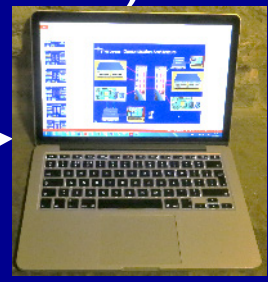


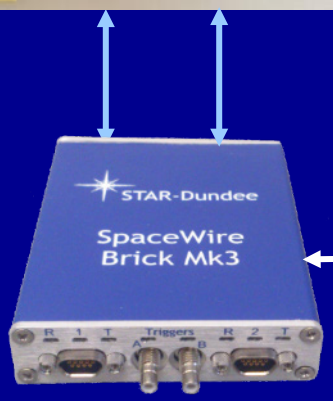


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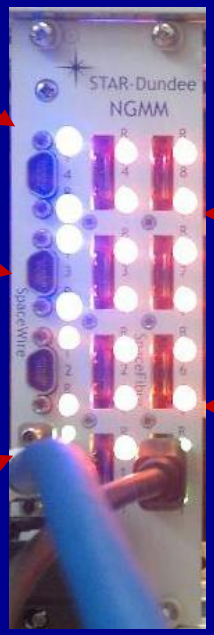




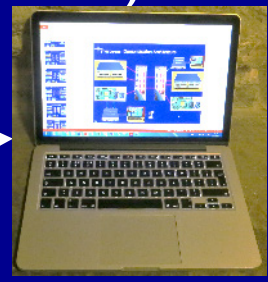


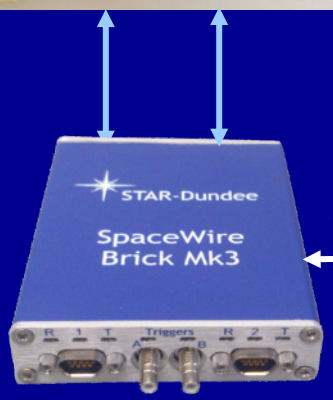


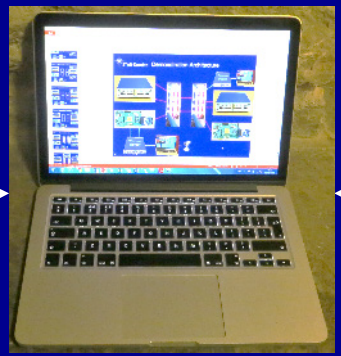

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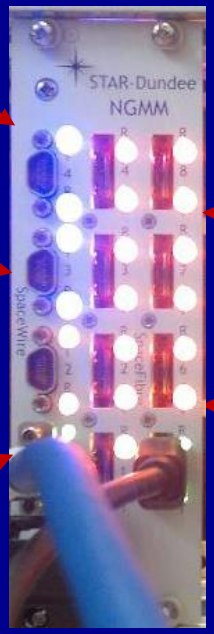
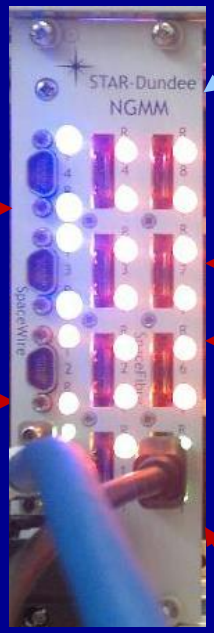
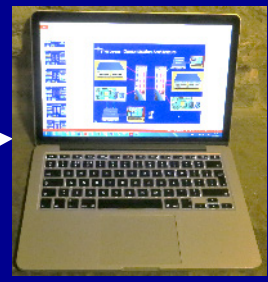
SpaceWire
SpaceFibre
IN
SpaceFibre
SpaceWire
STAR-Dundee
Out
Trigger


SpaceWire
SpaceFibre
IN
SpaceFibre
SpaceWire
STAR-Dundee
Out
Trigger

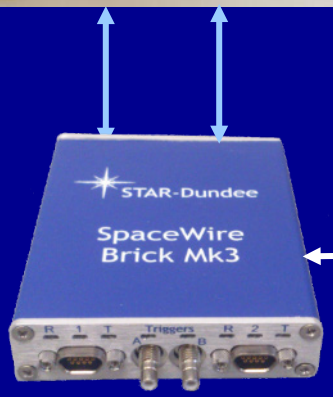

STAR-Dundee
NGMM


STAR-Dundee
NGMM


STAR-Dundee
SpaceWire
Brick Mk3




SpaceWire
SpaceFibre
IN
SpaceFibre
SpaceWire
STAR-Dundee
Out
Trigger


STAR-Dundee
SpaceWire
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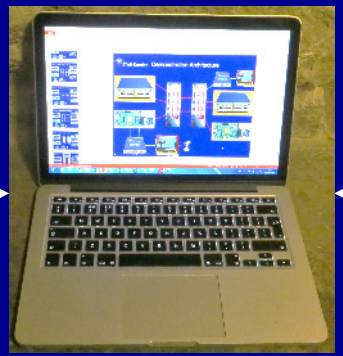

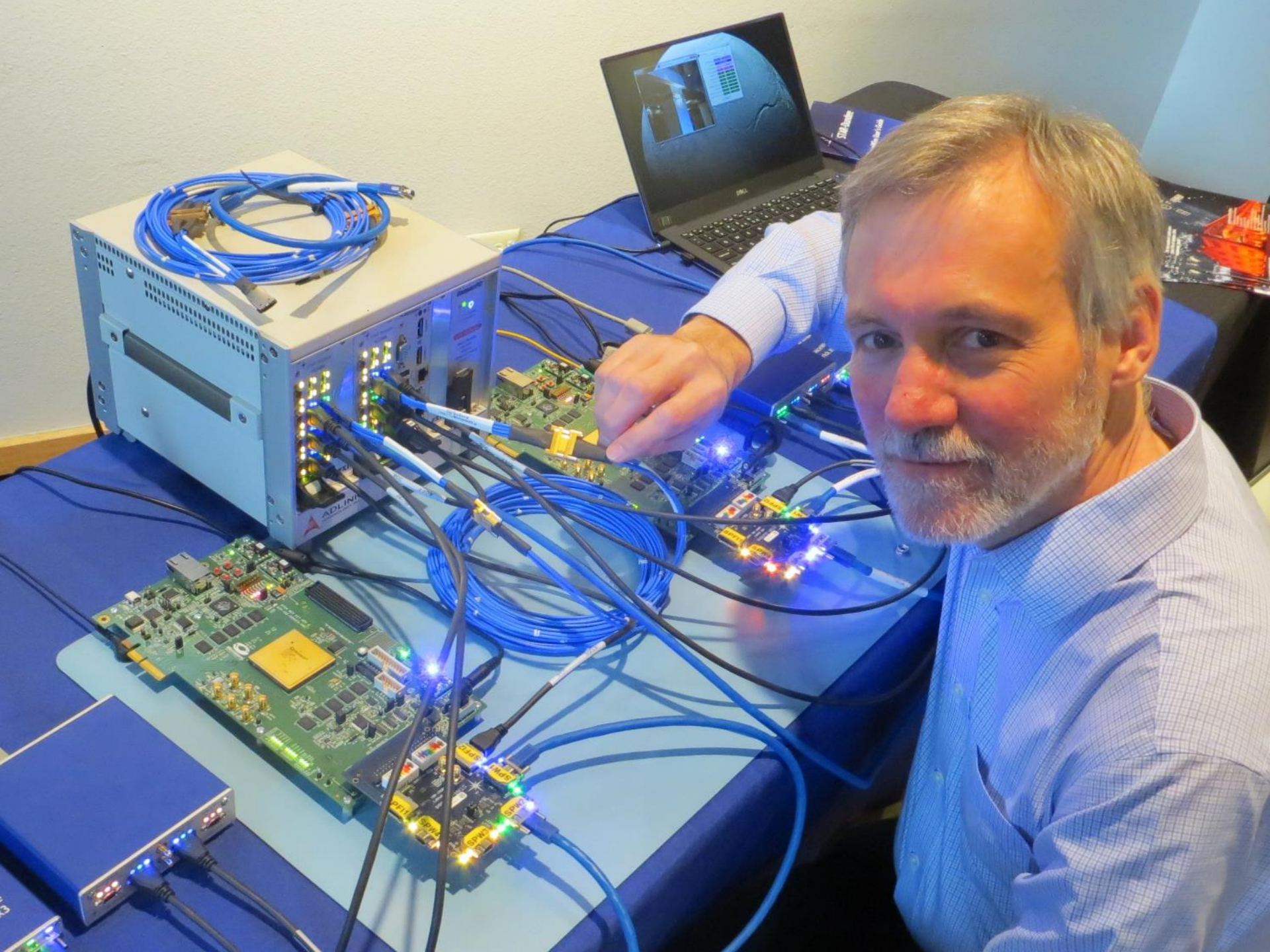

# Conclusions

- SpaceWire
  - An enabler for many space missions
- SpaceFibre
  - Ready for the next generation of space missions
  - Complementing and extending SpaceWire
  - Ideal for interconnection of DSP processors
- HPPDSP
  - Programmable DSP processor
  - With SpaceWire and SpaceFibre links
  - IO around 500 Mbits/s
- Ramon Chips RC64 many core DSP
  - 64 cores with very high performance
  - 12 SpaceFibre links on chip
- FFT processor
  - 2.4 Gsamples/s 2k-point FFT implemented in RTG4 FPGA

# Acknowledgements


- The research leading to these results has received funding from
  - The UK Space Agency, CEOI-ST under University of Leicester contract number:
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    - RP10G0327D13
    - RP10G0348A02
    - RP10G0348B206
    - RP10G0348A207
  - The European Space Agency under ESA contract numbers:
    - 17938/03/NL/LvH – SpaceFibre
    - 4000100103 - HPPDSP
    - 4000102641 - SpaceFibre Demonstrator
  - The European Union Seventh Framework Programme (FP7/2007-2013) under grant agreement numbers
    - 263148 - SpaceWire-RT (SpaceFibre QoS)
    - 284389 - SpaceFibre-HSSI (VHiSSI chip)