RC64
65nm Rad-Hard Hi-Rel Manycore High-Performance DSP for Software Defined Payloads

Ramon Chips is named in memory of Col. Ilan Ramon, Israeli astronaut who died on board the Columbia space shuttle, 1/2/2003

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Professor, EE, Technion—Israel

DSP Day, 15 June 2016

Contents

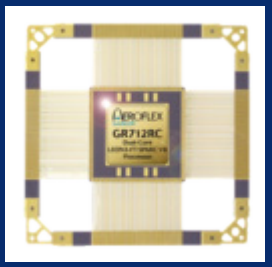
- Ramon Chips
- RC64 Architecture & Implementation
- RC64 Programming Model
- RC64 Software
- RC64 Applications

- Evening poster: MODEM on RC64
- Tomorrow: Image processing on RC64

Ramon Chips

- Government funded, in Israel, since 2002
- Make ITAR-free rad-hard hi-reliability high-performance processors for space
- Deliver & support for 30 years
- Combined leadership & heritage in
  - RH & HR
  - Semiconductors
  - Architecture
  - Software
  - Applications
  - Engineering
  - Production
  - Support

Present Products



COBHAM GAISLER
GR712RC
2-core LEON3

Image Compression

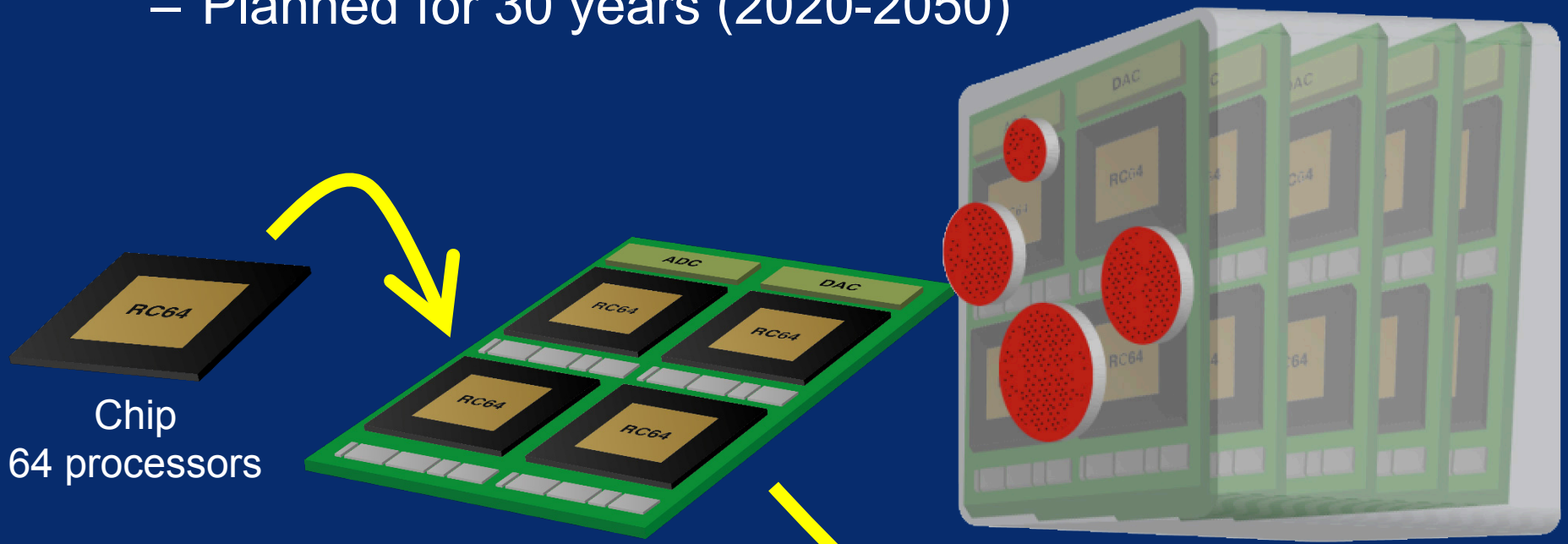
Plastic PQFP

OPSAT 3000

MASCOT on HAYABUSA-2

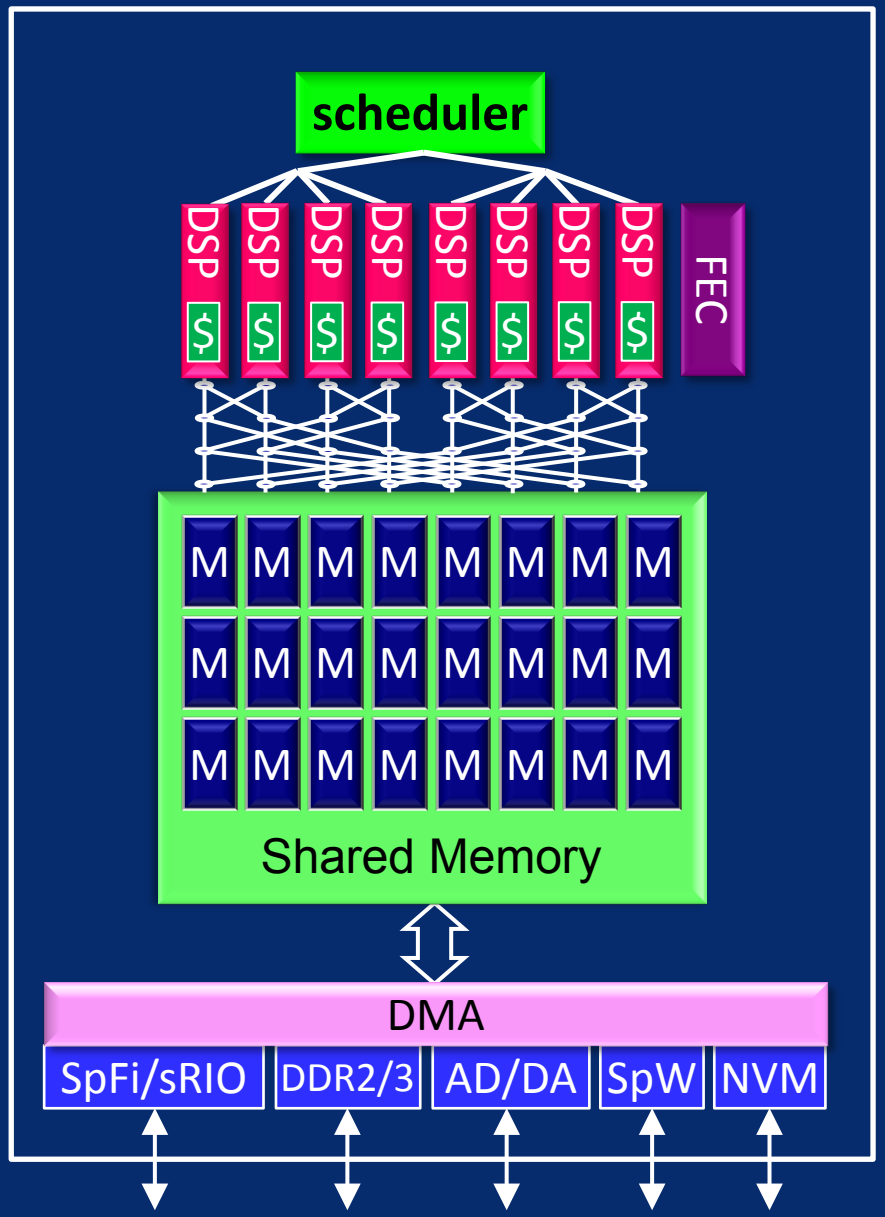
RC64 motivation

- Meet and exceed the NG-DSP challenge
  - From 1 GFLOPS to 40 GFLOPS and 150 GOPS
- Enable payload supercomputing for space
  - Replace ASICs, FPGAs, GPUs, CPUs
  - Planned for 30 years (2020-2050)



RC64

- 64 DSP cores
  - CEVA X1643
  - 300 MHz, 40 GFLOPS, 150 GOPS
- HW scheduler
- Modem HW accelerators
- 4 Mbyte shared memory
- Fast I/O
- Rad-Hard, FDIR
- 65nm LP TSMC
- 10 Watt
- PBGA & CCGA 624
- Designed for **SOFTWARE-DEFINED-PAYLOADS**



316 mm² Wire-bonded, IO around periphery

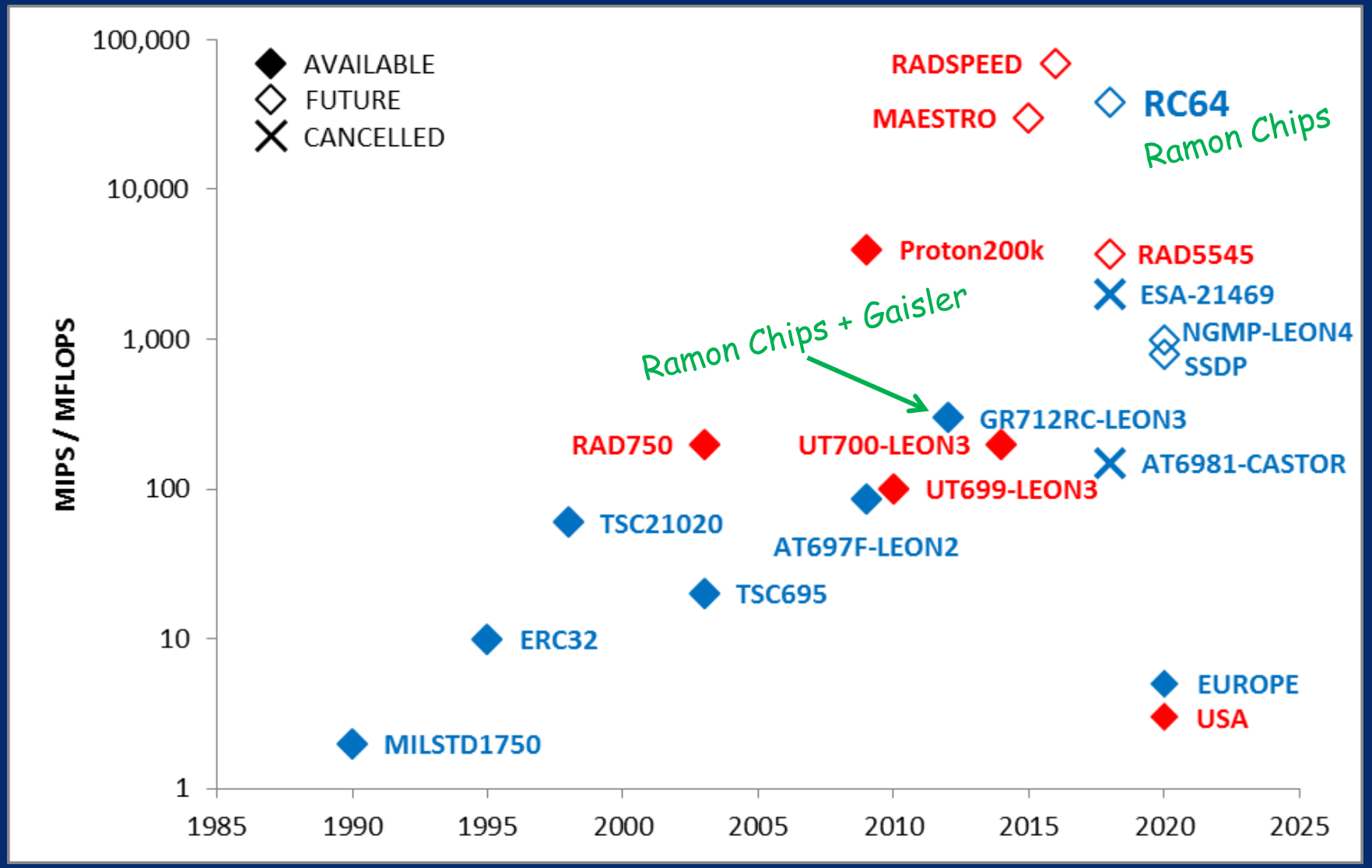
RC64 performance

- DVB-S2 modem: 2 Gb/s transmit, 1 Gb/s receive
- FFT (complex 16 bit fixed-point): 150 GOPS
- FFT (complex SP FP): 18 GFLOPS

- None of these use DDR3 external memory. Only streaming

- 10 Watt

RC64 *vs* other space processors



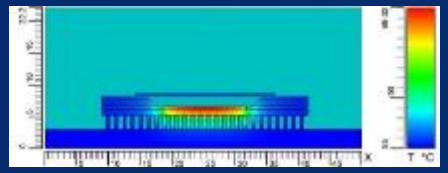
RC64 Power Dissipation

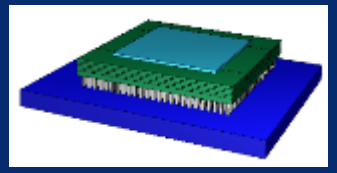
- 64 DSP cores (300 MHz): 8 Watt
- 12 SpFi links (6.25 Gbps): 2 Watt
- Power is scalable by # cores, frequency, I/O
  - One core at 150 MHz, no SpFi: 60 mWatt

- Power—Performance
  - 0.1 mW / MFLOP
    - 10,000 MFLOPS / Watt
  - 0.05 mW / MOP (Add or Mult)
  - 0.1 mW / MegaMAC
    - 10,000 MegaMAC / Watt
    - 20,000 MegaOPS / Watt

RC64 Package Options

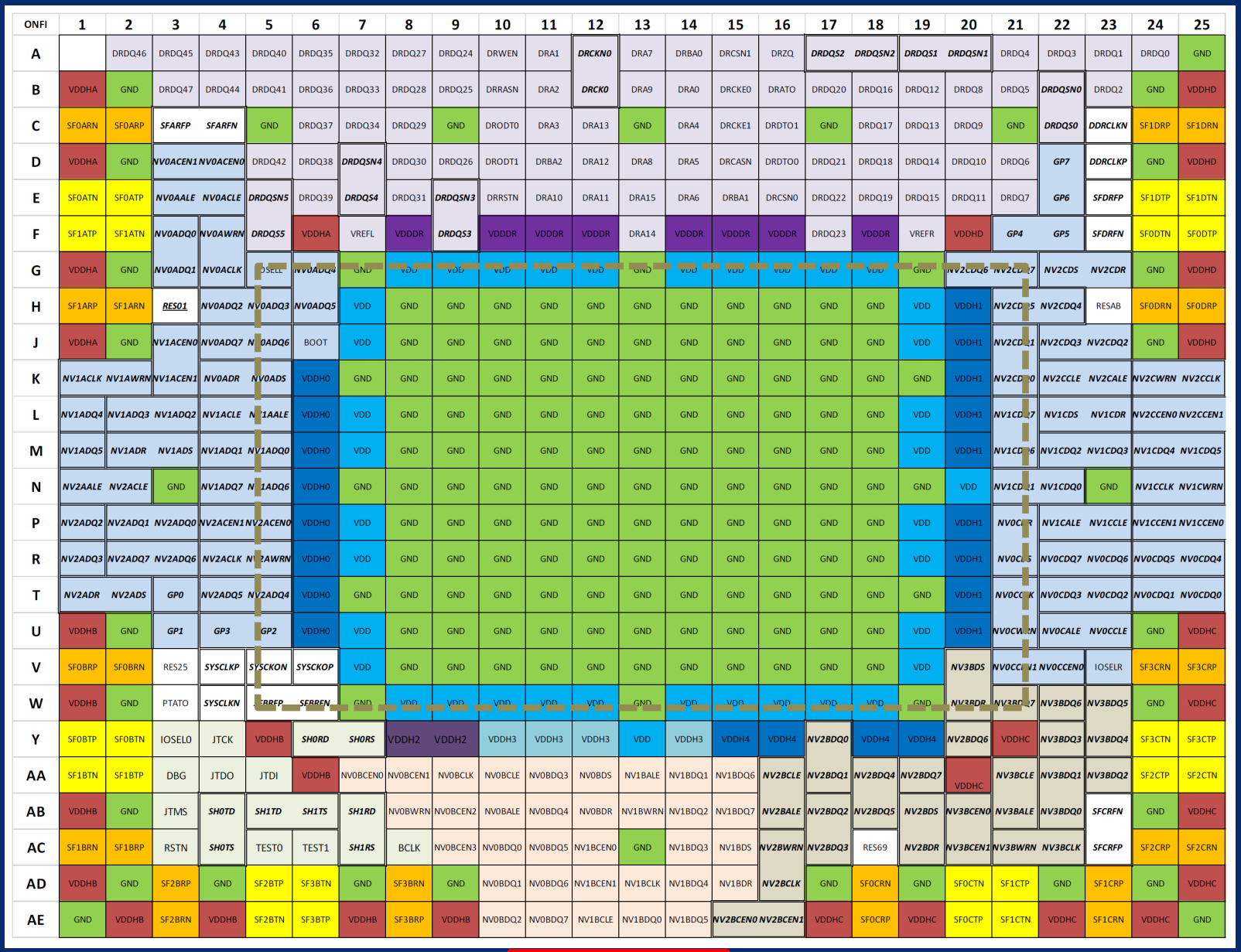
- Thermal cycling control by HW & SW
  - Temp sensors on-chip, SW maintains fixed temp
  - Mitigation of column / ball shearing due to cycles





1. PBGA 624
   - Wire bonded
2. CCGA 624
   - Wire bonded
3. CLGA 624

Pinout



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A		DRDQ46	DRDQ45	DRDQ43	DRDQ40	DRDQ35	DRDQ32	DRDQ27	DRDQ24	DRWEN	DRA1	DRCKN0	DRA7	DRBA0	DRCSN1	DRZQ	DRDQS2	DRDQSN2	DRDQS1	DRDQSN1	DRDQ4	DRDQ3	DRDQ1	DRDQ0	GND
B	VDDHA	GND	DRDQ47	DRDQ44	DRDQ41	DRDQ36	DRDQ33	DRDQ28	DRDQ25	DRRASN	DRA2	DRCK0	DRA9	DRA0	DRCKE0	DRATO	DRDQ20	DRDQ16	DRDQ12	DRDQ8	DRDQ5	DRDQSN0	DRDQ2	GND	VDDHD
C	SF0ARN	SF0ARP	SFARFP	SFARFN	GND	DRDQ37	DRDQ34	DRDQ29	GND	DRODT0	DRA3	DRA13	GND	DRA4	DRCKE1	DRDTO1	GND	DRDQ17	DRDQ13	DRDQ9	GND	DRDQS0	DDRCLKN	SF1DRP	SF1DRN
D	VDDHA	GND	NV0ACEN1	NV0ACEN0	DRDQ42	DRDQ38	DRDQSN4	DRDQ30	DRDQ26	DRODT1	DRBA2	DRA12	DRA8	DRA5	DRCASN	DRDTO0	DRDQ21	DRDQ18	DRDQ14	DRDQ10	DRDQ6	GP7	DDRCLKP	GND	VDDHD
E	SF0ATN	SF0ATP	NV0AALE	NV0ACLE	DRDQSN5	DRDQ39	DRDQS4	DRDQ31	DRDQSN3	DRRSTN	DRA10	DRA11	DRA15	DRA6	DRBA1	DRCSN0	DRDQ22	DRDQ19	DRDQ15	DRDQ11	DRDQ7	GP6	SFDRFP	SF1DTP	SF1DTN
F	SF1ATP	SF1ATN	NV0ADQ0	NV0AWRN	DRDQS5	VDDHA	VREFL	VDDDR	DRDQS3	VDDDR	VDDDR	VDDDR	DRA14	VDDDR	VDDDR	VDDDR	DRDQ23	VDDDR	VREFR	VDDHD	GP4	GP5	SFDRFN	SF0DTN	SF0DTP
G	VDDHA	GND	NV0ADQ1	NV0ACLK	DSELL	NV0ADQ4	GND	VDD	VDD	VDD	VDD	VDD	GND	VDD	VDD	VDD	VDD	VDD	GND	NV2CDQ6	NV2CDQ7	NV2CDS	NV2CDR	GND	VDDHD
H	SF1ARP	SF1ARN	RES01	NV0ADQ2	NV0ADQ3	NV0ADQ5	VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD	VDDH1	NV2CDQ5	NV2CDQ4	RESAB	SF0DRN	SF0DRP
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M	NV1ADQ5	NV1ADR	NV1ADS	NV1ADQ1	NV1ADQ0	VDDH0	VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD	VDDH1	NV1CDQ6	NV1CDQ2	NV1CDQ3	NV1CDQ4	NV1CDQ5
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V	SF0BRP	SF0BRN	RES25	SYSCLKP	SYSCKON	SYSCKOP	VDD	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD	NV3BDS	NV0CCEN1	NV0CCEN0	IOSELR	SF3CRN	SF3CRP
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AA	SF1BTN	SF1BTP	DBG	JTDO	JTDI	VDDHB	NV0BCEN0	NV0BCEN1	NV0BCLK	NV0BCLE	NV0BDQ3	NV0BDS	NV1BALE	NV1BDQ1	NV1BDQ6	NV2BCLE	NV2BDQ1	NV2BDQ4	NV2BDQ7	VDDHC	NV3BCLE	NV3BDQ1	NV3BDQ2	SF2CTP	SF2CTN
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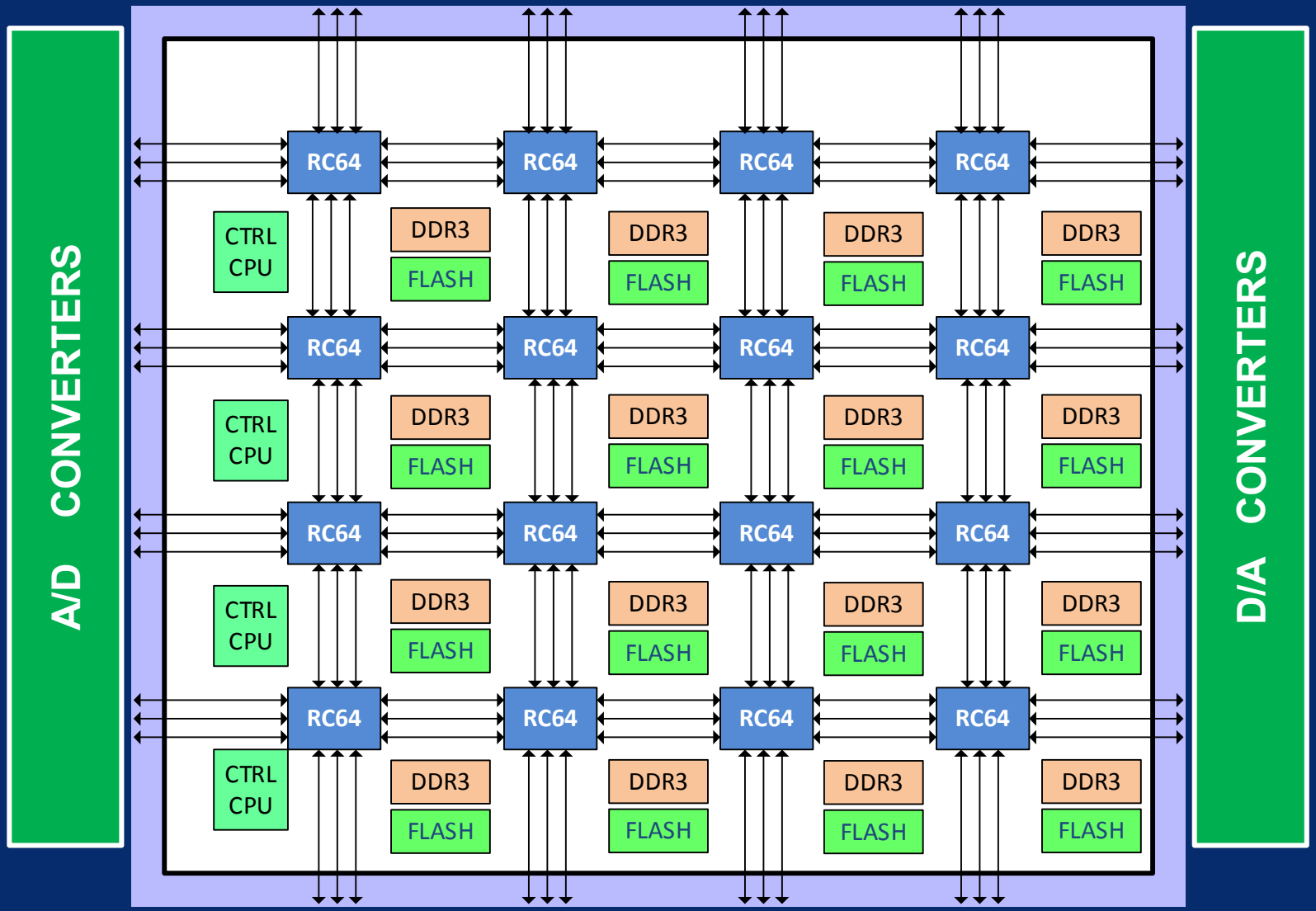
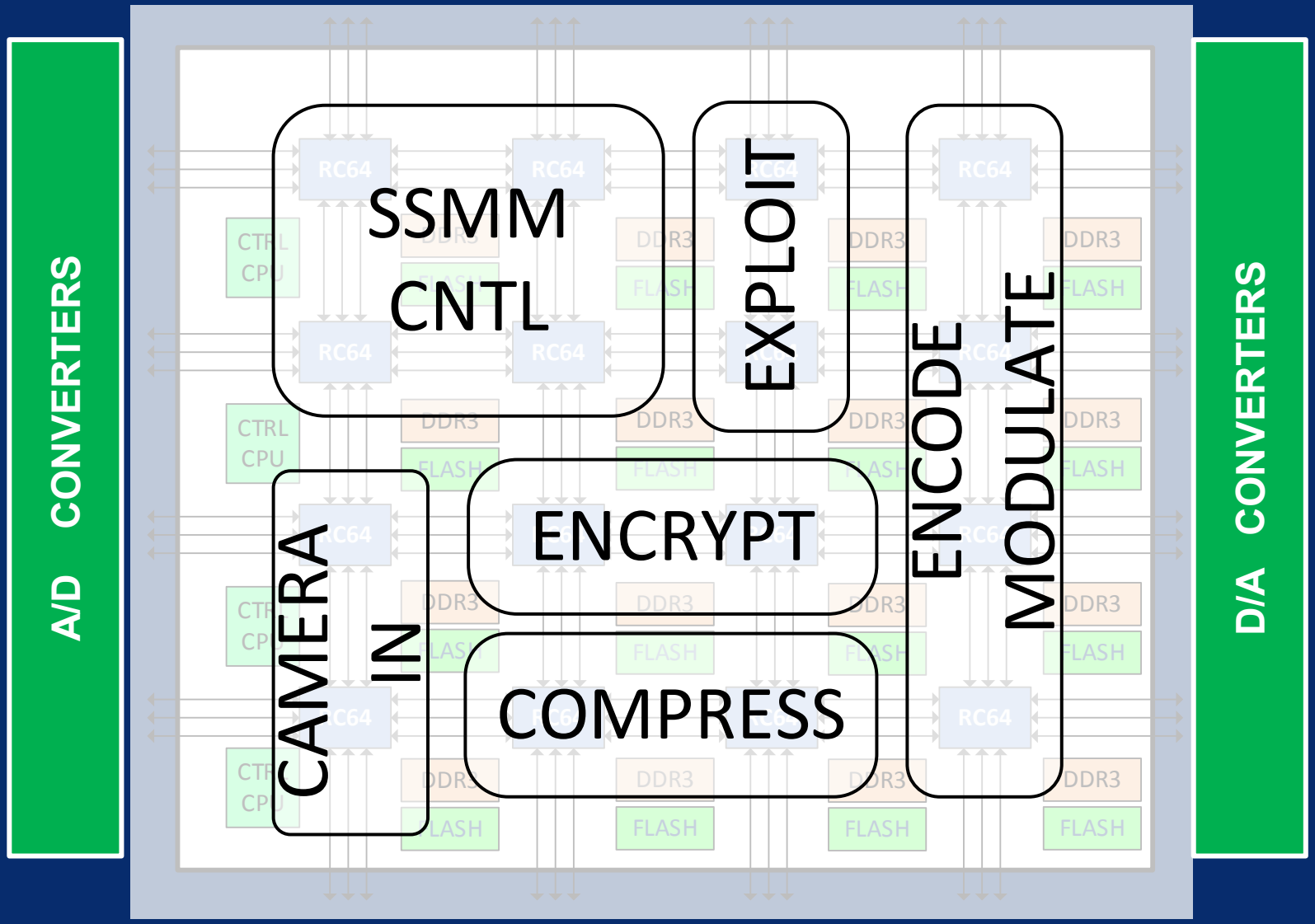
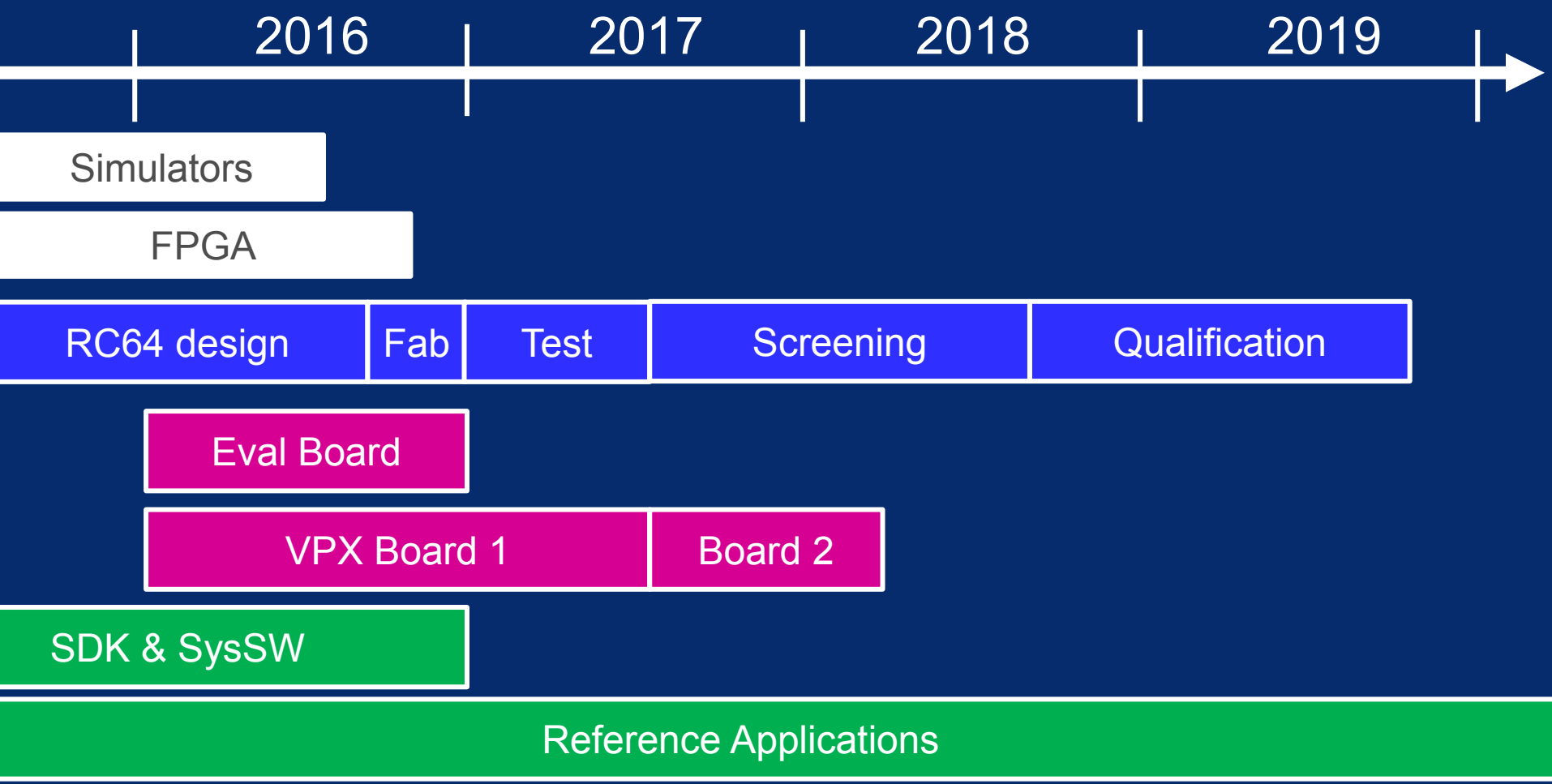
Software-Defined Payload



Software-Defined Payload

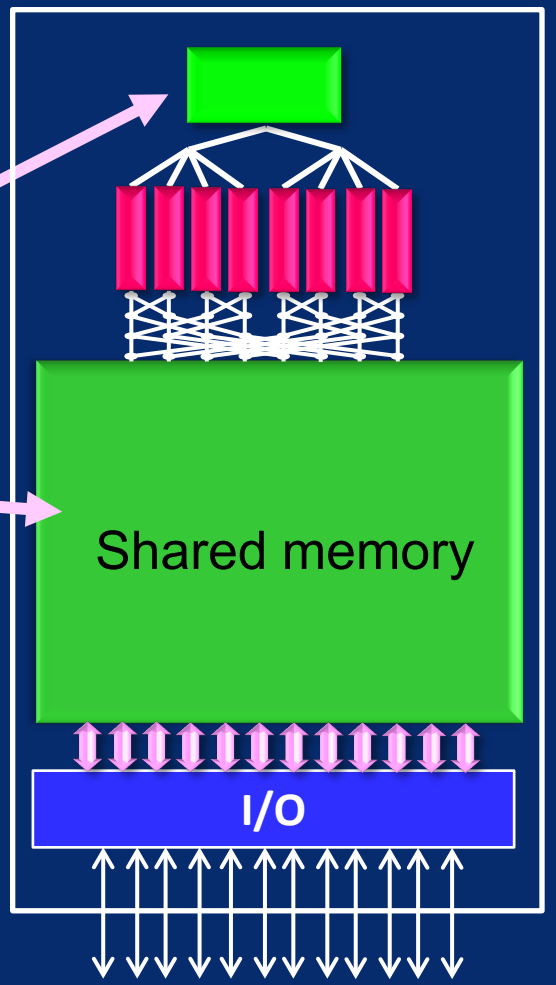


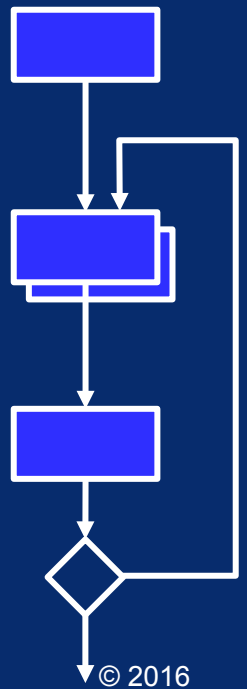
RC64 Near-Term Development Plan



RC64 Task-Oriented Programming Model

- Shared memory (PRAM)
  - No message passing among processors
- Single program, bare metal, no OS
  - Many-core, not multi-core
- Code in TWO parts:
  - Task-dependency-graph
  - Sequential task codes

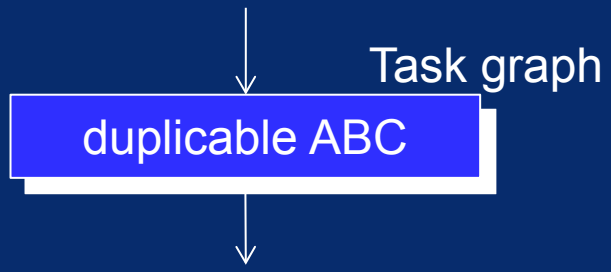




Code Example

Convert (independent) loop iterations

```
for ( i=0; i<10000; i++ ) {
   a[i] = b[i]*c[i];
}
```



into duplicable (parallel) tasks

```
set_task_quota(ABC, 10000)
```

Instance number

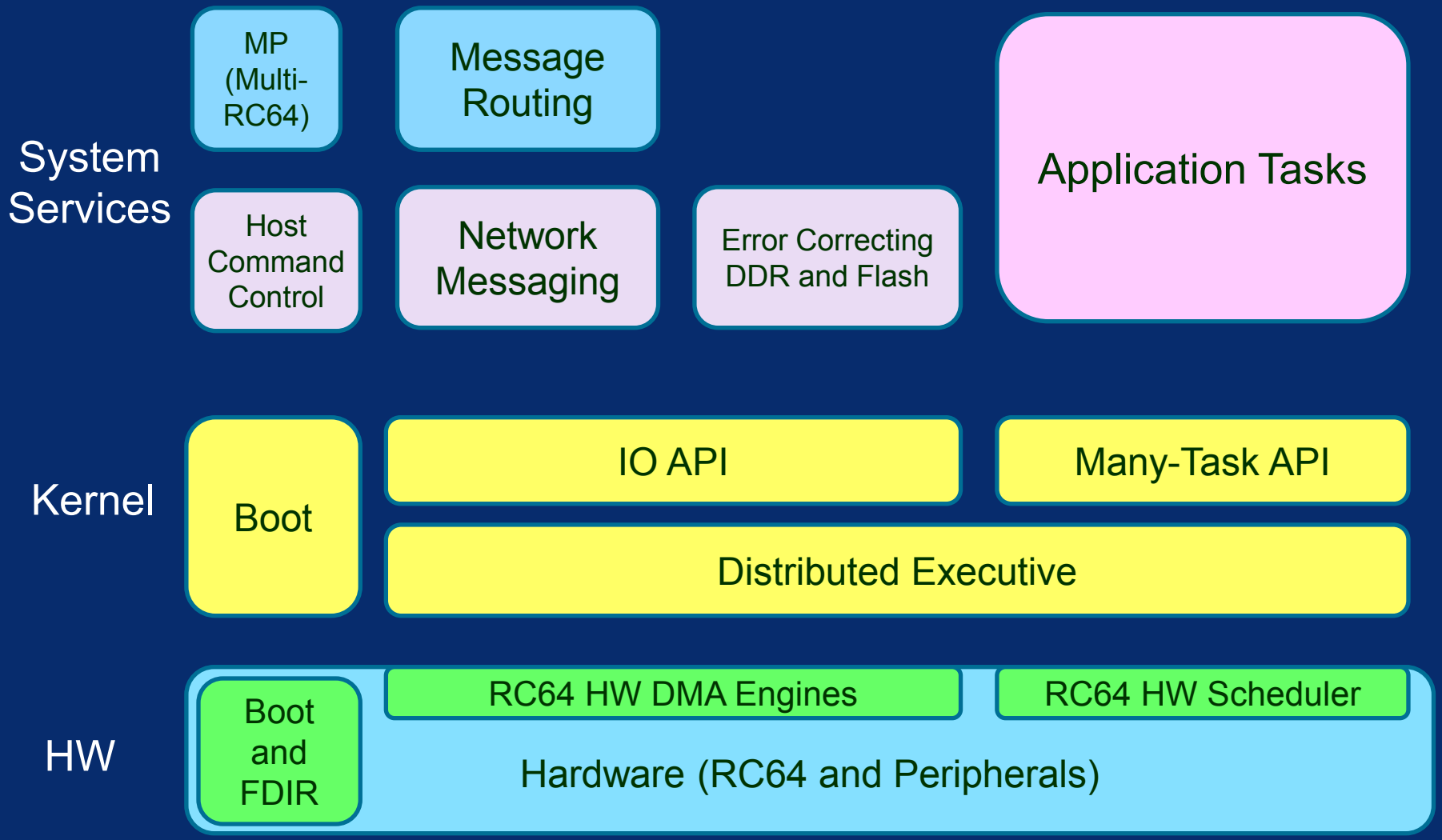
```
void ABC(id)
{ a[id] = b[id]*c[id]; }
```

Each task is sequential !

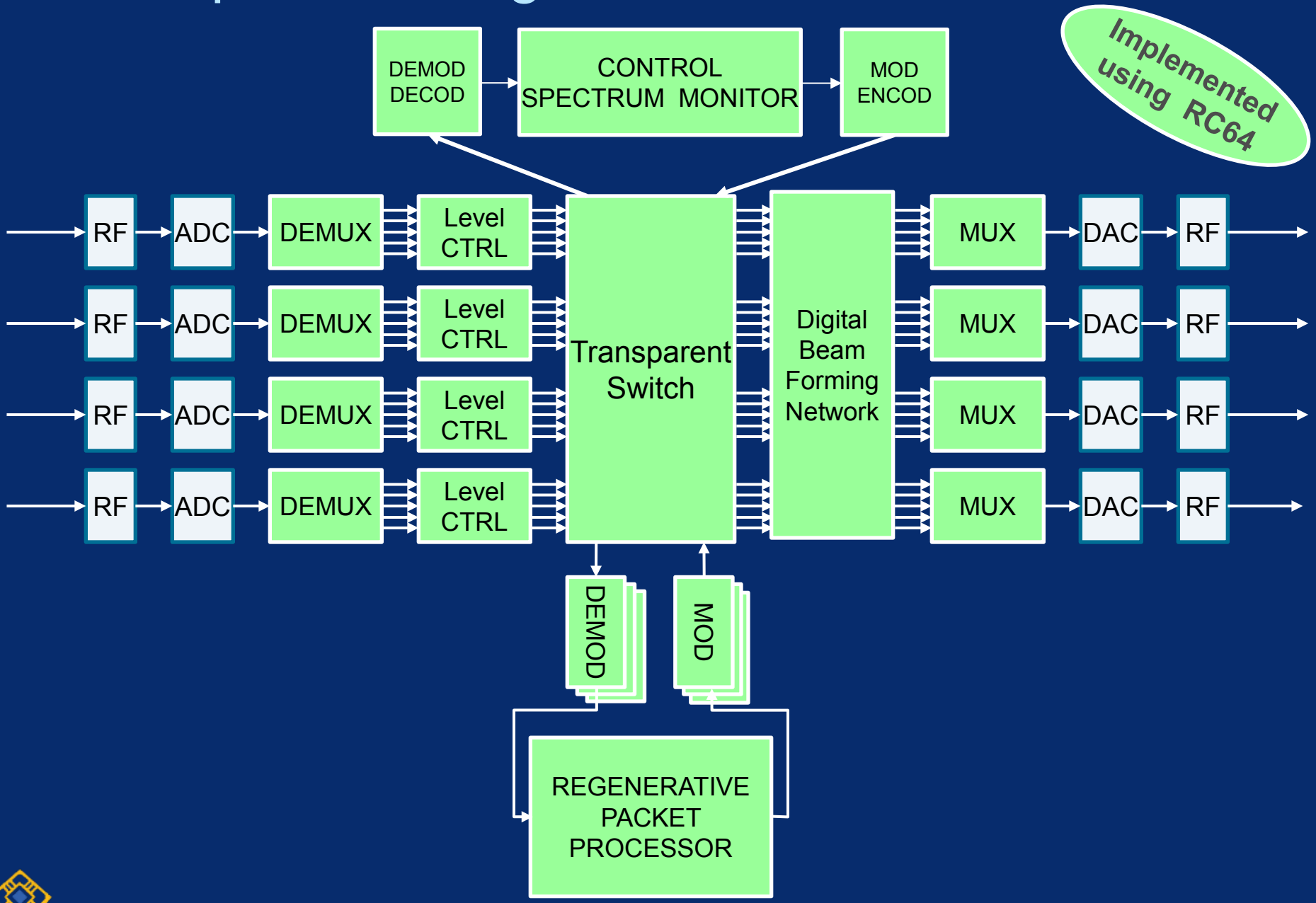
RC64 SW Development Tools

Optimization & performance tuning	Parallel Program Profiler	Event Recorder (time stamp tracer)	Parallel DSP Kernels & Libraries
Simulation	Parallel Program Simulator	RC64 Cycle-Accurate Simulator	Many Core Debugger
Parallel Programming	Task Compiler		
Compiler tool chain	Compiler, ASM, Linker	CEVA	Core DSP Libraries

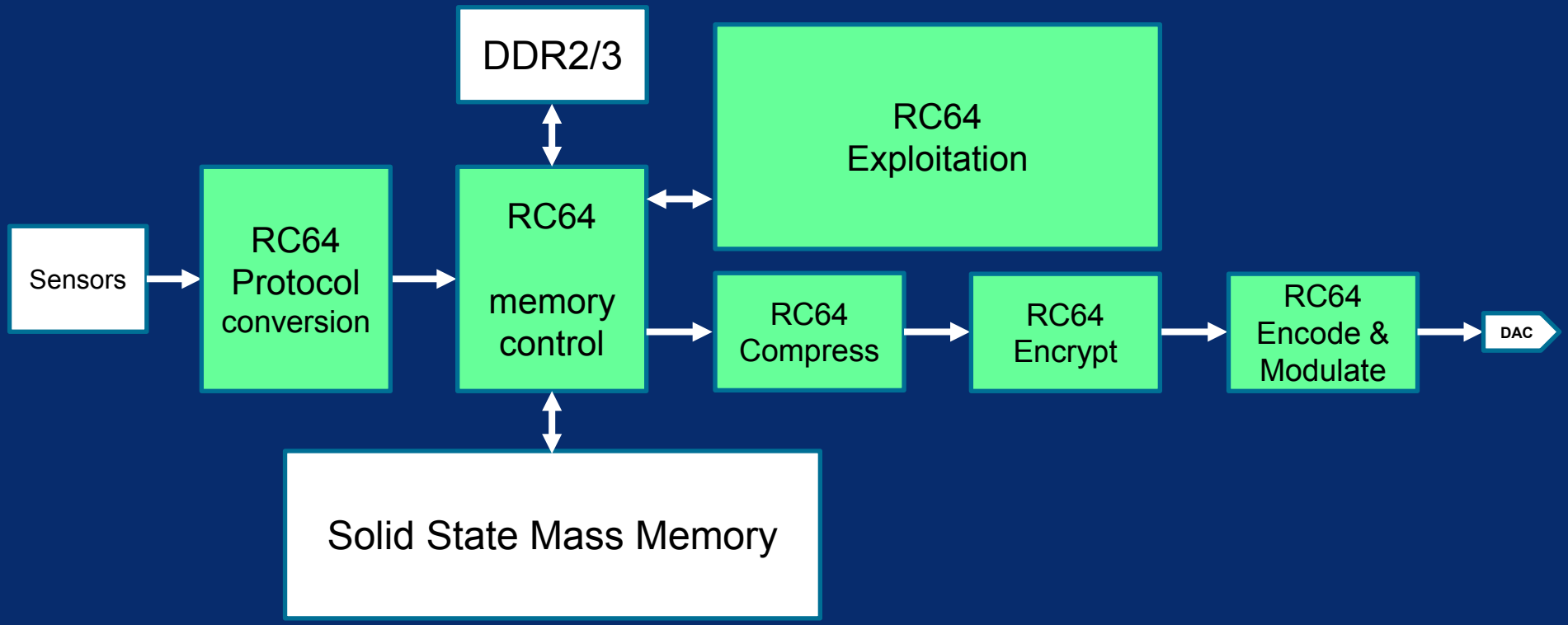
RC64 Run Time Model



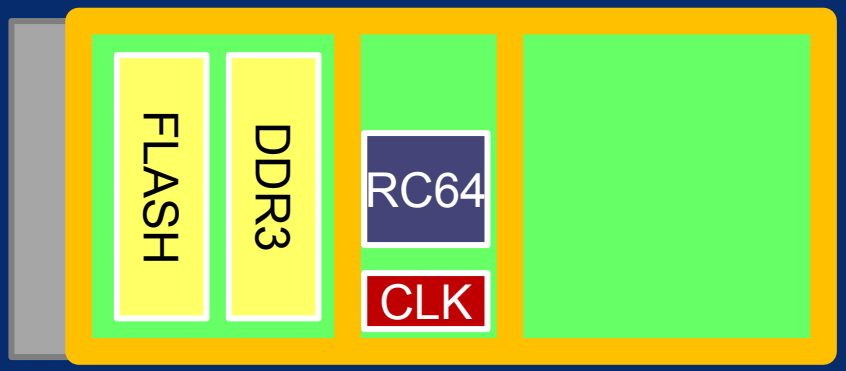
Transparent / Regenerative SW-Defined PLD



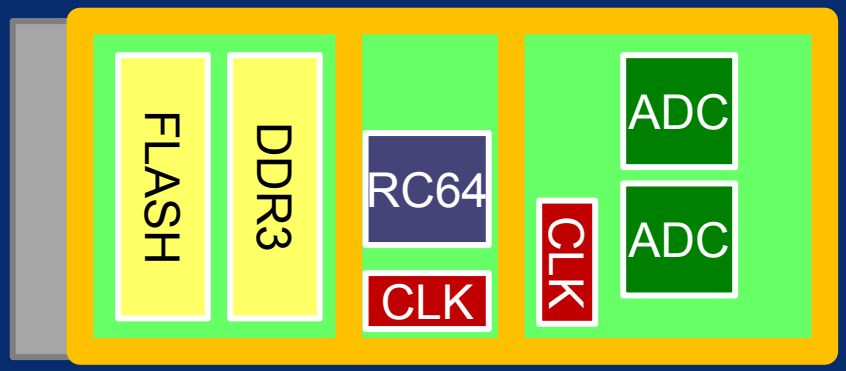
EOS Software-Defined Payload



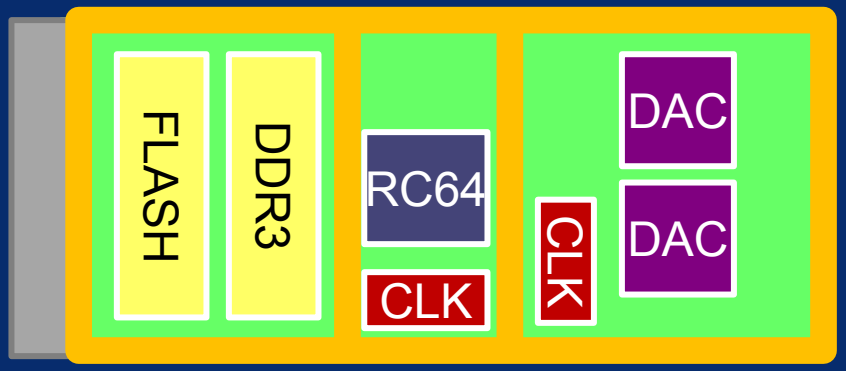
3U VPX cards



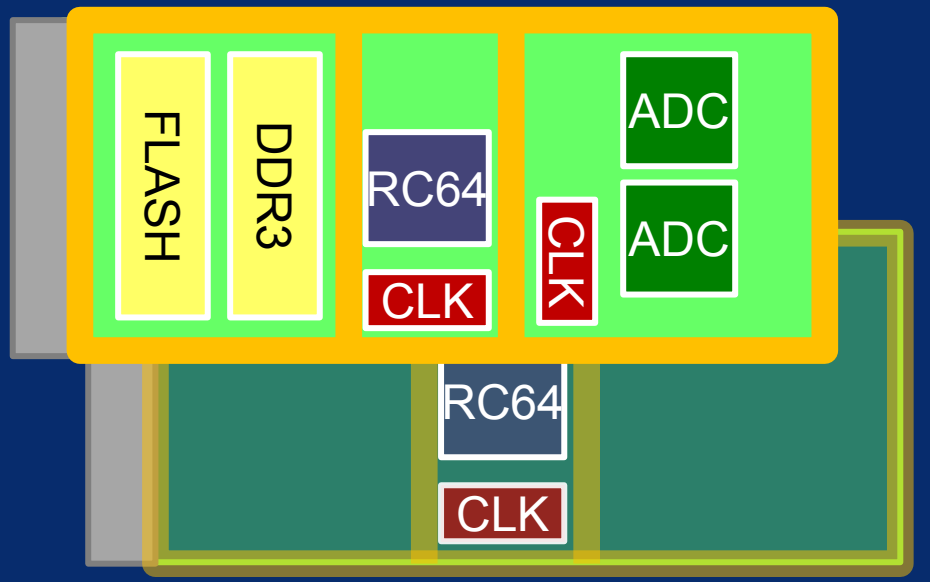
COMPUTE



RECEIVER

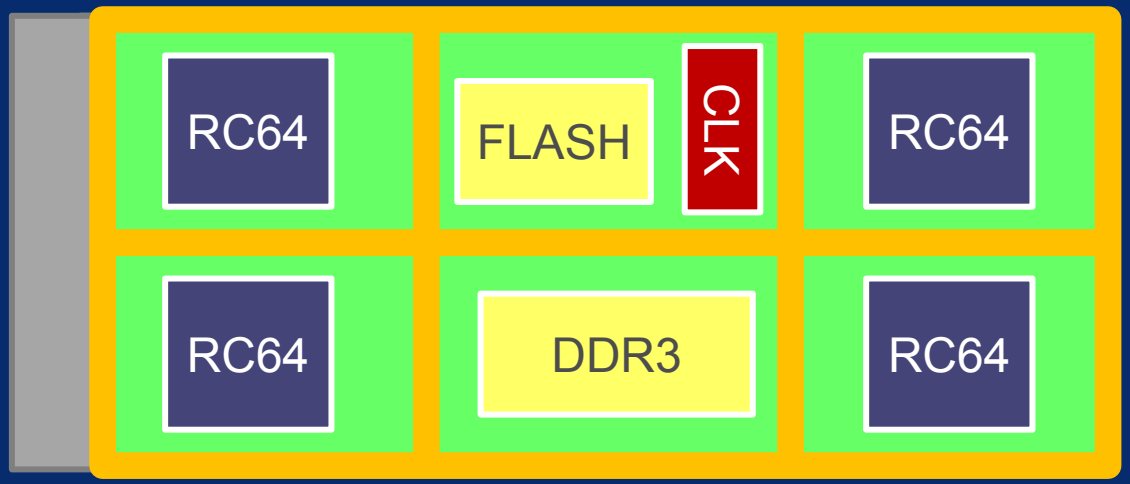


WB TRANSMITTER



WB RECEIVER

3U VPX 4X card



Summary

- High performance DSP/CPU for space
- 64 cores, large shared memory, high speed I/O
- Simpler shared memory programming
- For software-defined payloads
- HW: chips, boards, multi-board modules
- SW: SDK, System SW, Reference Applications
- ES 2017
  EM 2018
  FM 2019

- Evening poster, another talk tomorrow

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