Radiation Hardened by Design
Pipeline Analog-to-Digital Converter Blocks in CMOS 0.18µm Technology

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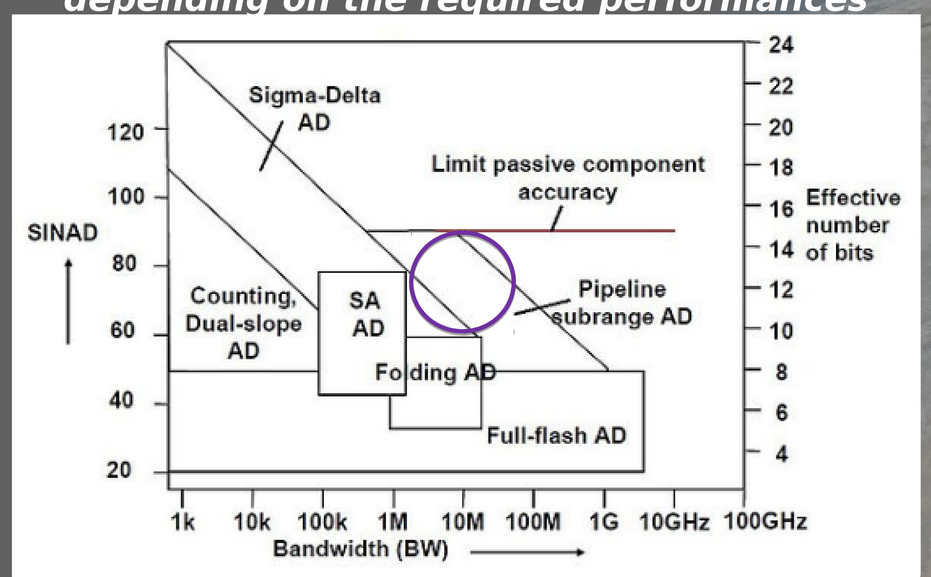
CCD sensors embedded in satellites :

- convert analog signals into digital ones with high precision and speed (11 bits – 14 bits at 10 MS/s)
- must be radiation hardened due to the space environment.

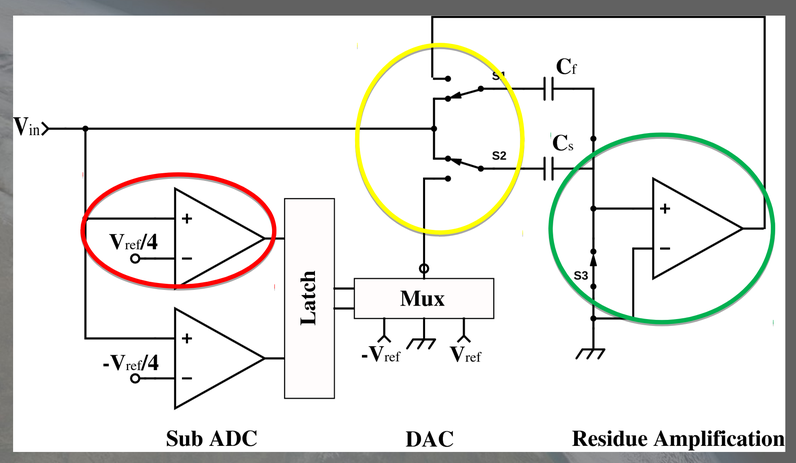
Overview of the most used architectures depending on the required performances



B. Murmann, "ADC Performance Survey 1997 – 2015"

Choice of the most suitable ADC

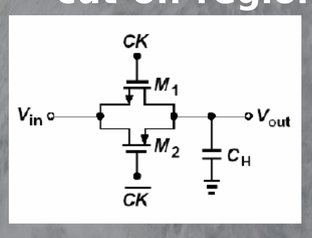
1.5 bit stage for Pipeline ADC

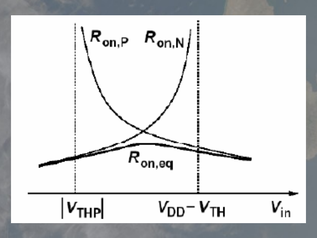


The components that have the greatest influence on the ADC performances and the most sensitive blocks to radiations are highlighted: comparator, switches and amplifier

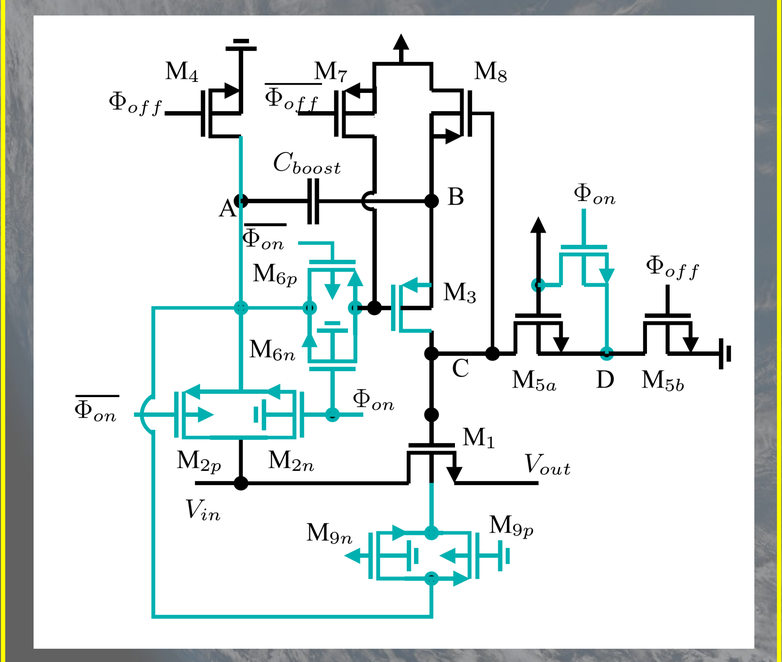
Switches

Analog CMOS switches weaknesses:
- charge injection,
- R_{on} depending on V_{in} amplitude,
- cut-off region.

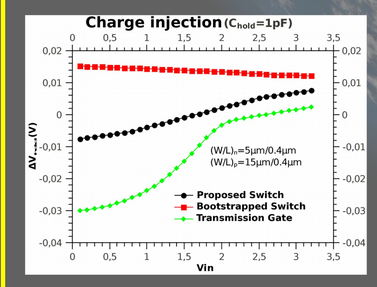


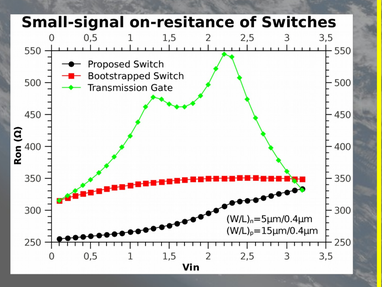


➢ Bootstrapped switch architecture : No voltage overshoot to prevent from SEGR damages

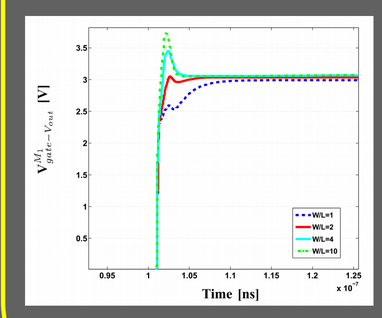


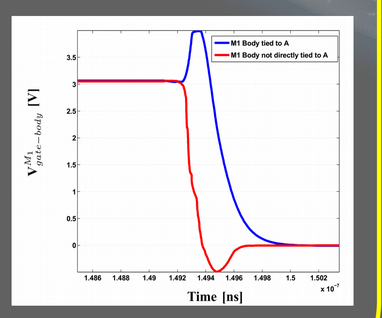
➢SWITCH Characteristics





➢No Overshoot

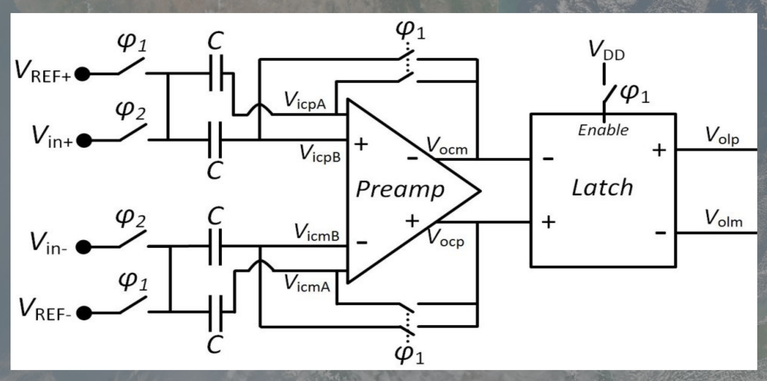


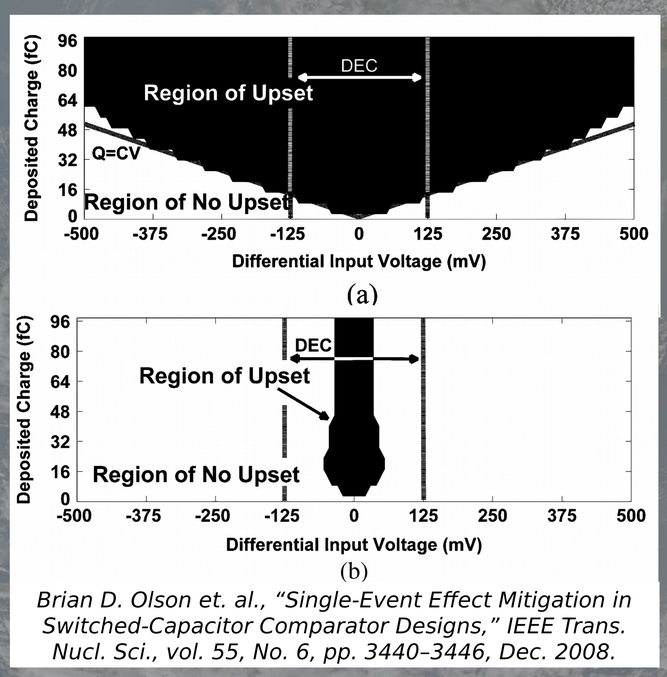


Comparator

Weaknesses in radiative environment:
- high number of SEU.

➢ Dual path design technique : lower vulnerability of floating nodes.
➢ Auto-zero approach to reduce the offset.





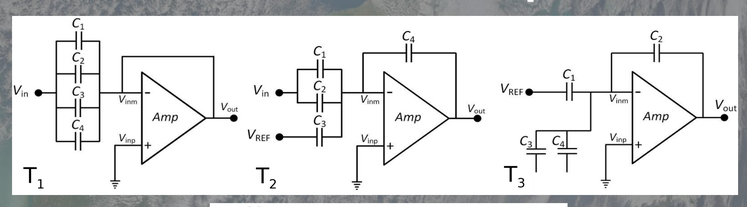
Brian D. Olson et. al., "Single-Event Effect Mitigation in Switched-Capacitor Comparator Designs," IEEE Trans. Nucl. Sci., vol. 55, No. 6, pp. 3440–3446, Dec. 2008.

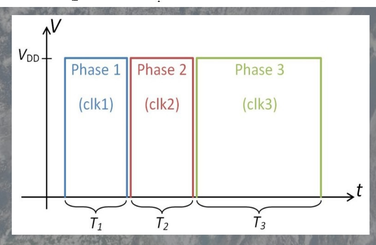
Simulated contour plots of differential pre-amp input voltage vs. deposited charge for (a) standard switched capacitor design and (b) dual path auto zero comparator

Amplifier

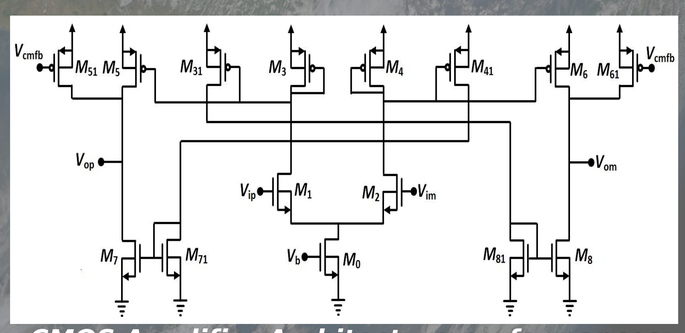
Weaknesses:
- reliability of the main stage amplifier,
- high power consumption (Gain, GBW).

➢ Correlated double sampling (CDS)
➢ Predictive rail to rail amplifier



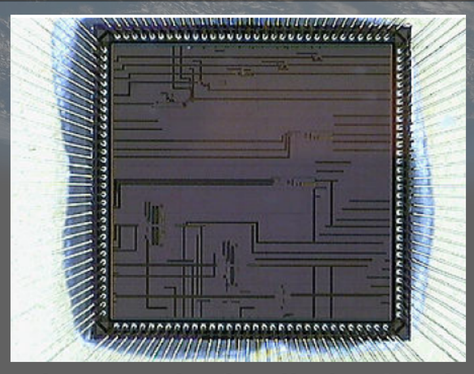


Principle of the 3 phases operation of the predictive amplifier : reset (T1), prediction (T2) and amplification (T3)



CMOS Amplifier Architecture performances:
- Gain: 45 dB,
- GBW: 260 MHz,
- Power consumption: 5 mW.

2-bits accuracy improvement for a 7% power consumption increase only.



Die photograph of radiation Hardened pipeline ADC blocks in 0.18 µm HV CMOS technology

Conclusion and Perspectives:

- Ongoing experimental measurements to validate simulation results,
- Heavy ions tests to assess SEE,
- Complete RHBD pipeline 11 bits 10MS/s ADC design.
- Higher Amplifier Gain based on RFC architecture (60-70dB gain)

Laboratoire conventionné avec l'Université de Toulouse