SIPHRA
Silicon Photomultiplier Readout ASIC

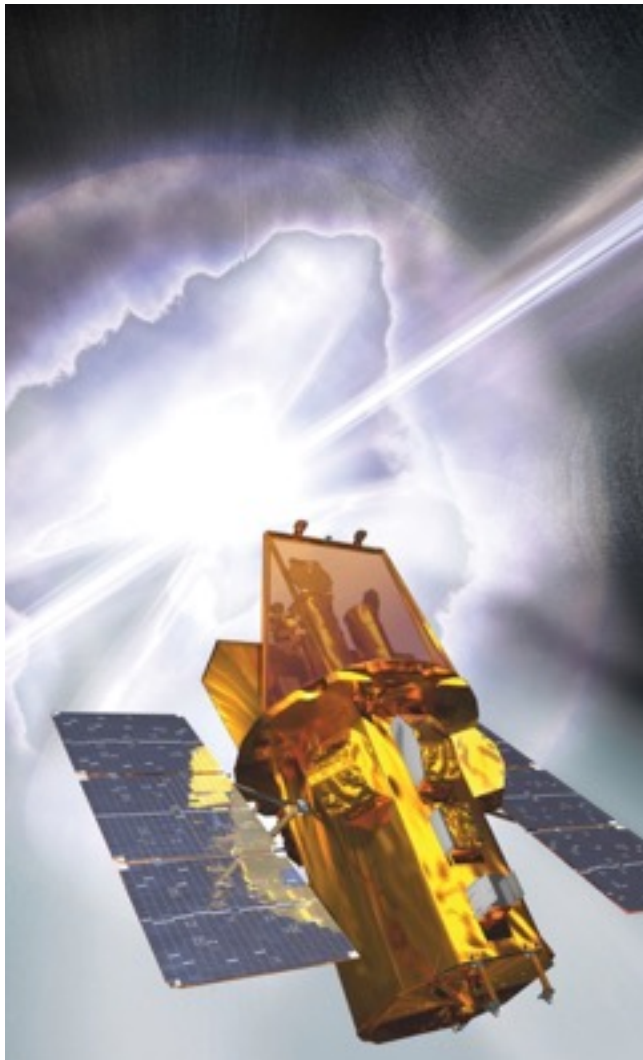
Prototype ASIC for SiPM Based Gamma-Ray Detector

Hans Kristian Otnes Berge
(hans.berge@ideas.no)

IDEAS - Integrated Detector Electronics AS

SIPHRA, an ASIC designed to measure gamma radiation in space

- Why measure gamma rays ?
  - We want to measure high energy radiation from cosmic sources to understand basic processes of the universe.
  - Understand the dark energy and dark matter puzzle.
  - Measure properties of planetary bodies by emitted and gamma rays.
  - Understand the radiation spacecrafts may be exposed to.



LaBr Scintillator with SiPMs

SiPMs for GRIPS Alexei Ulyanov

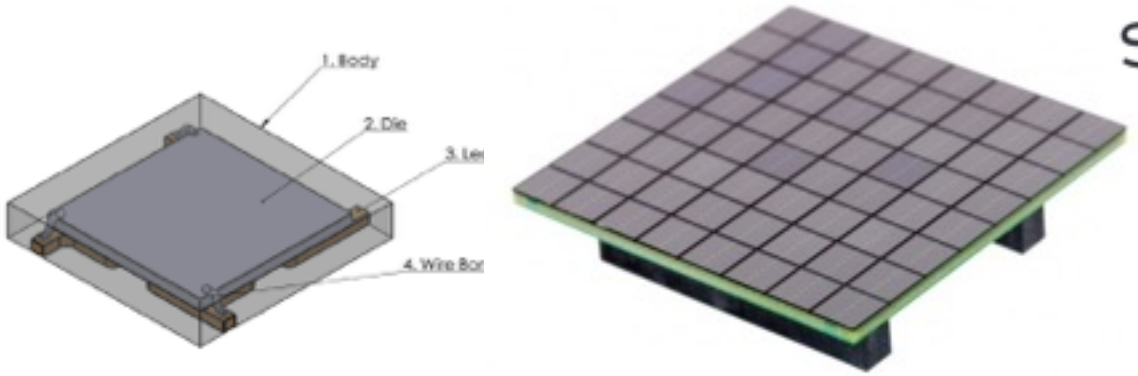
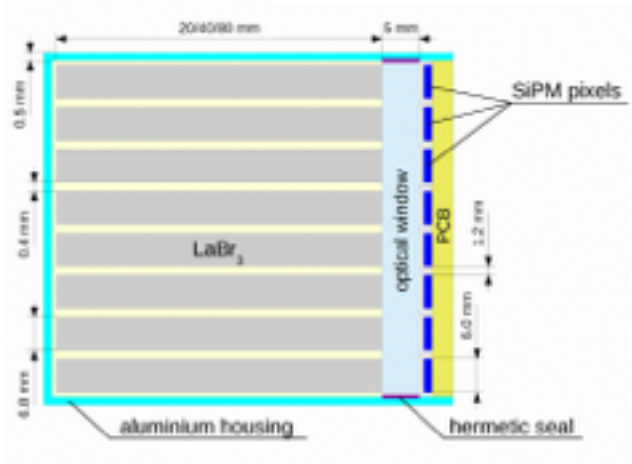
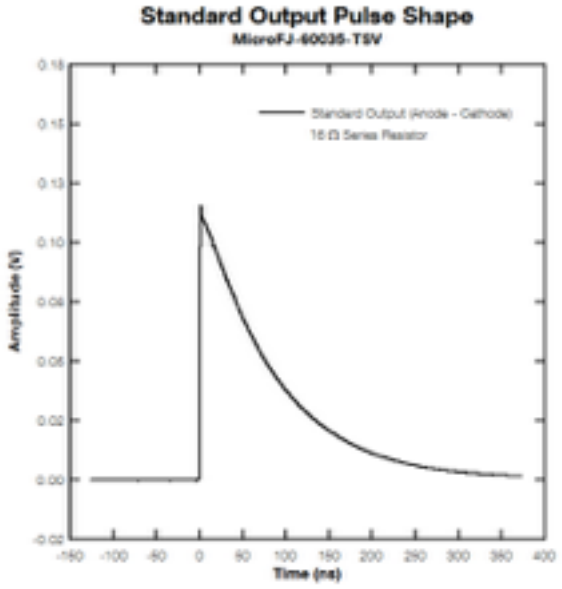


Figure 1: Silicon photomultiplier SMT package from SensL (**left**) and tiling example (**right**). Drawings by SensL.

http://sensl.com/estore/arrayj-60035-64p-pcb/

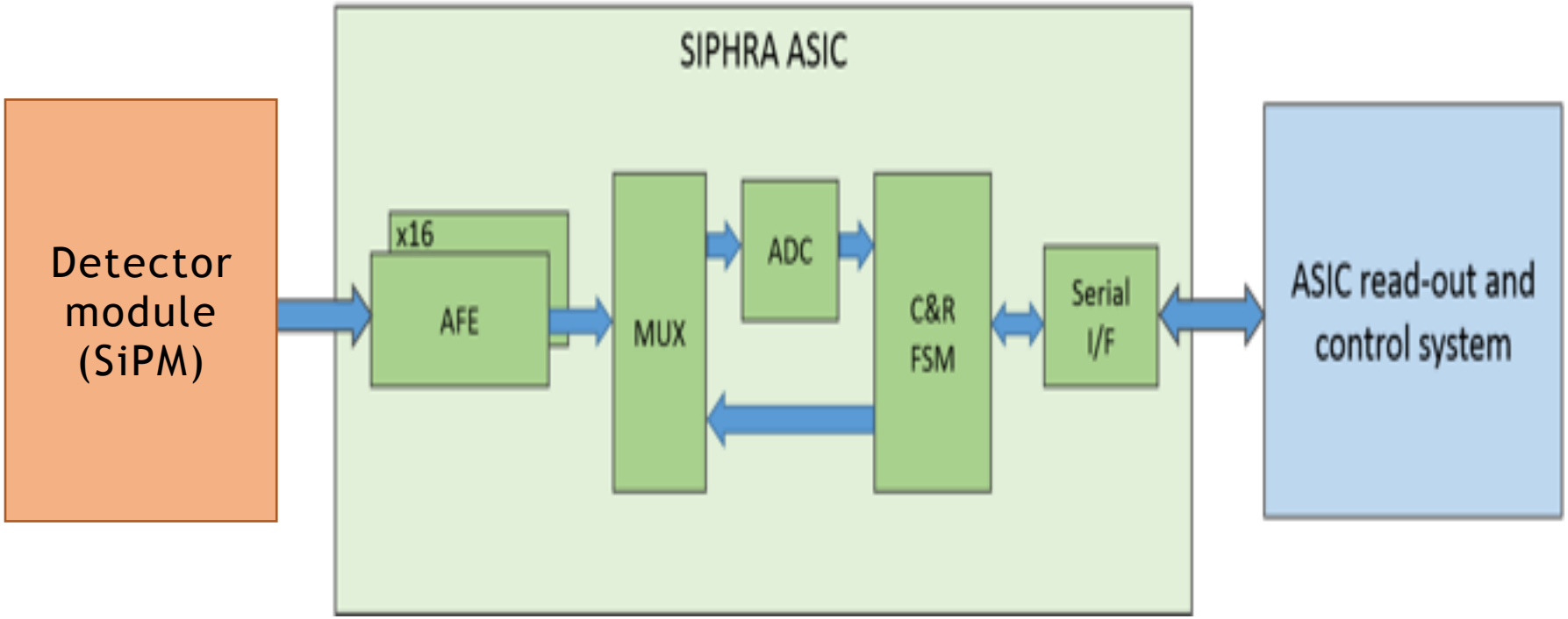


Polished $LaBr_3$ crystals with $n_{refraction}$= 2.3
Optical grease with $n_{refraction}$= 1.46 between crystals/window/sensors
No light absorption in crystals
Light scattering length of 90-150 mm depending on wavelength
Diffuse reflector around crystals with 98% reflectivity (with air gap)
Hermetic seal with 70% diffuse reflectivity



Ulyanov et al., "Study of silicon photomultipliers for the readout of scintillator crystals in the proposed GRIPS gamma-ray astronomy mission", Proc. of Science, arXiv:1302.5786v1

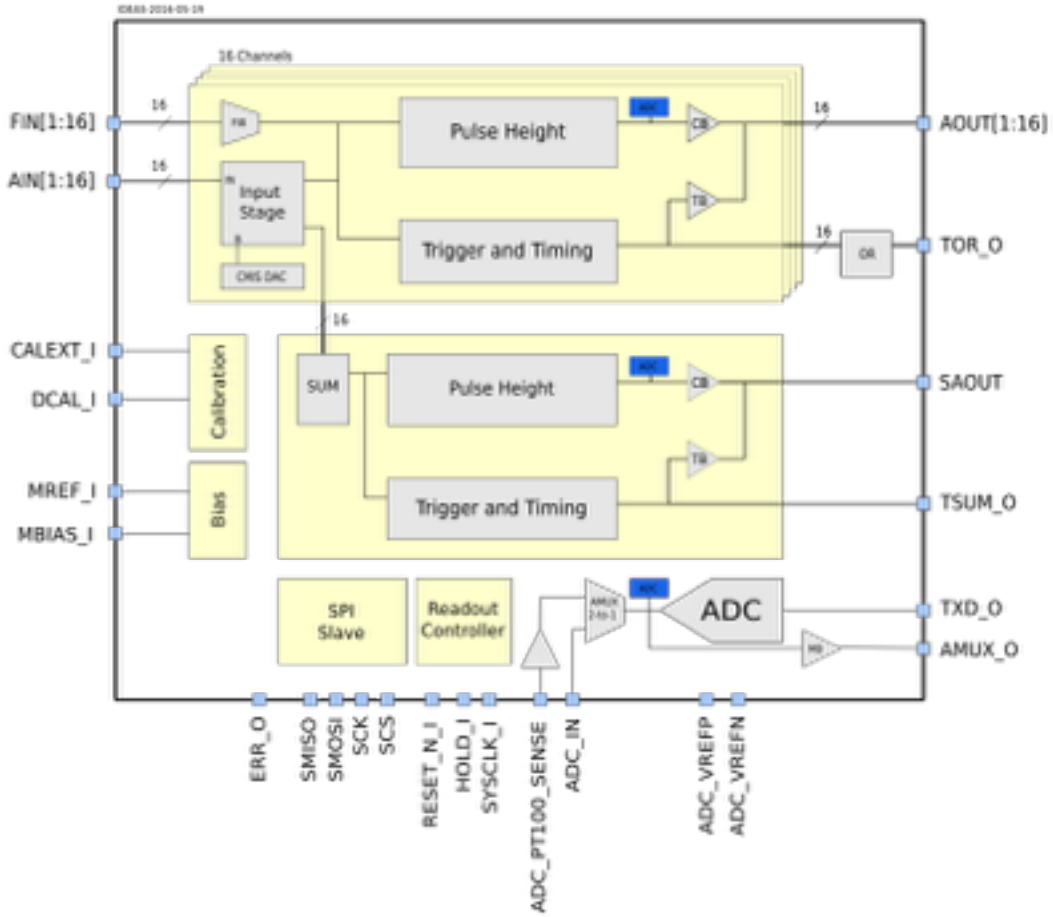
Block Diagram of System Components



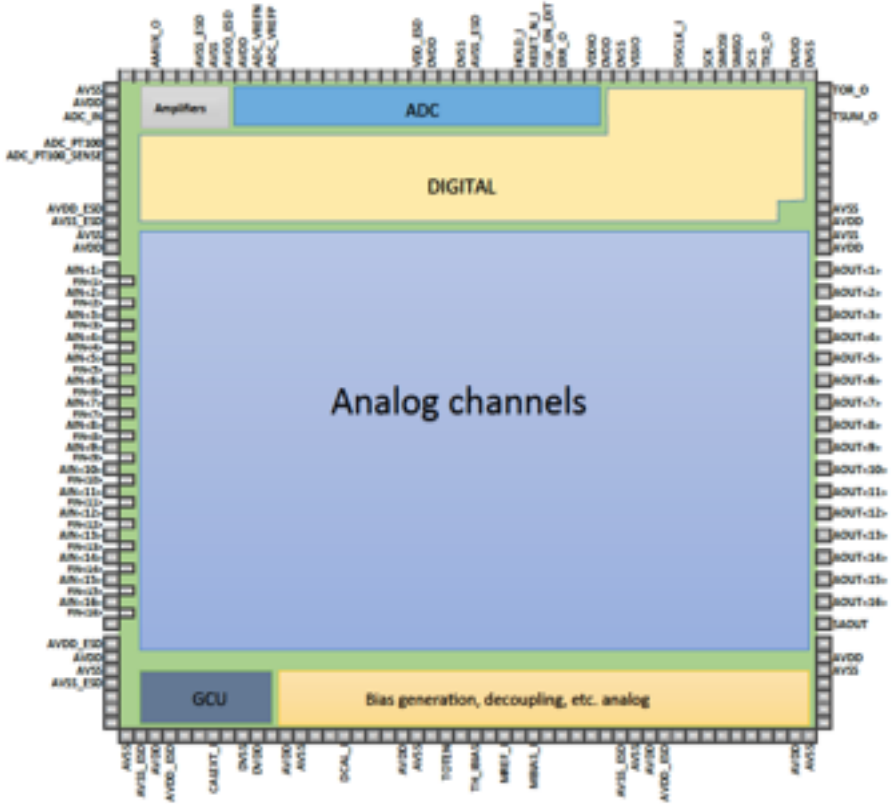
SIPHRA Features and Block Diagram

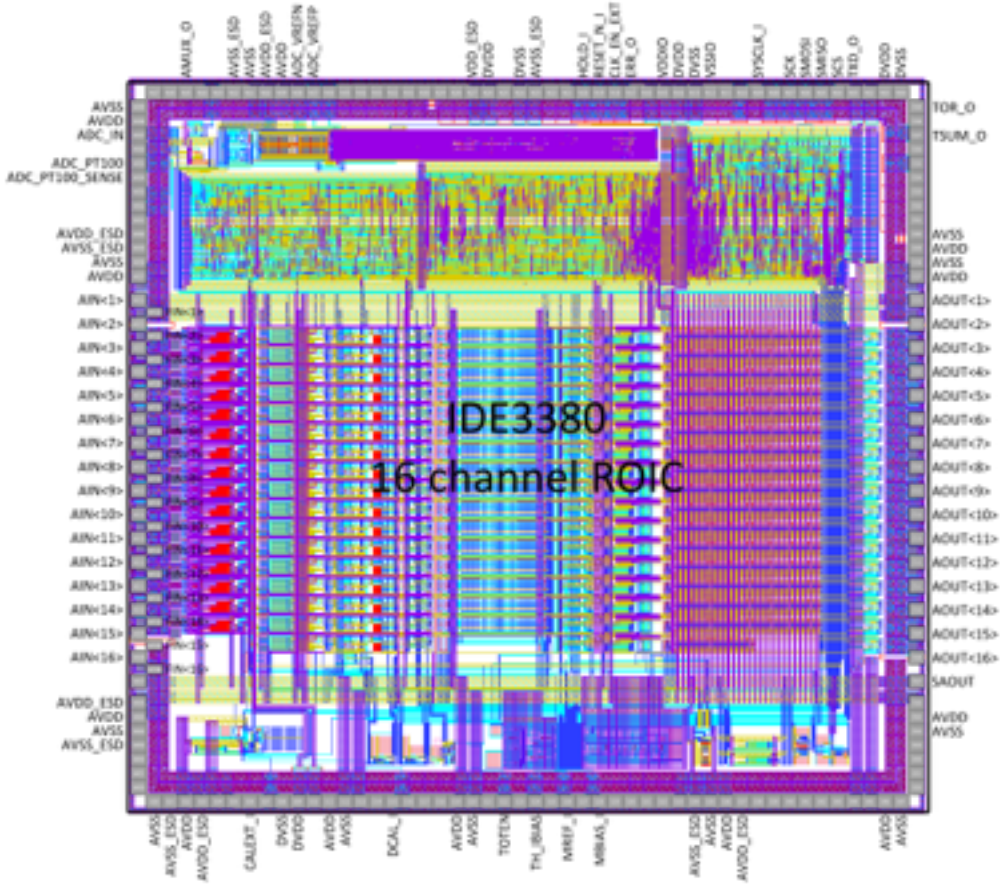
IDE3380 (SIPHRA) Features

- **16 readout channels**
  - 16 current sensitive inputs (≤ 16 nC)
  - 1 summing channel
- **Programmable attenuation to handle charge up to**
  - -16 nC, -8 nC, -4 nC, -400 pC at AIN inputs, or
  - +40 pC, +4 pC, +0.4 pC at FIN inputs
- **Programmable shaping time**
  - 200 ns, 400 ns, 800 ns, 1600 ns
- **16 inputs (AIN) with programmable offset voltage**
- **Pulse height spectroscopy**
  - 16 shapers followed by track-and-hold
  - Programmable hold timing
  - Analog and/or 12-bit digital readout
  - 3 ksps/channel max.
- **Trigger generation**
  - Internal from charge discriminator via programmable threshold in every channel
  - External (trigger on input, trigger on sum)
- **Power**
  - 15 mW without CMIS, 30 mW with CMIS active
  - Flexible power down scheme of channels or functions
- **SEL/SEU radiation hardened**
- **SPI Interface**



SIPHRA Floorplan and Pad Frame





Chip active area: 7.6 mm×6.8 mm, 103 (119[1)]) Pins
Planned Packaging Options: Plastic PQFP120, Bare-Die

[1)] Normally either 16 AIN or 16 FIN inputs will be bonded, not both.

Main Requirements for IDE3380

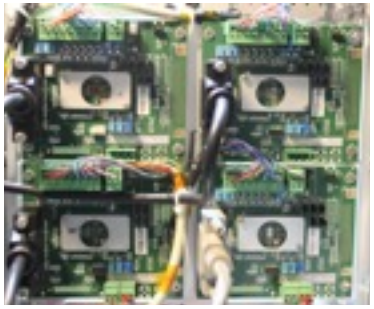
Parameter	Value	Comment
SiPM type	SensL B-60035 MPPC S10943-3183	Note 3.4 nF capacitance. 100 ns decay time constant. Note 12 pF capacitance, using FIN input.
Supply voltage (V)	3.2 V ≤ V ≤ 3.4 V	
Power (W)	<2 mW/channel ~2mW standby	Unused functions can be powered down When power on analog VDD
Temperature	0°C – 60°C	
TID (TID)	5 krad(Si) ≤ TID (req.)	Requirement. Expect much higher tolerance.
SEU LET_{th}	≥ 60 MeVcm^2/mg (req.)	
SEL	Immune	
Number of channels	16 + 1	The ASIC has 16 channels + 1 summing channel.
ADC resolution	12 bits, ENOB > 11 bits	12-bit SAR ADC
ADC conversion rate	50 ksps	Hit rate 1/sec in flight, 1000/sec in test

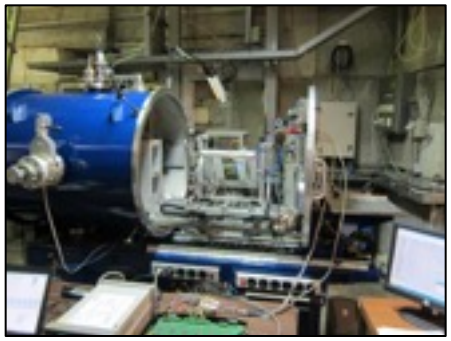
IDEAS Radiation Tolerant Standard Cell Library

- Small Library (<50 cells)
- Synthesis and Implementation with Cadence tools
- Previously Measured Radiation Tolerance:
  - SEU LET_{th} 50 $MeVcm^2/mg$
  - SEL LET_{th} ≥ 135 $MeVcm^2/mg$

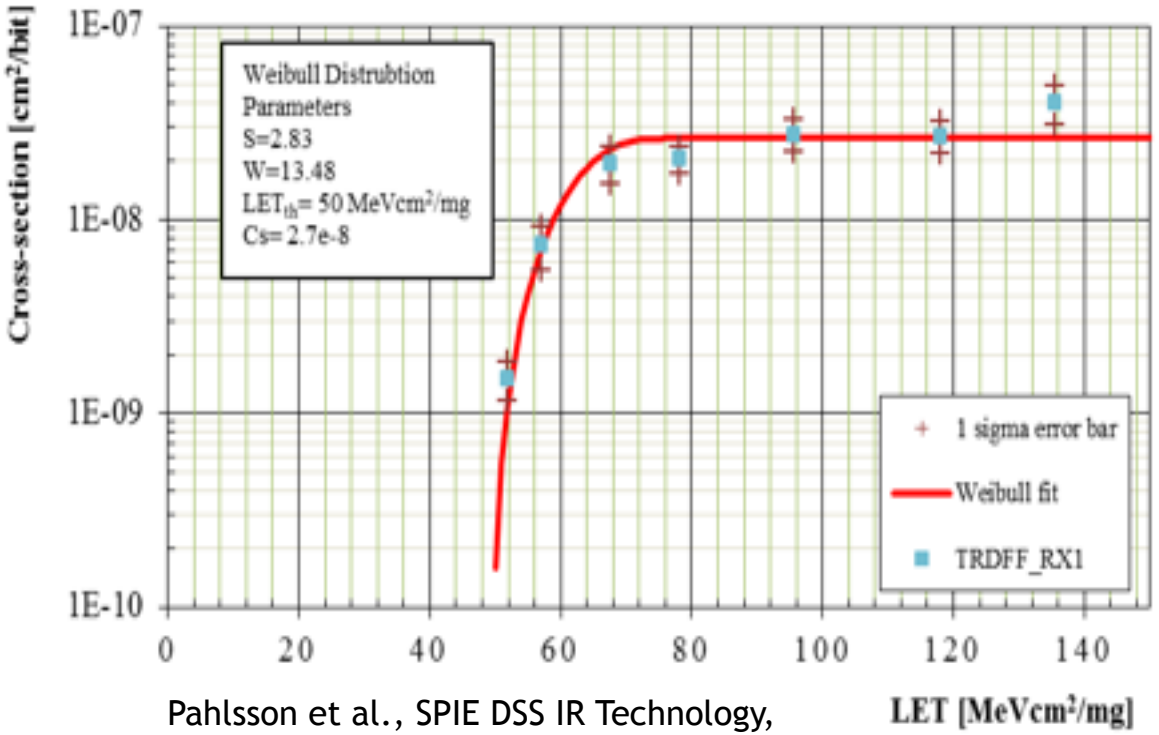
SEE Radiation Tolerance by Design

0.35µm AMS CMOS



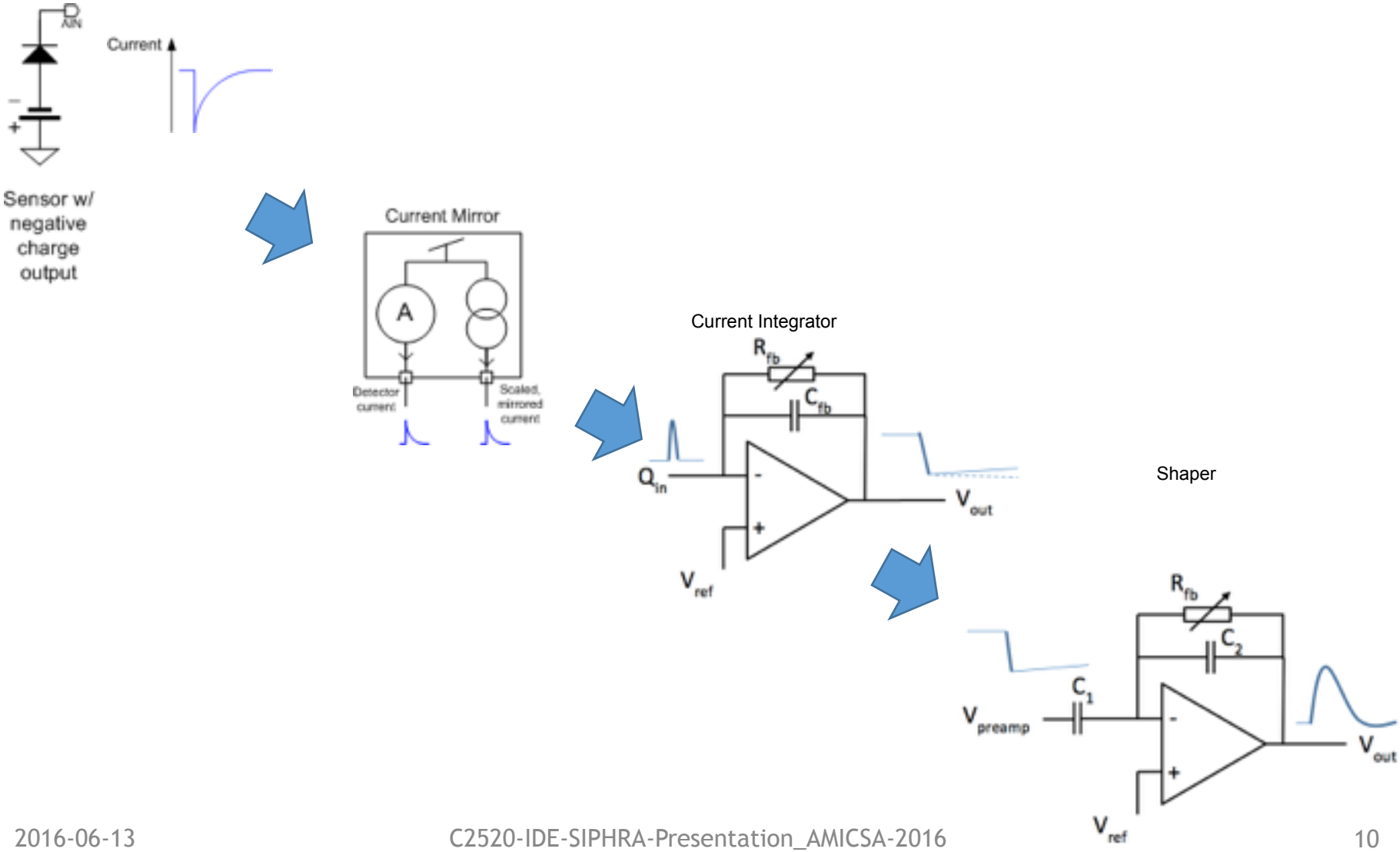


SEE tests at UCL HIF

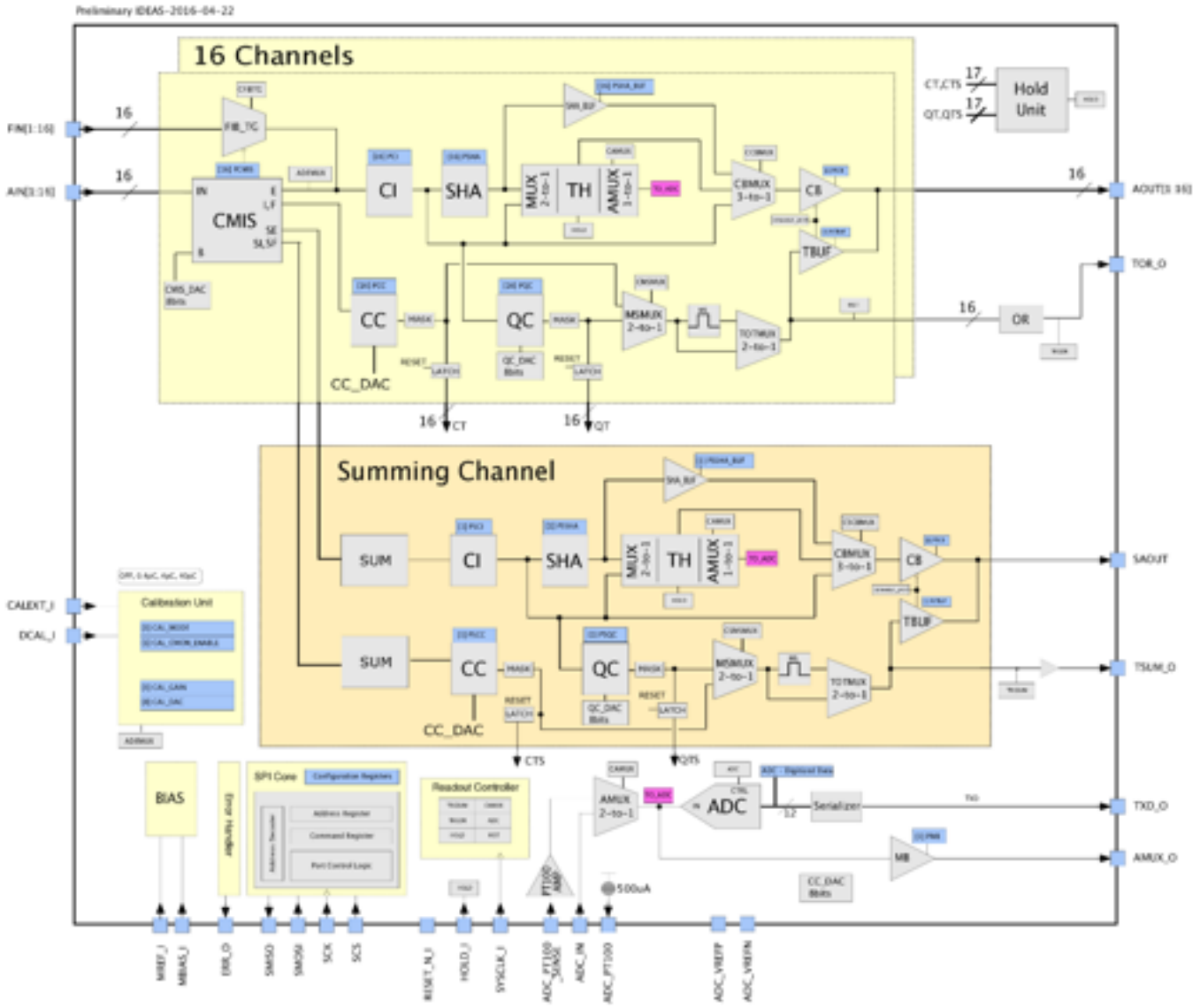


Pahlsson et al., SPIE DSS IR Technology,
http://dx.doi.org/10.1117/12.2180439

Signal Flow


Current
Sensor w/ negative charge output
Current Mirror
A
Detector current
Scaled, mirrored current
Current Integrator
R_{fb}
C_{fb}
Q_{in}
V_{out}
V_{ref}
Shaper
R_{fb}
C_2
C_1
V_{preamp}
V_{out}
V_{ref}

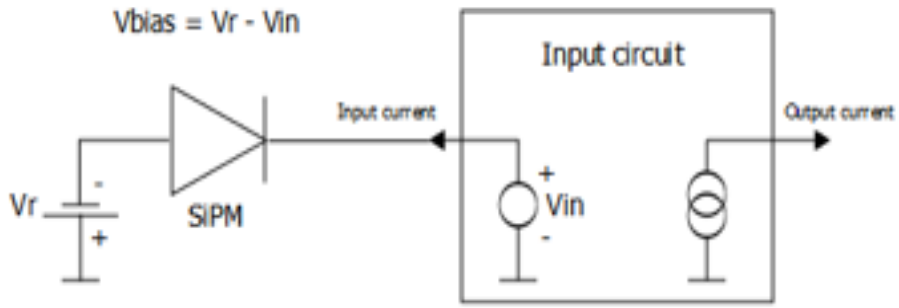
SIPHRA Architecture



CMIS - Current Mode Input Stage

CMIS main functions:

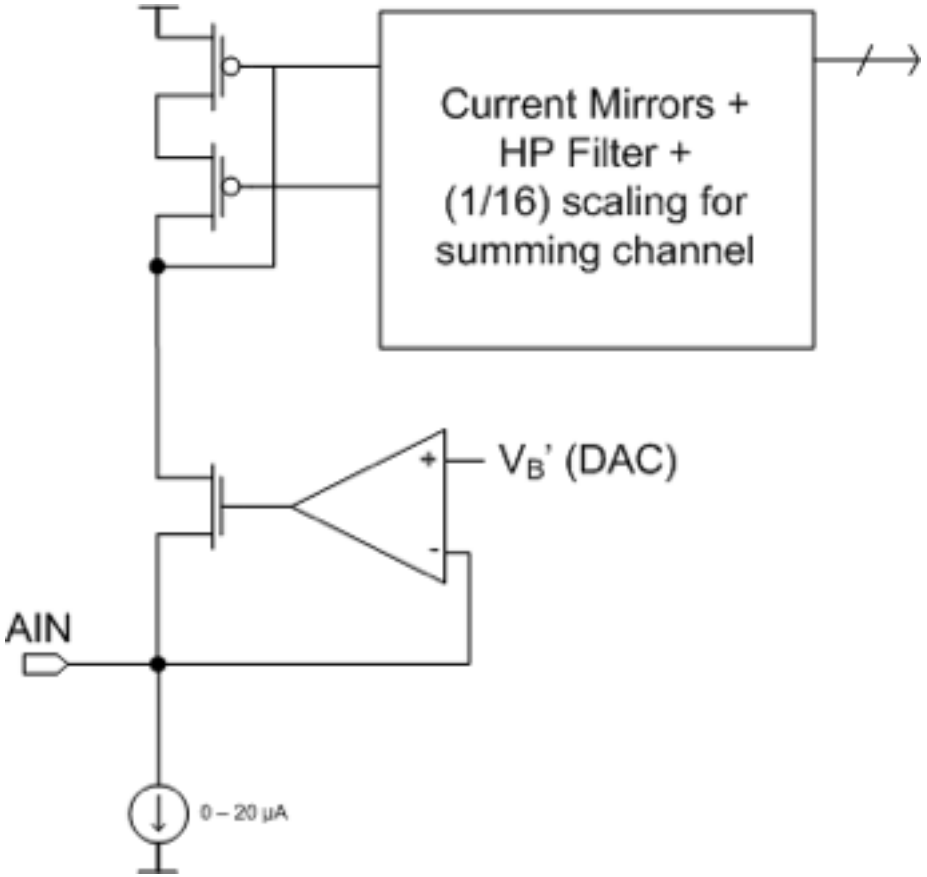
1. to provide a stable programmable input voltage at AIN. The input offset sets the SiPM bias voltage, allowing compensation of breakdown voltage variation among several SiPMs.
2. to scale down the detector current



CMIS performance:

- Designed for large negative charge
  Saturation: −16 nC, −8 nC, −4 nC, −0.4 nC
- Programmable gain attenuation:
  1/10, 1/100, 1/200, and 1/400
- Large capacitive load up to several nF,
- Large leakage current up to −100 µA.
- Input voltage is regulated to a stable bias
  voltage set via an 8-bit DAC over the range of 1 V.
- Input impedance 5..30 Ohm below 10 MHz. Above 10 MHz, input impedance becomes reactive and peaks with a few 100 Ohm at 250 MHz.

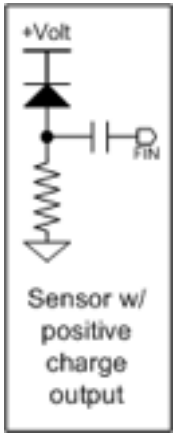
CMIS - Current Mode Input Stage



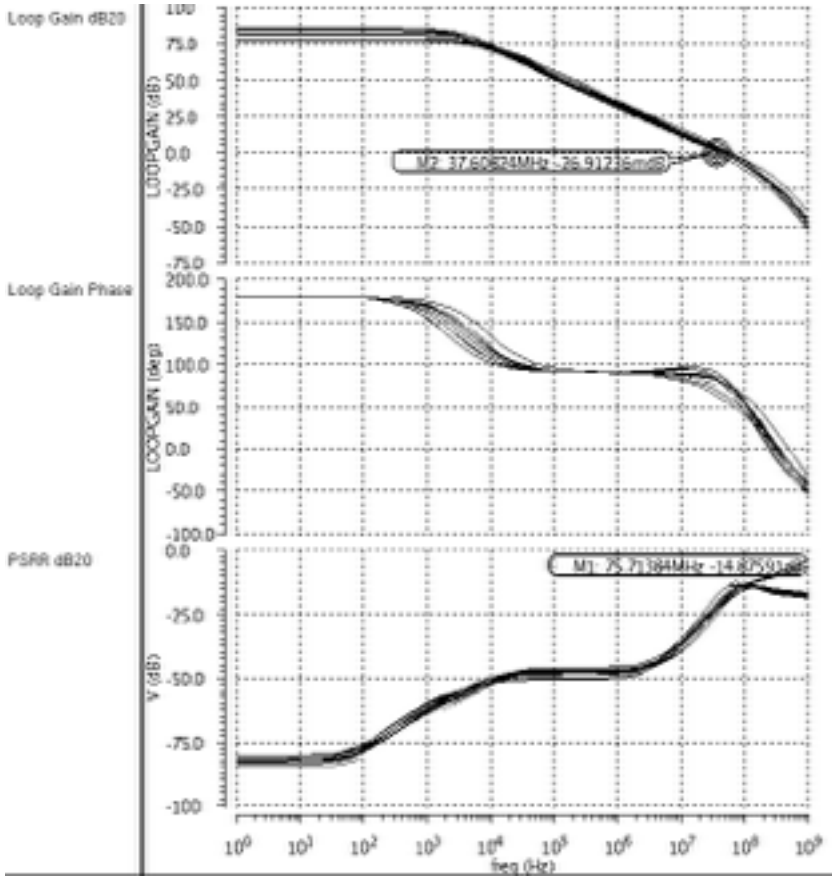
- Common-gate input (regulates DC bias)
  - Input voltage is regulated to a stable bias voltage set via an 8-bit DAC
    over the range of 1 V.
- Bias current 0-20µA.
  - Needed to keep current mirror ready for fast transients.

Current integrator, stand-alone

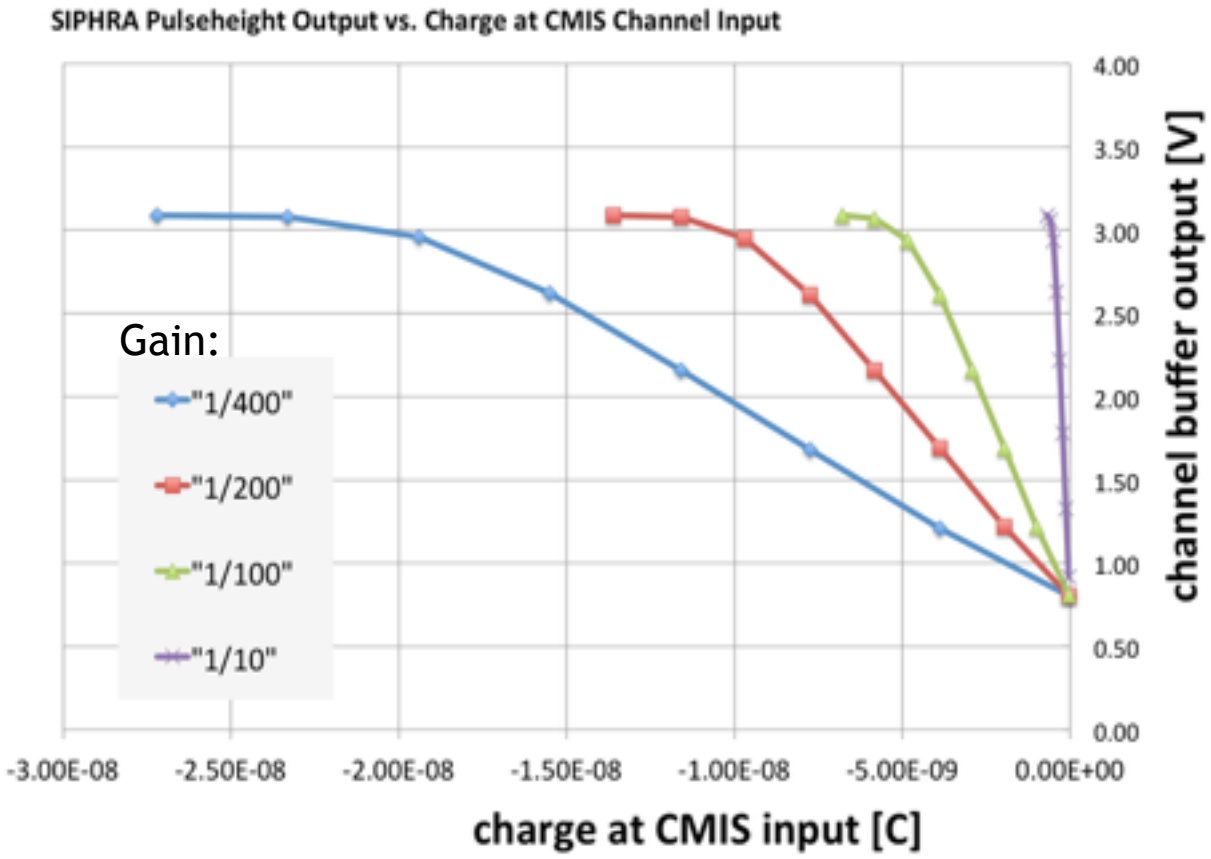
Parameter	Input load	Setting	Typical simulation result
Gain, peak		-1 V/750fC -1 V/3pC -1 V/30pC	-0.941 V/750fC -0.954 V/3pC -0.959 V/30pC
Non-linearity (full-scale, resistive feedback)		1V/750fC 1V/3pC 1V/30pC	<= 0.02%
Input/Output voltage range		2V/2V-0.7V	2V/2V-0.5V was used
Noise Eno (Vrms) (ideal gain values, ideal VREF)	14 pF 14 pF 14 pF 0.3 pF	1V/750fC 1V/3pC 1V/30pC 1V/30pC	648 µVrms 355 uVrms 86.3 uVrms 111 uVrms *(CB buffer Eno=157 µVrms)*
Noise ENC	14 pF 14 pF 14 pF 0.3 pF	1V/750fC 1V/3pC 1V/30pC 1V/30pC	486 aC (3.04k e) 1.07 fC (6.66k e) 2.59 fC (16.2k e) 3.33 fC (20.8k e)
Phase Margin	14 pF 14 pF 14 pF 0.3 pF	Min 1V/750fC Min 1V/3pC Min 1V/30pC Min 1V/30pC	>89.0 >68.6 >71.82 >62.59
Open-loop gain			>76 dB
PSRR		1V/30pC	>45 dB below 1 MHz
Power consumption		typical peak powerdown	468 uW < 3 mW 100 pW



SIPHRA mode (1V/30pC) corner simulations.
Lot-to-lot variation, 0˚C-60˚C



Dynamic Range, Trigger Range



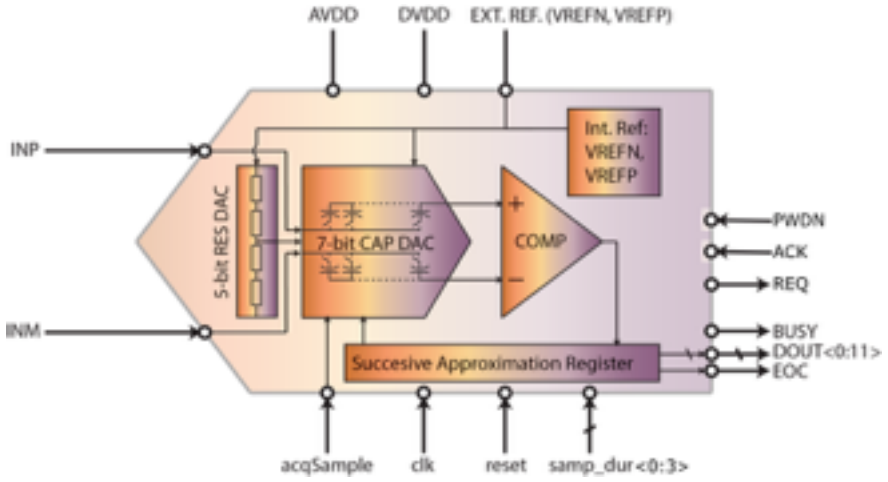
CMIS gain	Trigger threshold charge range	
	Minimum	Maximum
1/10	-4 pC	-560 pC
1/100	-43 pC	-5.4 nC
1/200	-87 pC	-10.8 nC
1/400	-175 pC	-20.9 nC

Dynamic Range, Noise

- Analog readout:
  - Dynamic range 65 dB – 78 dB (simulation)
- Digital readout:
  - 10.8 bit – 11.5 bit (ADC limit)
- Cross-talk 0.1%
  - Post-Layout simulation (Ideal supply, Excl. package bonds, leads.)

CMIS gain	Shaping time [ns]	Saturation charge [pC]	ENC [pC]	Dynamic range	Dynamic range [dB]
1/10	200	-510	0.24	2125	66.5
	400		0.28	1823	65.2
	800		0.28	1797	65.1
	1600		0.28	1841	65.3
1/100	200	-4980	0.83	6000	75.6
	400		0.73	6822	76.7
	800		0.67	7433	77.4
	1600		0.63	7904	78.0
1/200	200	-9830	1.62	6068	75.7
	400		1.40	7021	76.9
	800		1.28	7680	77.7
	1600		1.18	8331	78.4
1/400	200	-19500	3.27	5963	75.5
	400		2.80	6964	76.9
	800		2.56	7617	77.6
	1600		2.37	8228	78.3

12 bit ADC
50+ ksps

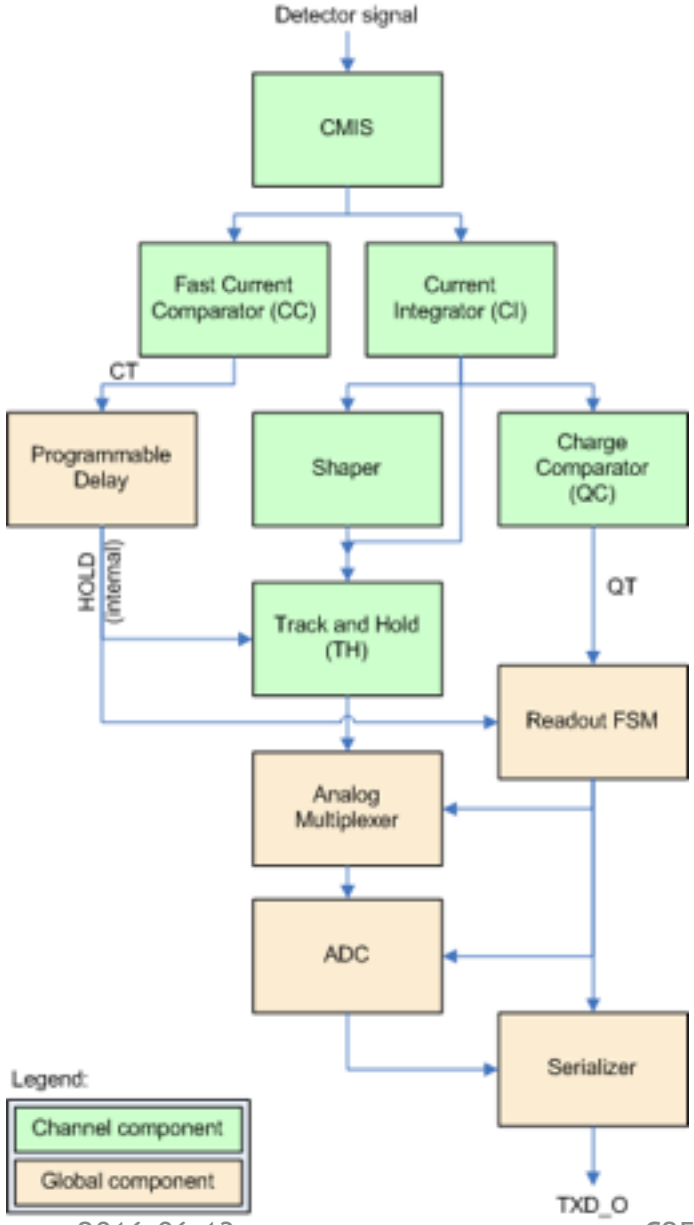


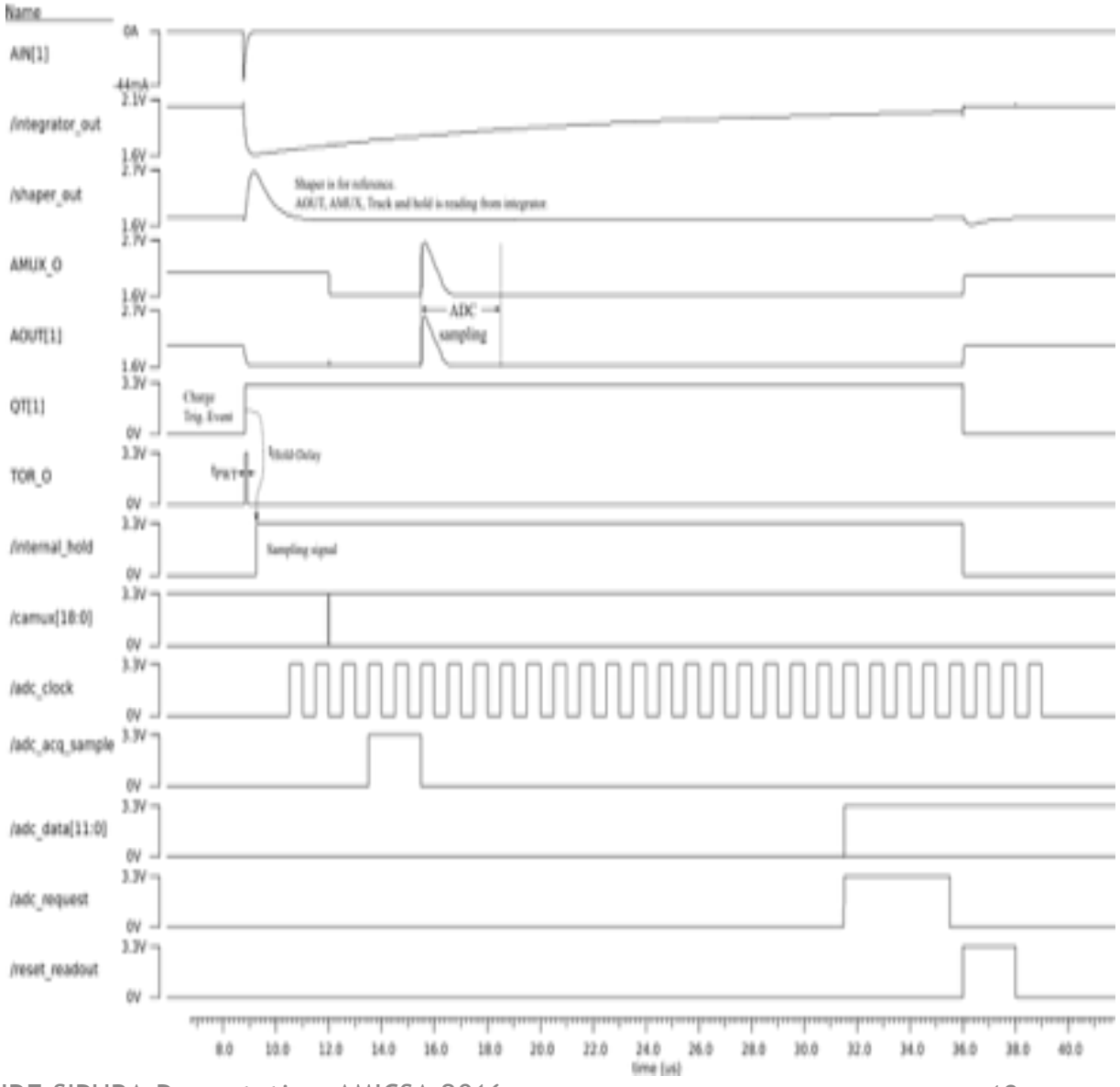
Simulated parameters:

Parameter	MIN	TYP	MAX
Resolution		12-bit (11 ENOB)	
Supply voltage	2.7 V	3.3 V	3.6 V
Positive voltage reference (VREFP)	2.15 V	2.65 V	AVDD
Negative voltage reference (VREFN)		0.65 V	1.15 V
Voltage reference difference (VREFP-VREFN)	1 V	2V	AVDD
Impedance between VREFP and VREFN	0.83*TYP	96 kΩ	1.25*TYP
Input voltage range (differential)	±1 V	±2 V	± (AVDD-100 mV)
Input voltage range (single-ended)	1 V	2 V	AVDD-100 mV
Input voltage	100 mV	-	AVDD
Input capacitance	0.9*TYP	11.5 pF (sample mode) 1 pF (hold mode)	1.1*TYP
Input resistance	0.9*TYP	430 Ω	1.1*TYP
Sampling frequency	-	50 ksps	100 ksps
DNL	± 0.25 LSB	± 0.5 LSB	± 1 LSB
INL	± 0.5 LSB	± 0.75 LSB	± 1 LSB
Offset error	1 LSB	0.5 LSB	1 LSB
Gain error	1 LSB	0.5 LSB	1 LSB
Average power consumption (VDD = 3.3 V)		< 1 mW @ 50 ksps	
Average power consumption (standby mode)	-	29 µW (@ 1 kHz hit rate. clock active 1 MHz during sleep)	-
Average power consumption (power down mode)	-	3 µW (clock active. 1 MHz) 10 nW (clock off)	-
Temperature range	-20 °C	25 °C	60 °C

[1] Standby mode is when the ADC and its reference buffers are subjected to intermediate wake ups, in order to be able to wake up within one clock cycle (given Tclk > 1 us).

Digital Readout Flow





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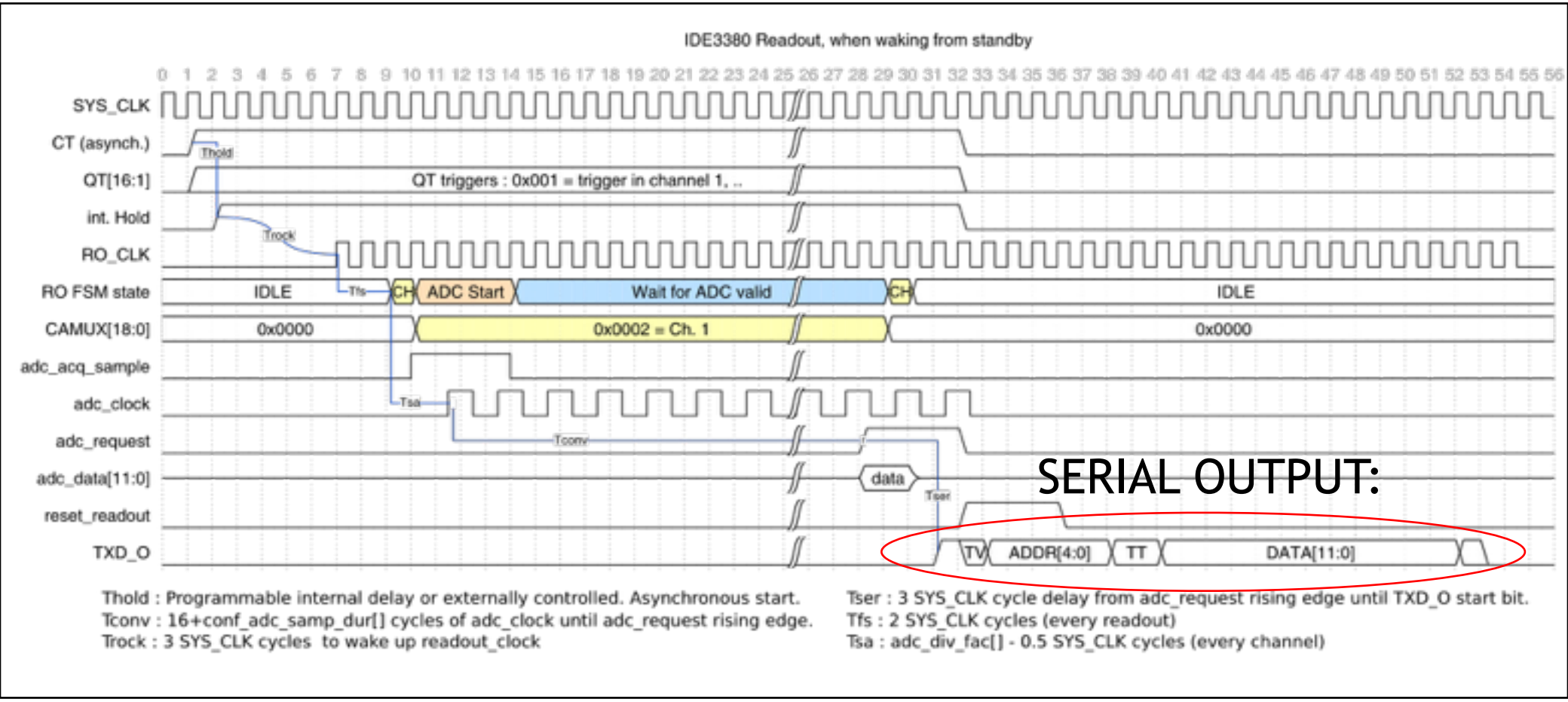
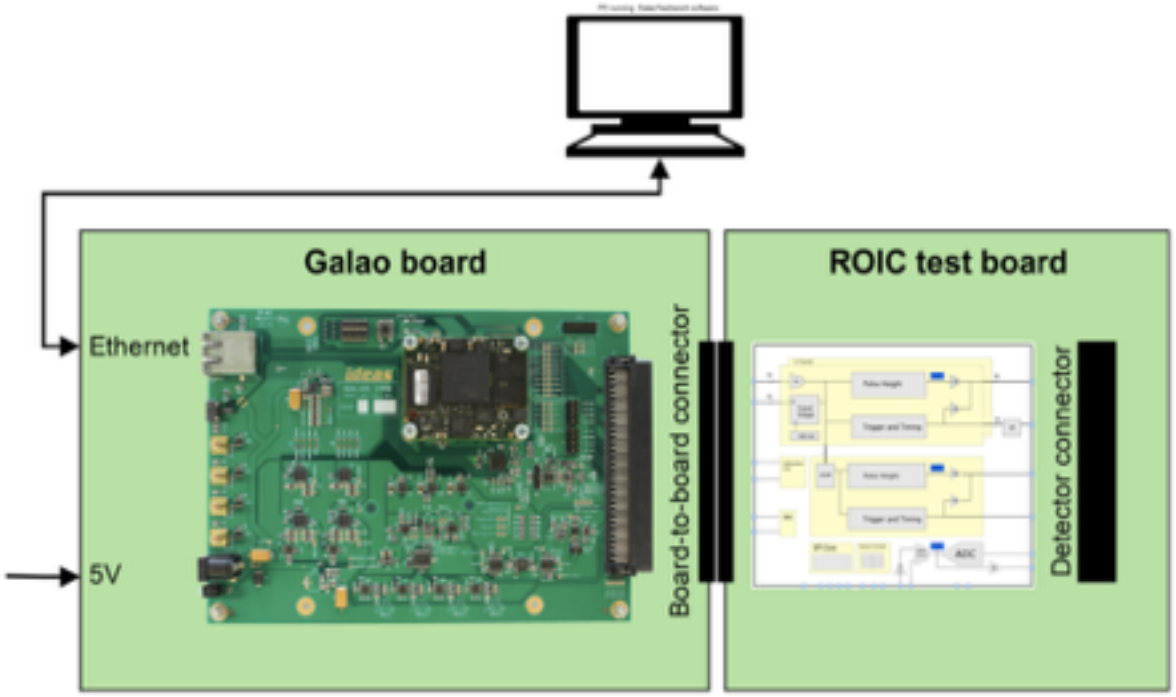
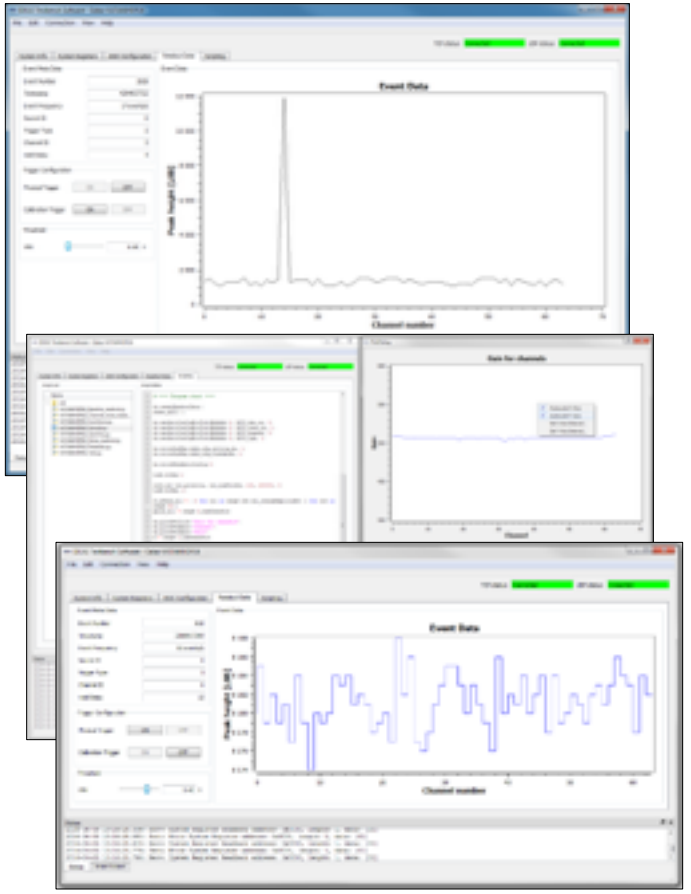


IDE3380 Test System



Block diagram of the ASIC design validation and test system.



Software
(Python Scripting,
LabView API)

The ASIC design validation is scheduled for the fall 2016, using IDEAS Galao development kit to interface to TOIC test PCB. The Galao development kit is based on the Xilinx Zynq-7000 with custom firmware for the SIPHRA ASIC readout and control. The system is controlled via Ethernet (GbE) from a computer. The SIPHRA ASIC is located on the ROIC test board, which allows one to connect to the detector array.

References

1. J. Greiner et al., “GRIPS Gamma-Ray Imaging, Polarimetry and Spectroscopy”, arXiv:1105.1265, see also http://www.grips-mission.eu
2. Xin Wu et al., “PANGU: A High Resolution Gamma-ray Space Telescope”, arXiv:1407.0710v2, 17. Jul 2014.
3. S. Zhang et al., "The High Energy cosmic-Radiation Detection (HERD) Facility onboard China's Future Space Station", arXiv:1407.4866 , 18. Jul 2014.
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We would like to acknowledge the support from the European Space Agency (ESA contract number 4000113026), the Norwegian Space Center (contract number BAS.05.14.1), and the University of Geneva.

IDE3380 (SIPHRA) is now in manufacturing and we expect first samples July 30.

Thank You

www.ideas.no
hans.berge@ideas.no

THE END