Radiation Hardened High-Voltage and Mixed-Signal IP with DARE technology

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Background

- Commercial CMOS technologies for mixed-signal and high-voltage radiation applications
  - Low cost / high yield
  - High speed
  - Low power
  - Thin-gate oxide technologies => high TID tolerance

- Need for an IP eco system to enable re-use and reduce cost for full SoC developments
  - Standard design flow in standard technologies (ADK, PDK)
  - Silicon-proven hardened digital libraries
  - Silicon-proven hardened analog, mixed-signal and high-voltage IP
IP in imec DARE solution

imec DARE (Design Against Radiation Effects) [see previous AMICSA proceedings]

- DARE180U in UMC 0.18um CMOS technology
  - No high-voltage capabilities
  - > 1 Mrad => ELT devices => high power consumption
  - No NVM
  - Digital libraries and memory compilers available
- DARE180X in XFAB XH018 0.18um BCD technology
  - > 100kRad => lower power
  - High-voltage BCD
  - Non-volatile memory
  - Digital libraries available
- I3t80 On semiconductor 0.35um BCD
  - 80V devices available
  - No digital library
IP in imec DARE solution

- ICsense analog, mixed-signal and high-voltage IP in DARE180U and DARE180X
- All IP blocks developed for the DPC of Thales Alenia Space Belgium (ETCA)
  - 13 bit, 1MSps ADCs
  - 120MHz PLL with ultra-low SET sensitivity (no glitches)
  - 12 bit, 3.75MHz DACs
  - Voltage and current references with embedded temperature sensor
  - 100kHz accurate RC oscillator
  - 3.3V – 1.8V linear regulators for analog and digital supplies
  - Inductive DCDC converters for secondary supply conversion to 3.3V and 1.8V (DARE180X only)
  - Drivers up to 18V (DARE180X only)
  - Other auxiliaries (comparators, buffers, filters, PGAs, levelshifters, ....)
IP in imec DARE solution

Analog, mixed-signal and high-voltage IP in i3t80 ON Semiconductor

• ADK has been developed by imec
• Allows for high-voltage ASIC developments in Cadence design flow
• Contains:
  • ELT pcells for nmos and pmos
  • ELT for NDMOS
  • Octogonal devices for IO cells
  • Calibre decks have been updated for
    • ELT integration
    • Guard rings
    • N-to-n type leakage
• Used to developed a high-voltage, rad-hard ASIC with max. voltage of 40V and several amps
• SEGR and SEB minimization
Availability of IPs in (X)DARE180

- Supported ICsense analog, mixed-signal and high-voltage IP in DARE180U and DARE180X
  - 13 bit, 1MSps ADC
  - 120MHz PLL with ultra-low SET sensitivity (no glitches)
  - 12 bit, 3.75MHz DAC
  - Voltage and current references with embedded temperature sensor
  - 3.3V – 1.8V linear regulators for analog and digital supplies

- IP in DARE180U is **silicon and radiation proven**!
- IP in DARE180X is under development
- Product briefs available
- Deliverables: datasheets, VerilogAMS model, integration guidelines, encrypted Spectre netlist
Linear regulators

- **Digital supply**
  - 3.3V to 1.8V
  - Current up to 700mA
  - Area 4.7mm² against thermal degradation

- **Analog supply**
  - 3.3V to 1.9V
  - Current up to 30mA

- Package changes or current changes require simulations/redesign
PLL

- Long-term frequency spikes and phase shifts due to SET are minimized
  - Simulation example with ICsense proprietary SET flow
  - 60MeV cm²/mg strike at 1us
- Input: 100kHz accurate oscillator or Xtal
- Tailoring of frequency possible

<table>
<thead>
<tr>
<th>Spec</th>
<th>Unit</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>mm²</td>
<td>-</td>
<td>2.3</td>
<td>-</td>
<td></td>
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<tr>
<td>Supply PLL</td>
<td>V</td>
<td>1.8</td>
<td>1.9</td>
<td>1.98</td>
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<tr>
<td>PLL current consumption</td>
<td>mA</td>
<td>-</td>
<td>-</td>
<td>13.8</td>
<td></td>
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<tr>
<td>PLL frequency range when locked</td>
<td>MHz</td>
<td>-0.5%</td>
<td>120</td>
<td>+0.5%</td>
<td>Aging and TID effects not included</td>
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<tr>
<td>PLL frequency range during SET when locked</td>
<td>MHz</td>
<td>-3%</td>
<td>120</td>
<td>+3%</td>
<td>Deviation immediately after SET event</td>
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<tr>
<td>Cycle to cycle jitter</td>
<td>fs</td>
<td>-</td>
<td>-</td>
<td>400</td>
<td></td>
</tr>
<tr>
<td>Spurious free dynamic range</td>
<td>dB</td>
<td>100</td>
<td>-</td>
<td>-</td>
<td></td>
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</table>
13 bit, 1MSps ADC

- Cyclic topology with input S&H
  - Integrated reference buffer
  - No external components
  - Requires the voltage reference from ICsense

- SET behavior
  - ADC controller cannot enter a locked state
  - Max 3 ADC samples are affected by an SET strike
  - Multiplexers are hardened

<table>
<thead>
<tr>
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<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Comment</th>
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</thead>
<tbody>
<tr>
<td>Area</td>
<td>mm²</td>
<td>-</td>
<td>0.425</td>
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<tr>
<td>Current consumption ADC</td>
<td>mA</td>
<td>-</td>
<td>-</td>
<td>6.0</td>
<td></td>
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<tr>
<td>Resolution</td>
<td>bits</td>
<td>-</td>
<td>13</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>LSB</td>
<td>mV</td>
<td>-</td>
<td>0.330</td>
<td>-</td>
<td>At the input of S/H</td>
</tr>
<tr>
<td>Sample rate</td>
<td>MS/s</td>
<td>-</td>
<td>-</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>INL (differential) / (single-ended)</td>
<td>LSB</td>
<td>-</td>
<td>-</td>
<td>4.0 / 6.2</td>
<td></td>
</tr>
<tr>
<td>DNL</td>
<td>LSB</td>
<td>-</td>
<td>-</td>
<td>1.5</td>
<td></td>
</tr>
<tr>
<td>SNDR (differential) / (single-ended)</td>
<td>dB</td>
<td>-</td>
<td>73 / 67.5</td>
<td>- 100kHz</td>
<td></td>
</tr>
</tbody>
</table>
P-type current-steered 12-bit DAC

- With DEM: 58.6kHz data rate
- Without DEM: 3.75 MHz data rate

<table>
<thead>
<tr>
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<th>Max</th>
<th>Comment</th>
</tr>
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<tbody>
<tr>
<td>Area</td>
<td>mm²</td>
<td>-</td>
<td>0.39</td>
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</tr>
<tr>
<td>Current consumption</td>
<td>mA</td>
<td>-</td>
<td>4.2</td>
<td>4.5</td>
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<tr>
<td>Resolution</td>
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<td>-</td>
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<tr>
<td>LSB</td>
<td>µA</td>
<td>0.93</td>
<td>0.98</td>
<td>1.03</td>
<td>P-type current</td>
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<tr>
<td>Full scale</td>
<td>mA</td>
<td>3.8</td>
<td>4</td>
<td>4.2</td>
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</tr>
<tr>
<td>Output range</td>
<td>V</td>
<td>0</td>
<td>-</td>
<td>2.5</td>
<td>Compliance voltage of 0.5V</td>
</tr>
<tr>
<td>Data rate no DEM/DEM</td>
<td>MS/s</td>
<td>-</td>
<td>3.75/0.058</td>
<td>-</td>
<td></td>
</tr>
<tr>
<td>DNL no DEM/DEM</td>
<td>LSB</td>
<td>-</td>
<td>-</td>
<td>2 / 0.75</td>
<td></td>
</tr>
<tr>
<td>INL no DEM/DEM</td>
<td>LSB</td>
<td>-</td>
<td>1.5 / 1.06</td>
<td>1.7 / 1.26</td>
<td>Output buffer @ output</td>
</tr>
</tbody>
</table>
Voltage and current reference

- Bandgap voltage of 1V
  - Reference distribution with current possible
- Bias block of 47 output currents of 10uA
- Temperature sensor embedded
- SET behavior
  - SET cannot trigger unwanted shutdown/start
  - Only minor glitches on BG voltage

### Specification Table

<table>
<thead>
<tr>
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<th>Typ</th>
<th>Max</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Area</td>
<td>mm²</td>
<td>-</td>
<td>1.67</td>
<td>-</td>
<td>-</td>
</tr>
<tr>
<td>Current consumption</td>
<td>mA</td>
<td>1.65</td>
<td>2.0</td>
<td>2.55</td>
<td></td>
</tr>
<tr>
<td>Nominal reference voltage (Vbg)</td>
<td>V</td>
<td>0.9874</td>
<td>1.0075</td>
<td>1.0277</td>
<td></td>
</tr>
<tr>
<td>Vbg integrated noise 1Hz - 1 GHz</td>
<td>μV rms</td>
<td>15.840</td>
<td>19.250</td>
<td>23.792</td>
<td></td>
</tr>
<tr>
<td>Vbg min, PSRR 1Hz - 120MHz</td>
<td>dB</td>
<td>34</td>
<td>-</td>
<td>-</td>
<td>PSRR @DC &gt;60dB</td>
</tr>
<tr>
<td>Vbg temperature drift -20-110°C</td>
<td>ppm</td>
<td>-887</td>
<td>-</td>
<td>984</td>
<td>After 2nd order digital compensation</td>
</tr>
<tr>
<td>Error of temperature sensor in temperature range -20-110°C</td>
<td>°C</td>
<td>-0.81</td>
<td>-</td>
<td>1.01</td>
<td>After digital compensation.</td>
</tr>
</tbody>
</table>
High-voltage power management in DARE180X

- Input voltages from 4 to 16.5 V
  - XFAB XH018 45V devices used to minimize SEGR

- Different blocks:
  - High-voltage regulator: 4-16.5V to 3.3V for low power blocks (max 3.5mA)
  - Shunt regulator for intermediate voltages
  - Hysteretic 1.8V inductive buck DCDC converter: 3-16.5V to 1.8V
    - maximum load current of 600 mA
    - efficiency of 70-86% for different load conditions
  - Hysteretic 3.3V inductive buck DCDC converter: 4V-16.5V to 3.3V
    - maximum load current of 350mA
    - efficiency of 86-94% for different load conditions
  - High-voltage driver up to 125mA and 16.5V
High-voltage power management in DARE180X

- Radiation hardness using ICsense proprietary rad hard simulation methodology
  - Effect of SET on output voltage is only +- 0.2%
  - Digital controller: rad hard cells only for static signals
  - For bias nodes of critical blocks (gm cells):
    - Filtering techniques
    - Higher currents in bias currents
      - Fast startup
      - Lower voltage peaks
  - Current sense: LPF for deglitching the output
  - Deglitched and hardened Schmitt triggers at the output
  - Soft start is hardened to limit startup currents
Rad Hard high-voltage in i3t80

Driver ASIC to drive up to 40V and several amps of current

Features:
- Very low-ohmic high-voltage switches
  - VGS < 3.3V. Floating switches
- 4KV HBM ESD (high- and low-voltage)
- Minimal number of external components
- Maximal integration: bandgap refs, amplifiers, POR, regulator, reference buffers, level shifters, test

Rad hard measures:
- SEGR minimization: stacked NDMOS
- Bandgap, POR and levelshifters: SET proof through filtering techniques

Measurements ongoing
Conclusions

Blocks available and can be purchased through imec:
- 13 bit, 1MSps ADC
- 120MHz PLL with ultra-low SET sensitivity (no glitches)
- 12 bit, 3.75MHz DAC
- Voltage and current references with embedded temperature sensor
- 3.3V – 1.8V linear regulators for analog and digital supplies (not standalone)

- UMC 0.18 IP: silicon and radiation proven
- XFAB XH018 IP: under development
- I3t80 high-voltage ASIC: proven in silicon
- Radiation hard design through the proprietary ICsense under-radiation simulation flow
Acknowledgements

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  - Imec: Geert Thys, Steven Redant

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  - The XFAB XH018 developments

- RUAG Space Sweden

- ESA for all support
  - Richard Jansen

- Flanders Investment & Trade
ASIC for mining industry
(Sealevel -4 km)

Cancer cell detection ASIC
(Sealevel)

RFID ASIC for airplanes
(Sealevel + 10 km)

ASIC 9-DOF IMU MEMS
(Sealevel)

Satellite motor control ASIC
(Sealevel + 160 km)

Gas sensor ASIC
(Sealevel)

Electronic compass ASIC
(Sealevel)
Corporate overview

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SET simulations flow at ICsense

- Inject double exponential current with total charge depend on LET
- Flow procedure for building block SET simulations
  - Typical conditions: inject in every node to produce short list of sensitive nodes
  - SET simulations for all sensitive nodes over PVT.
  - Adapt design if needed
- Re-inject all nodes in worst-case corners
- Clock signals: vary also injection time relative to clock period
- Top level: check e.g. if SET on bandgap does not influence PLL
- Fully automated flow integrated into our MATLAB driven design environment