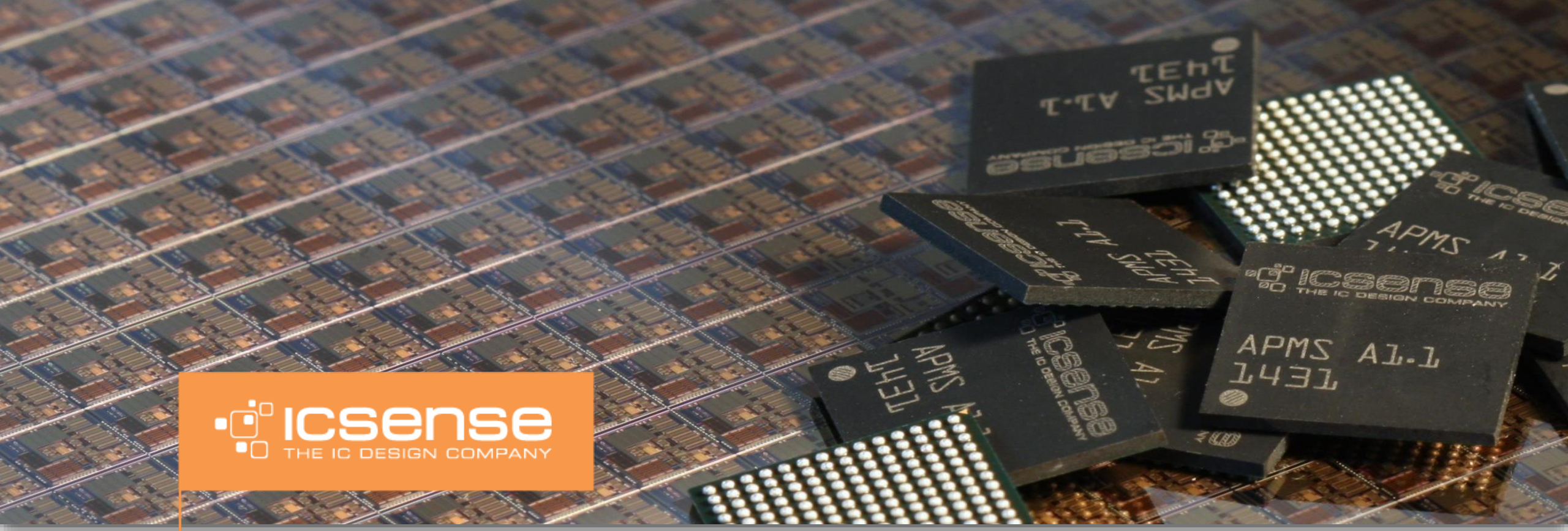


Radiation Hardened High-Voltage and Mixed-Signal IP with DARE technology

Bram De Muer, CEO
AMICSA 2016, 14/06/16

Background

- Commercial CMOS technologies for mixed-signal and high-voltage radiation applications
  - Low cost / high yield
  - High speed
  - Low power
  - Thin-gate oxide technologies => high TID tolerance

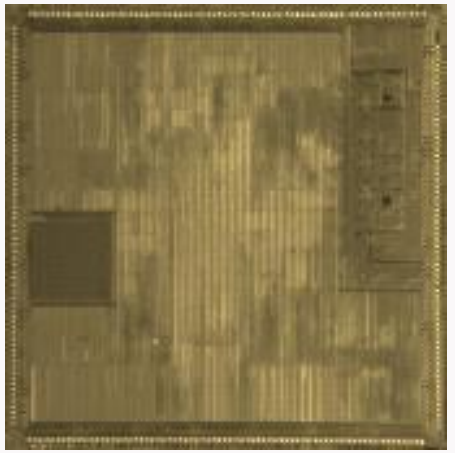
- Need for an IP eco system to enable re-use and reduce cost for full SoC developments
  - Standard design flow in standard technologies (ADK, PDK)
  - Silicon-proven hardened digital libraries
  - Silicon-proven hardened analog, mixed-signal and high-voltage IP

IP in imec DARE solution

- imec DARE (Design Against Radiation Effects) [see previous AMICSA proceedings]
  - DARE180U in UMC 0.18um CMOS technology
    - No high-voltage capabilities
    - > 1 Mrad => ELT devices => high power consumption
    - No NVM
    - Digital libraries and memory compilers available
  - DARE180X in XFAB XH018 0.18um BCD technology
    - > 100kRad => lower power
    - High-voltage BCD
    - Non-volatile memory
    - Digital libraries available
  - I3t80 On semiconductor 0.35um BCD
    - 80V devices available
    - No digital library

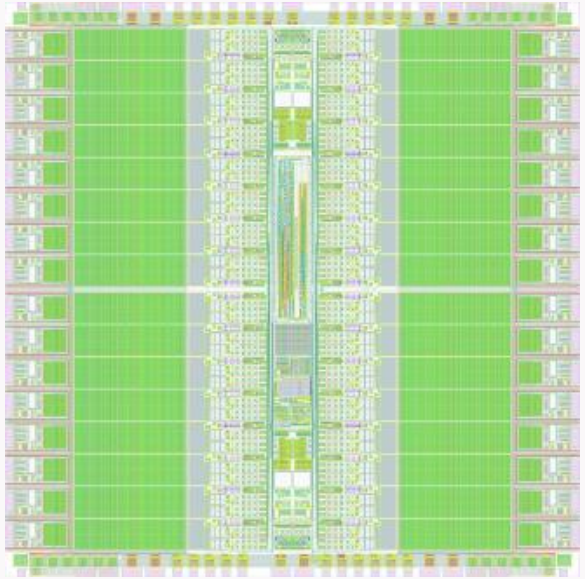
IP in imec DARE solution

- ICsense analog, mixed-signal and high-voltage IP in DARE180U and DARE180X
- All IP blocks developed for the DPC of Thales Alenia Space Belgium (ETCA)
  - 13 bit, 1MSps ADCs
  - 120MHz PLL with ultra-low SET sensitivity (no glitches)
  - 12 bit, 3.75MHz DACs
  - Voltage and current references with embedded temperature sensor
  - 100kHz accurate RC oscillator
  - 3.3V – 1.8V linear regulators for analog and digital supplies
  - Inductive DCDC converters for secondary supply conversion to 3.3V and 1.8V (DARE180X only)
  - Drivers up to 18V (DARE180X only)
  - Other auxiliaries (comparators, buffers, filters, PGAs, levelshifters, ….)



IP in imec DARE solution

- Analog, mixed-signal and high-voltage IP in i3t80 ON Semiconductor
  - ADK has been developed by imec
  - Allows for high-voltage ASIC developments in Cadence design flow
  - Contains:
    - ELT pcells for nmos and pmos
    - ELT for NDMOS
    - Octogonal devices for IO cells
    - Calibre decks have been updated for
      - ELT integration
      - Guard rings
      - N-to-n type leakage
  - Used to developed a high-voltage, rad-hard ASIC with max. voltage of 40V and several amps
  - SEGR and SEB minimization

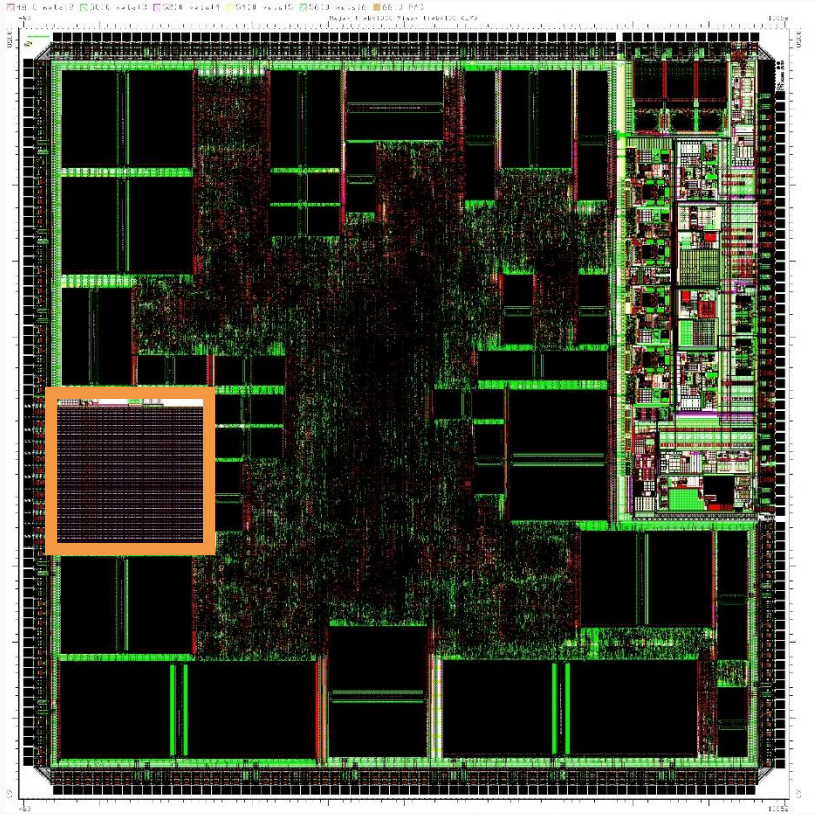


Availability of IPs in (X)DARE180

- Supported ICsense analog, mixed-signal and high-voltage IP in DARE180U and DARE180X
  - 13 bit, 1MSps ADC
  - 120MHz PLL with ultra-low SET sensitivity (no glitches)
  - 12 bit, 3.75MHz DAC
  - Voltage and current references with embedded temperature sensor
  - 3.3V – 1.8V linear regulators for analog and digital supplies
- IP in DARE180U is **silicon and radiation proven**!
- IP in DARE180X is under development
- Product briefs available
- Deliverables: datasheets, VerilogAMS model, integration guidelines, encrypted Spectre netlist

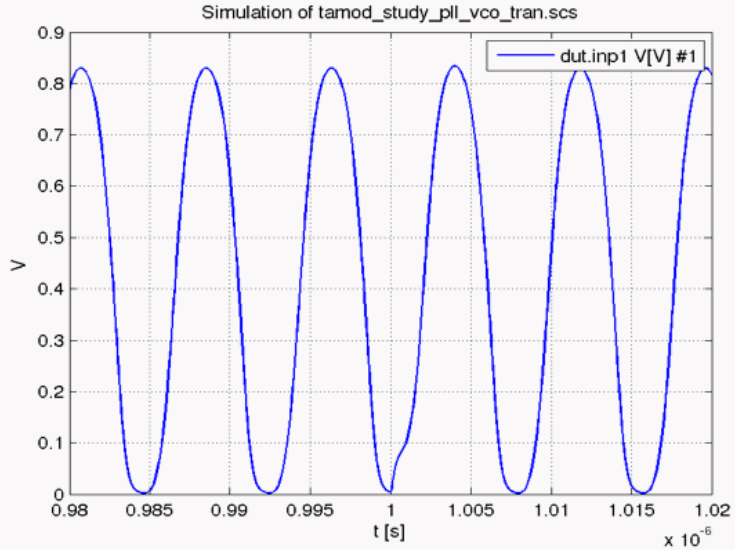
Linear regulators

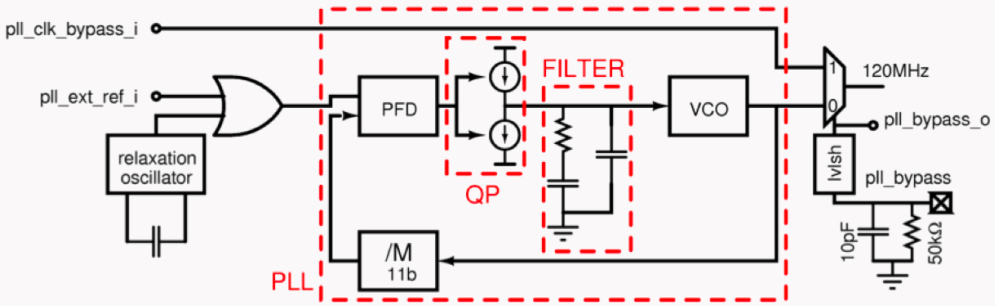
- Digital supply
  - 3.3V to 1.8V
  - Current up to 700mA
  - Area 4.7mm^2 against thermal degradation
- Analog supply
  - 3.3V to 1.9V
  - Current up to 30mA
- Package changes or current changes require simulations/redesign



PLL

- Long-term frequency spikes and phase shifts due to SET are minimized
  - Simulation example with ICsense proprietary SET flow
  - 60MeV cm2/mg strike at 1us
- Input: 100kHz accurate oscillator or Xtal
- Tailoring of frequency possible

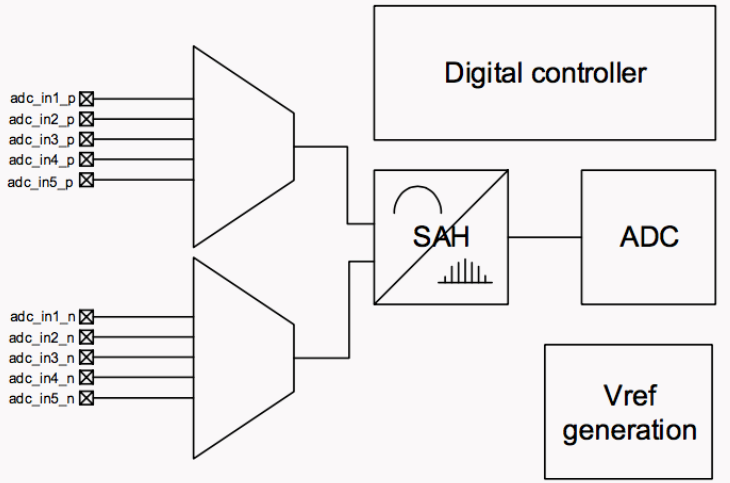




Spec	Unit	Min	Typ	Max	Comment
Area	mm^2	-	2.3	-	
Supply PLL	V	1.8	1.9	1.98	
PLL current consumption	mA	-	-	13.8	
PLL frequency range when locked	MHz	-0.5%	120	+0.5%	Aging and TID effects not included
PLL frequency range during SET when locked	MHz	-3%	120	+3%	Deviation immediately after SET event
Cycle to cycle jitter	fs	-	-	400	
Spurious free dynamic range	dB	100	-	-	

13 bit, 1MSps ADC

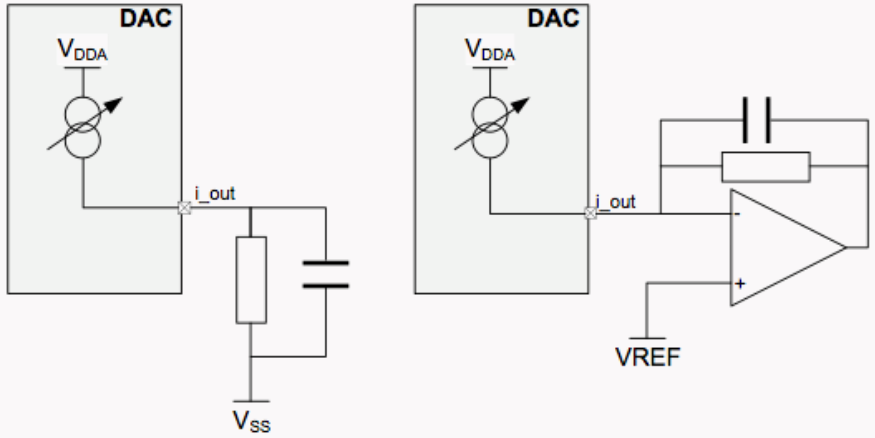
- Cyclic topology with input S&H
  - Integrated reference buffer
  - No external components
  - Requires the voltage reference from ICsense
- SET behavior
  - ADC controller cannot enter a locked state
  - Max 3 ADC samples are affected by an SET strike
  - Multiplexers are hardened



Spec	Unit	Min	Typ	Max	Comment
Area	mm^2	-	0.425	-	
Current consumption ADC	mA	-	-	6.0	
Resolution	bits	-	13	-	
LSB	mV	-	0.330	-	At the input of S/H
Sample rate	MS/s	-	-	1	
INL (differential) / (single ended)	LSB	-	-	4.0 / 6.2	
DNL	LSB	-	-	1.5	
SNDR (differential) / (single ended)	dB	-	73 / 67.5	-	100kHz

DAC

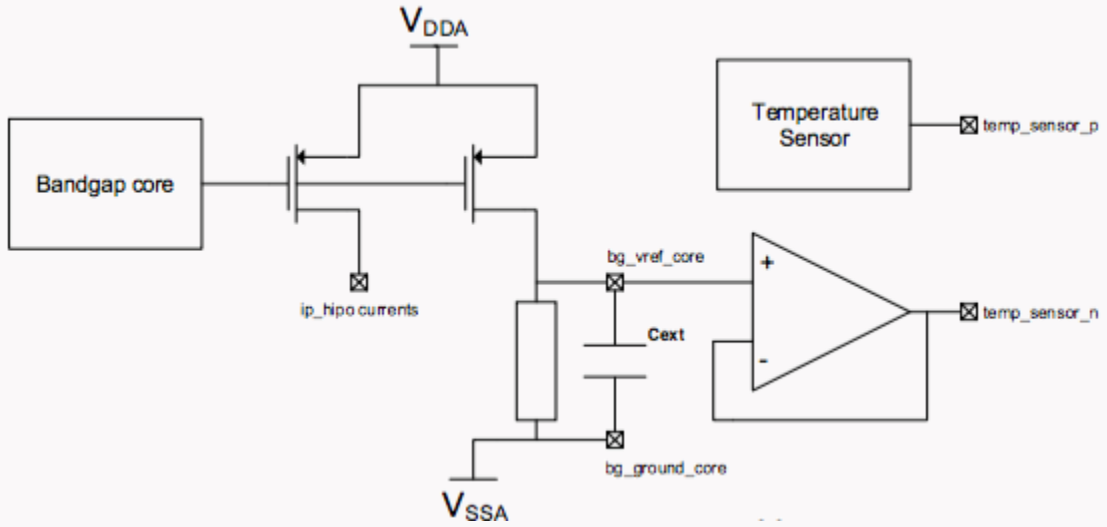
- P-type current-steered 12-bit DAC
  - With DEM: 58.6kHz data rate
  - Without DEM: 3.75 MHz data rate



Spec	Unit	Min	Typ	Max	Comment
Area	mm^2	-	0.39	-	
Current consumption	mA	-	4.2	4.5	
Resolution	bit	-	12	-	
LSB	uA	0.93	0.98	1.03	
Full scale	mA	3.8	4	4.2	P-type current
Output range	V	0	-	2.5	Compliance voltage of 0.5V
Data rate no DEM/DEM	MS/s	-	3.75 / 0.058	-	
DNL no DEM/DEM	LSB	-	-	2 / 0.75	
INL no DEM/DEM	LSB	-	1.5 / 1.06	1.7 / 1.26	Output buffer @ output

Voltage and current reference

- Bandgap voltage of 1V
  - Reference distribution with current possible
- Bias block of 47 output currents of 10uA
- Temperature sensor embedded
- SET behavior
  - SET cannot trigger unwanted shutdown/start
  - Only minor glitches on BG voltage



Spec	Unit	Min	Typ	Max	Comment
Area	mm^2	-	1.67	-	
Current consumption	mA	1.65	2.0	2.55	
Nominal reference voltage (Vbg)	V	0.9874	1.0075	1.0277	
Vbg Integrated noise 1Hz – 1 GHz	μV_{RMS}	15.840	19.250	23.792	
Vbg min. PSRR 1Hz - 120MHz	dB	34	-	-	PSRR @DC >60dB
Vbg temperature drift -20-110°C	ppm	-887	-	984	After 2nd order digital compensation
Error of temperature sensor in temperature range -20-110°C	°C	-0.81	-	1.01	After digital compensation.

High-voltage power management in DARE180X

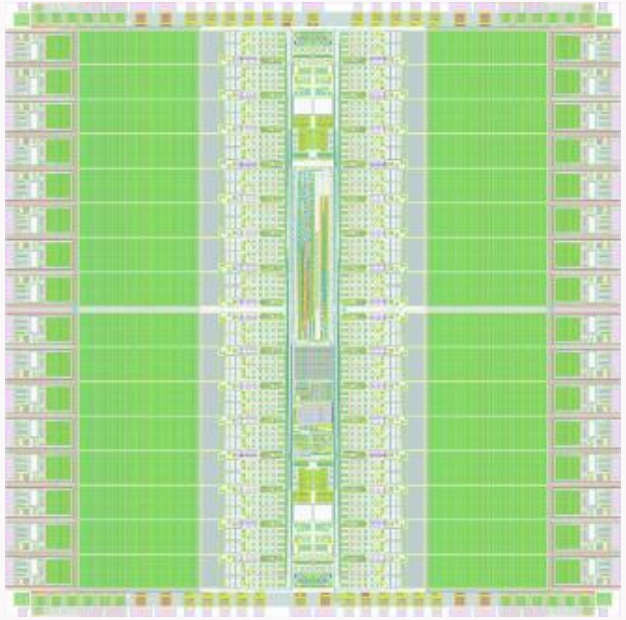
- Input voltages from 4 to 16.5 V
  - XFAB XH018 45V devices used to minimize SEGR
- Different blocks:
  - High-voltage regulator: 4-16.5V to 3.3V for low power blocks (max 3.5mA)
  - Shunt regulator for intermediate voltages
  - Hysteretic 1.8V inductive buck DCDC converter: 3-16.5V to 1.8V
    - maximum load current of 600 mA
    - efficiency of 70-86% for different load conditions
  - Hysteretic 3.3V inductive buck DCDC converter: 4V-16.5V to 3.3V
    - maximum load current of 350mA
    - efficiency of 86-94% for different load conditions
  - High-voltage driver up to 125mA and 16.5V

High-voltage power management in DARE180X

- Radiation hardness using ICsense proprietary rad hard simulation methodology
  - Effect of SET on output voltage is only +- 0.2%
  - Digital controller: rad hard cells only for static signals
  - For bias nodes of critical blocks (gm cells):
    - Filtering techniques
    - Higher currents in bias currents
      - Fast startup
      - Lower voltage peaks
  - Current sense: LPF for deglitching the output
  - Deglitched and hardened Schmitt triggers at the output
  - Soft start is hardened to limit startup currents

Rad Hard high-voltage in i3t80

- Driver ASIC to drive up to 40V and several amps of current
- Features:
  - Very low-ohmic high-voltage switches
    - VGS < 3.3V. Floating switches
  - 4KV HBM ESD (high- and low-voltage)
  - Minimal number of external components
  - Maximal integration: bandgap refs, amplifiers, POR, regulator, reference buffers, level shifters, test
- Rad hard measures:
  - SEGR minimization: stacked NDMOS
  - Bandgap, POR and levelshifters: SET proof through filtering techniques
- Measurements ongoing



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Conclusions

- Blocks available and can be purchased through imec:
  - 13 bit, 1MSps ADC
  - 120MHz PLL with ultra-low SET sensitivity (no glitches)
  - 12 bit, 3.75MHz DAC
  - Voltage and current references with embedded temperature sensor
  - 3.3V – 1.8V linear regulators for analog and digital supplies (not standalone)
- UMC 0.18 IP: silicon and radiation proven
- XFAB XH018 IP: under development
- I3t80 high-voltage ASIC: proven in silicon
- Radiation hard design through the proprietary ICsense under-radiation simulation flow

Acknowledgements

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SET simulations flow at ICsense

- Inject double exponential current with total charge depend on LET
- Flow procedure for building block SET simulations
  - Typical conditions: inject in every node to produce short list of sensitive nodes
  - SET simulations for all sensitive nodes over PVT.
  - Adapt design if needed
- Re-inject all nodes in worst-case corners
- Clock signals: vary also injection time relative to clock period
- Top level: check e.g. if SET on bandgap does not influence PLL
- Fully automated flow integrated into our MATLAB driven design environment