RADIATION HARDENED HIGH-VOLTAGE AND MIXED-SIGNAL IP WITH DARE TECHNOLOGY

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Abstract

Recent trends show the growing need for more analog, mixed-signal and high-voltage IP to enhance the intelligence and reduce the cost of satellites. This paper presents the set of radiation hard, mixed-signal and high-voltage IP that is part of the imec DARE solution and that is developed in UMC 0.18um, XFAB XH018 and On Semiconductor i3t80 technology. The IP is conceived to enable rad-hard SoC developments and consists of ADCs, PLLs, clocks, linear regulators, bandgap references with current reference and temperature sensors, high-voltage DCDC converters to convert the satellite main supply to analog and digital on-chip voltages and several high-power and high-voltage switches and drivers. The IP is versatile to be useful in a myriad of applications and is part of the DARE platform.

The IP in UMC 0.18um has been successfully silicon proven and radiation tested. First-time-right radiation hardness is achieved through a proprietary under-radiation simulation approach developed by ICsense and elaborated in this paper.

I. INTRODUCTION

Harsh radiation environments constitute an essential challenge for space applications. Pervasive particles from cosmic rays induce cumulative and transient effects that can cause soft errors or even permanent damage in electronics circuits. Mixed-signal integrated circuits implemented in deep submicron commercial technologies have already been qualified as a cost efficient solution for satellites and radiation applications [1]. Besides the low cost, these thin gate oxide technologies are inherently hardened against total ionizing dose (TID) and offer high speed, low power consumption and high yield.

Although commercial libraries and mixed-signal IP are available, they often present high single-event latch-up (SEL) and single-event transients (SET) sensitivity when used in mixed-signal ICs. On the other hand, radiation hardened mixed-signal IP and digital libraries are designed using special design and layout techniques to cope with such issues and still provide high density and low power consumption. These libraries can be used in traditional standard cell design flows.

The existing DARE180 library solution, implemented in UMC 0.18 µm technology, and including mixed-signal IPs such as ADC, PLL, DAC, linear regulators, clocks and current/voltage references with embedded temperature sensor, has already been validated in several space applications [2-4]. The mixed-signal IP in UMC 0.18um has been successfully silicon proven and radiation tested. This solution was designed to be useable in a broad range of systems and therefore offers a very high TID tolerance at the cost of higher power consumption and lower gate density than commercial libraries.

The DARE180X library platform is currently under development with a test chip being taped-out. It includes similar IP blocks, but also DCDC converters to convert the satellite secondary power supply to usable voltages for digital and mixed-signal ASIC use (3.3V and 1.8V). The library platform provides a solution tailored for space applications that require TID tolerance of at least 100 kRad while keeping power consumption and gate density closer to the commercial libraries and enabling high-voltages up to 18V in mixed-signal SoC developments for power management and drivers. Similarly to its UMC-based counterpart, DARE180X includes blocks specially designed to mitigate various single event effects (SEE). More information on the digital DARE180X library and a comparison with the DARE180 library can be found in [5].

Last but not least, the DARE solution has been extended with a ADK for On Semiconductor i3t80, which is a 0.35um BCD process with high-voltage devices up to 80V. It is created to allow radiation hardened, DARE methodology compatible, high-voltage ASIC developments in a standard Cadence design flow as is available for UMC and XFAB technologies. The commercially available PDK has been extended with ELT (Enclosed Layout Transistor) pcells for both nmos and pmos low-voltage devices and for NDMOS high-voltage devices and with octagonal devices for IO cells. The default physical verification decks (Mentor Calibre) have been updated for integration of the ELT pcells, guard rings and n-to-n type leakage. This ADK has been used to develop a high-voltage, radiation-hardened ASIC in i3t80 with maximal voltages up to 40V and currents of several amperes. Care has been taken to minimize SEGR and SEB.

II. RADIATION HARDENED MIXED-SIGNAL IP

All mixed-signal IP blocks - available in both the DARE180 in UMC 0.18um CMOS and the DARE180X in XFAB XH018 - have been developed in the framework of the digital programmable controller (DPC) of Thales Alenia Space [4]. Since the DPC is a highly versatile radiation hardened SOC for a myriad of applications in satellites, it comprises all important mixed-signal blocks needed to build a SoC:

- Reference voltage and current generation
- Built-in temperature sensor
- Power-management block with linear regulators for analog and digital power supply generation
- SET insensitive 120 MHz frequency reference system (PLL) to provide the clock to the digital part
- 100kHz reference oscillator
- 4 flexible 13 bit , 1MSps ADCs with extensive input muxing capabilities
- 3 12 bit, 3.75 MSps DAC current-mode outputs
- Power-on-reset circuit and under voltage detector
- Rail to rail comparators, PGA (0dB, 10dB, 20dB), level shifters, buffers, …

This paper only focuses on the test results of the analog blocks that are readily available in the DARE solution, being the PLL, ADC, bandgap with temperature sensor, DAC and linear regulators. Radiation test data is available and shows all blocks performing as specified under radiation. This excellent result can be attributed to the ICsense proprietary, automated SET hardening simulation environment to assess and decrease the SET sensitivity of the mixed-signal IP [3].

A. Linear regulators

Two linear regulators have been developed, both needing an external compensation capacitor.

For digital supply: Converts the 3.3V main supply to 1.8V with a current capability of 700mA. The area is 4.7mm2 which is needed to avoid temperature degradation. For analog supply: converts the 3.3V main supply to 1.9V with a current capability of 30mA.

Changing the package or the current capability of any of the regulators requires new simulations and possibly a redesign..

B. PLL

For a reliable operation of the digital part, it is essential the clock generation is without glitches (stable clock period and duty-cycle), even during SET events. 'Long-term' frequency spikes and phase shifts due to SET are minimized. The complete PLL, including divider, loop filter and VCO is integrated on-chip. The measured output frequency of the PLL is 120MHz and the bandwidth 7kHz. The input frequency to the PLL is a 100kHz input source selectable between an off-chip reference oscillator or an integrated relaxation oscillator.

The integrated 120MHz Voltage Controlled Oscillator (VCO) has been designed to ensure SET free operation. The VCO is less sensitive to power supply disturbances and provides lower jitter compared to a plain ring oscillator.

The measured specifications are shown in Table 1. All specifications have been validated under radiation and glitch free operation has been proven.

Spec	***Unit***	***Min***	***Typ***	***Max***
Area	mm^2	-	2.3	-
Supply PLL	V	1.8	1.9	1.98
PLL current consumption	mA	-	-	13.8
PLL frequency range when locked	MHz	-0.5%	120	+0.5%
PLL frequency range during SET when locked	MHz	-3%	120	+3%
Cycle to cycle jitter	Fs	-	-	400
Spurious free dynamic range	dB	100	-	-

Table 1: Measured specifications of the integrated PLL

C. ADC

The Analog-to-Digital converter has a cyclic topology with a sample-and-hold structure at the input. The block can operate both differentially and single-ended. It has an integrated reference buffer and requires no external components. The ADC requires a 120MHz clock signal that is internally divided to 30MHz to control the ADC. The block offers full flexibility over the timing of the mux and sample-and-hold. A sampling signal marks the start of the sampling operation of the sample-and-hold, while a start-of-conversion signal marks the end of the sampling operation and triggers the conversion of the sampled signal by the ADC. A block diagram is given in Figure 1. The behavior under SET is as follows:

- The ADC controllers are sensitive to SET, but they cannot enter a locked state.
- The analog part are sized such that an SET strike can only influence 3 ADC samples.
- The multiplexers are hardened for SET strikes to ensure that the analog inputs are never shorted.

The sample-and-hold/mux circuit operates with a 2.5Vptp differential input signal at a common-mode of typically 1.25V. The measured specification can be found in Table 2.

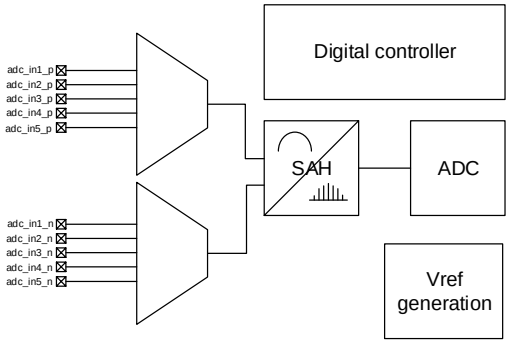

Figure 1: Block diagram of the ADC

Spec	*Unit*	*Min*	*Typ*	*Max*
Area	mm^2	-	0.42	-
Current consumption ADC	mA	-	-	6.0
Resolution	bits	-	13	-
LSB	mV	-	0.33	-
Sample rate	MS/s	-	-	1
INL (diff) / (se)	LSB	-	-	4.0 / 6.2
DNL	LSB	-	-	1.5
SNDR (differential) / (single ended)	dB	-	73 / 67.5	-
RMS noise	LSB	-	0.6	0.75

Table 2: Measured specifications of the ADC

D. DAC

The Digital-to-Analog Converter is a p-type current-steered 12-bit resolution DAC that can operate with/without Dynamic Element Matching (DEM). The DAC-current can be converted to a voltage with a resistor to ground or it can be fed into a buffer. The latter use case has superior linearity. The DAC supports two operation modes.

- Without DEM: Data can change at 3.75MHz data rate. An external filter at 1MHz should be employed.
- With DEM mode: Data can change at divisions of 58.6kHz (3.75MHz/64) data rate. Other data rates will show drop in performance. A first order filtering at 58.6kHz must be employed to suppress switching artefacts of the DEM.

Spec	*Unit*	*Min*	*Typ*	*Max*
Area	mm^2	-	0.39	-
Current consumption	mA	-	4.2	4.5
Resolution	bit	-	12	-
LSB	uA	0.93	0.98	1.03
Full scale	mA	3.8	4	4.2
Output range	V	0	-	2.5
Data rate no DEM/DEM	MS/s	-	3.75 / 0.058	-
DNL no DEM/DEM	LSB	-	-	2 / 0.75
INL no DEM/DEM	LSB	-	1.5 / 1.06	1.7 / 1.26

Table 3: The measured specifications of the DAC

E. Voltage and current reference with built-in temperature sensor

The voltage and current reference block provides an accurate radiation hard reference voltage and currents. It consists of a bandgap, bandgap buffer, current bias block and temperature sensor:

- The bandgap provides a high-impedance, unbuffered bandgap voltage of 1V. It requires an external decoupling cap of 4.7nF. The reference currents can be used to generate accurate voltages in other blocks by using matched unit resistances.
- The bias block uses an external resistor to generate accurate bias currents. It has 47 current outputs of 10uA and an additional source to be used together with the reference oscillator IP block.
- The temperature sensor, including output buffers, provides a PTAT (Proportional To Absolute Temperature) voltage and is compatible with the ADC IP block, so enabling digital temperature read-out.

The behavior under SET is as follows:

- SET cannot trigger an unwanted shutdown/restart sequence of the bandgap.
- SET can only generate minor disturbance on bandgap voltage (few mV) and on the currents.
- Temperature sensor and buffer outputs are not SET hardened.

Spec	*Unit*	*Min*	*Typ*	*Max*
Area	mm^2	-	1.67	-
Current consumption	mA	1.65	2.0	2.55
Nominal reference volt (Vbg)	V	0.987	1.0075	1.028
Integrated noise 1Hz – 1 GHz	μV_{RMS}	15.840	19.250	23.792
min. PSRR 1Hz - 120MHz	dB	34	-	-
Temp drift -20-110°C	ppm	-887	-	984
Error of temperature sensor in -20-110°C	°C	-0.81	-	1.01

Table 4: Measured specifications of the references

III. HIGH-VOLTAGE POWER MANAGEMENT IP IN XFAB XH018

As part of the DARE180X library, high-voltage power management blocks are developed and included in the test chip that is being processed. These blocks have been developed to handle input voltages between 4 and 16.5V. The XFAB XH018 high-voltage devices (45V) have been used in these blocks to have sufficient margin to avoid Single-Event-Gate-Rupture (SEGR). A previous test chip has been tested under radiation to assess the performance and robustness of these high-voltage devices.

The different high-voltage blocks that have been developed are:

- High-voltage regulator: converts the 4-16.5V to 3.3V for low power blocks (max 3.5mA) that have to start up fast;
- Shunt regulator that generates intermediate voltages for the DCDC converters;
- Hysteretic 1.8V DCDC converter that converts a 3V-16.5V input to a 1.8Voutput with a maximum load current of 600 mA and a maximum voltage ripple of 130mVptp; the efficiency is 70-86% for different load conditions;
- Hysteretic 3.3V DCDC converter that converts a 4V-16.5V input to a 3.3V output with a maximum load current of 350mA and a voltage ripple of 130mVptp; the efficiency is 86-94% for different load conditions;
- High-voltage driver that can drive up to 125mA with an output voltage of 16.5V.

Both DCDC converters use an external inductor and several external capacitors for their operation. The DCDC converts consists of a voltage loop with built-in soft start, with hysteresis that is controlled externally, type II compensation and a current loop that measures the coil current trough an external resistor. A SET hardened comparator compares the measured current to the wanted current in the voltage loop. The coil driver drives the coil controlled by the comparator. When the DCDC is disabled, the coil-driver is put into tri-state. The output supply is in this case pulled to ground. The DCDC is able to withstand a short at its output pin.

In Table 5, the total output variation is given for different parameters with and without trimming.

Parameter	**Unit**	**Variation**	
		Min.	**Max.**
SET event	%	-0.17	0.20
Load step drop	%	-7.87	6.35
Total	%	-2.97	2.57
Total, batch trimming	%	-1.65	1.34
Total, sample trimming	%	-1.01	0.7

Table 5: Output variation on the 1.8V DCDC converter

Several measures haven been taken to maximize the radiation hardness of the DCDC converter using the proprietary rad hard simulation methodology of ICsense [3]. As can be seen in Table 5, the effect of an SET is only +-0.2% due to these measures. For the digital controllers, rad hard cells are only used for controlling static signals to reduce spikes on the analog supply. For all critical bias nodes of the critical blocks (integrator gm cell, current sense gm cells), filtering techniques and higher currents have been used in bias branches to have faster settling and smaller voltage peaks. In the current sense block, low pass filters of 160 kHz have been added to the outputs of the comparators to deglitch the output, followed by a deglitched and hardened Schmitt trigger.

The soft start slope node has a high impedance, and is thus susceptible to SET strikes. It has been designed to limit the maximal current delta due to a SET event during startup to ±50 mA by choosing the right capacitor value. The soft start ensures that the current sensing has already started up before any current starts flowing in the coil.

IV. High-Voltage IP Development in i3t80

Using the radiation hardening ADK (Analog Design Kit) for the On Semiconductor i3t80 technology in de DARE solution of imec, a high-voltage, radiation-hardened ASIC in i3t80 has been developed.

The ASIC is a driver ASIC able to drive voltages up to 40V and currents up to several amperes in total. To limit the voltage drop and power dissipation very low-ohmic, high-voltage switches have to be used. To drive these switches a floating voltage domain for each high-voltage input is created, since the gate-source voltage of the high-voltage devices can be maximally 3.6V. Given the size of the DMOS devices care has to be taken of radiation effects, especially SEGR. In addition, the high-voltage power supply is protected with a 4kV HBM ESD clamp. The outputs are self-protecting up to 4kV. All low voltage pads are protected up to 4kV as well.

The ASIC only needs a minimal number of external component. All other blocks are integrated such as bandgap references, amplifiers, POR, regulators, level shifters, reference buffers, test infrastructure ... The layout is shown in Figure 2.

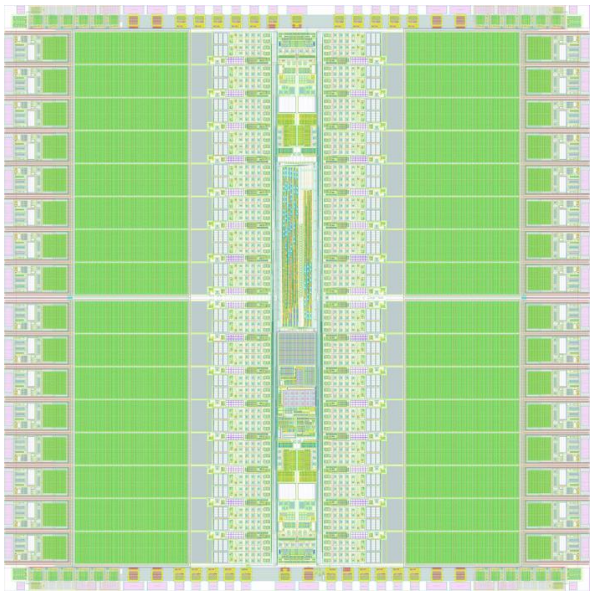

Figure 2: i3t80 ASIC layout

Several measures are taken to attain radiation hardness for a TID up to 100kRad and 60 MeV/mg/cm^3 LET. For TID effect minimization, ELT devices are used for both nmos and pmos devices and NDMOS devices. To prevent SEGR and SEB, DNMOS devices are stacked. Safe operating checks have been implemented to monitor the VDS of all high-voltage devices during simulation. To prevent SET effects, the proprietary SET simulation flow has been used to assess and minimize the impact of an SET pulse. The bandgap, level shifters and POR have been made SET proof through filters and increased currents to avoid state changes due to SET events.

The measurements of the ASIC are ongoing and show excellent results at the moment of writing this paper.

V. Conclusions

Thanks to the successful collaboration with its partners and customers, ICsense has been able to develop a set of radiation hard, mixed-signal and high-voltage IP blocks. The IP is commercially available as part of the imec DARE solution in UMC 0.18um, XFAB XH018 and On Semiconductor i3t80 technology. The IP enables rad-hard SoC developments and consists of ADCs, PLLs, DACs, linear regulators, bandgap references with current reference and temperature sensors, high-voltage DCDC converters to convert the satellite main supply to analog and digital on-chip voltages and several high-power and high-voltage switches and drivers.

The IP blocks in XFAB XH018 are being processed. The IP in UMC 0.18um has been successfully silicon proven and radiation tested. The high-voltage ASIC in i3t80 has been successfully proven in silicon and radiation testing is ongoing. First-time-right radiation hardness is achieved through a proprietary under-radiation simulation approach developed by ICsense.

VI. ACKNOWLEDGEMENTS

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