ESA Cosmic Vision MF ASICs and IPs Development

E. Pun[a] , F. Serra-Graells[b], J. Madrenas[c], M. García[d], R. Jansen[e], F. Muñoz[f], D. González[a], Michele Dei[b], L. Entrena[d], D. Fernández[c]

[a]ARQUIMEA Ingeniería S.L.U, Madrid, Spain
[b]Instituto de Microelectrónica de Barcelona (IMB-CSIC), Barcelona, Spain
[c]Universitat Politècnica de Catalunya (UPC), Barcelona, Spain
[d]Universidad Carlos III de Madrid (UC3M), Madrid, Spain
[e]ESA, 2200 AG Noordwijk, The Netherlands
[f]Universidad de Sevilla, Seville, Spain

epun@arquimea.com

paco.serra@imb-cnm.csic.es

jordi.madrenas@upc.edu

mgvalder@ing.uc3m.es

richard.jansen@esa.int

fmunoz@gte.esi.us.es

dgonzalez@arquimea.com

michele.dei@imb-cnm.csic.es

entrena@ing.uc3m.es

dfernan@eel.upc.edu

Abstract

In the radiation environment envisaged for the interplanetary mission to Jupiter named Juice, the electronic equipment will require to withstand up to 300krad of Total Ionization Dose. The availability of high performance components that can cope with that requirement is low or non-existent and for that reason ESA funded an activity to create radiation tolerant high-performance mixed-signal IPs.

In the frame of the project two different ASICs where implemented: A rad-hard programmable ∑Δ modulator (CVB-001) which contains four separate ∑Δ modulator and a Rad-hard analogue front-end chip (CVC-001) which contains a Bessel Filter, a Digital to Analogue Converter, a Low Noise Amplifier and a Power amplifier.

Simulation and validation results of those chips and in particular the detailed behaviour of each of the IPs will be presented.

I. Introduction

A set of rad-hard IPs were implemented to provide system designers with the tools needed to build an analogue front-end (from the acquisition of the sensor signal to the data digitalization) for the instruments to be used in Juice missions (i.e. CCD signal conditioner, radiation detector, radiation spectrometer, etc.). These IPs were distributed in two ASICs: CVB001 and CVC001. The former is a rad-hard analogue-to-digital converter (ADC) composed by four ΣΔ modulators (ΣΔM), each of them optimized for a frequency range. The latter includes a filter, a digital-to-analogue converter (DAC), and two kinds of amplifiers: low-noise and power amplifiers. All the IPs were designed to be compatible for interconnection, in order that the signal integrity is maintained all over the possible block chains. Furthermore, all the IPs are configurable, in order to maximize the signal-to-noise and distortion ratio and reduce the power consumption of the overall system. The communications interface to control the ASICs at system level is SPI. Internally, APB protocol is used to read and write the configuration registers.

The considered signal bandwidth is [0.05; 5] MHz and the target resolution is 18 effective bits for the lower frequency limit down to 13 effective bits for the highest.

The IPs design was distributed among a consortium of research groups leaded by a private company:

- ARQUIMEA Engineering (ARQ): in charge of the the coordination, the design of the general purpose IPs, CVB001 and CVC001 system design, system integration, system verification and system validation.
- Microelectronics Institute of Barcelona CSIC (IMB-CSIC): in charge of the mixed signal IPs design.

- Carlos III University of Madrid (UC3M): in charge of the digital design.
- Polytechnic University of Catalonia (UPC): in charge of the amplifiers IPs design.
- University of Seville (USE): in charge of the filter IP design.

CVB001 and CVC001 ASIC were implemented using DARE180 mixed signal library based on UMC180 technology.

A. List of IPs

As mentioned before, the IPs were implemented in two separate ASICS: CVB001 and CVC001. Nevertheless some additional IPs (needed for the basic operation, communication and configuration of the ASICs) were also implemented.

General purpose IPs included in both ASICs are:

- 3.3/1.8V power supply regulator for analogue circuitry (REGA) (designed by ARQ)
- 3.3/1.8V power supply regulator for digital circuitry (REGD) (designed by ARQ)
- SPI/APB communication blocks (SPI) (designed by UC3M)
- High accuracy bandgap voltage reference (BGR) (designed by ARQ)
- Analogue test bus (ATBUS) (designed by ARQ) with 16 channels.
- Digital test bus (DTBUS) (designed by ARQ) with 16 channels.

The Main IPs included in CVB001 are listed below:

- Low-speed single-bit (LSSB) ΣΔ modulator (designed by IMB-CSIC), designed for the [50; 150] kHz signal frequency range.
- High-speed single-bit (HSSB) ΣΔ modulator (designed by IMB-CSIC) designed for the [150; 500] kHz signal frequency range.
- Low-speed multi-bit (LSMB) ΣΔ modulator (designed by IMB-CSIC), designed for the [0.5; 2] MHz signal frequency range.
- High-speed multi-bit (HSMB) ΣΔ modulator (designed by IMB-CSIC), designed for the [2; 5] MHz frequency range.

The Main IPs included in CVC001 are listed below:

- Bessel filter (BF) (designed by USE) with configurable bandwidth (1 and 5 MHz options)
- Low-speed DAC (LSDAC) (designed by IMB)
- Low-noise amplifier (LNA) (designed by UPC) with voltage and trans-impedance programmable amplification modes.
- Power amplifier (PA) (designed by UPC) with voltage, current, trans-impedance and trans-conductance amplification modes.

This paper will be focused on the verification and electrical validation results of three of the developed IPs and in a few configuration modes, for concision. These are: LSSB ΣΔM, LNA (voltage gain) and PA (voltage gain). It shall be noted that radiation testing was not foreseen in the frame of this project.

B. Main specifications

The requirements specification of the IPs was very ambitious and sometimes even above the state of the art, targeting then high performance blocks. The general requirements of the IPs are collected in Tables 1 to 3. Requirements for the ΣΔM modulators, LNA and PA are collected in tables 4 to 6 respectively.

Table 1: Temperature specifications

Parameter	Value	Unit
Operational range	[-10; 85]	°C
Functional range	[-55; 125]	°C

Table 2: Radiation specifications

Parameter	Value	Unit
TID	300	Krad
SEL	80	MeV·cm2/mg
SER	1e-10	errors/bit/day

Table 3: Supply specifications

Parameter	Value	Unit
Supply voltage	[2; 3.6]	V
Supply current	<27	mA

Table 4: ADC main specifications

Parameter	Value	Unit
Signal bandwidth	[0,05; 5]	MHz
Effective resolution	[13; 19]	bits
Consumption	[1; 20]	mA

Table 5: LNA main specifications

Parameter	Value	Unit
Signal bandwidth	[0,05; 5]	MHz
Analogue inputs	[0; 4] / [-0.7; 0.7]	V / mA
THD	[80; 114]	dB
Consumption	4	mA

Table 6: PA main specifications

Parameter	Value	Unit
Signal bandwidth	[0,05; 5]	MHz
Analogue outputs	[0; 4] / [0; 80]	V / mA
Consumption	45	mA

II. ASICs Architecture

A. CVB001 block diagram

The simplified block diagram of the CVB001 ASIC is depicted in figure 1.

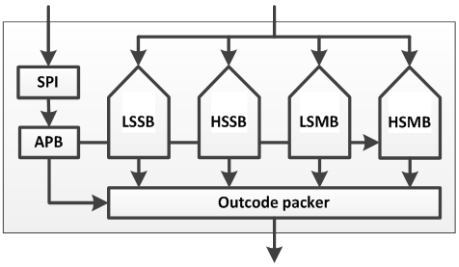

Figure 1: CVB001 block diagram

CVB001 ASIC is composed by four ΣΔ modulators: LSSB, HSSB, LSMB and HSMB. Each one is designed to operate in a non-overlapped signal frequency range: LSSB for [50; 150] kHz, HSSB for [150; 500] kHz, LSMB for [0.5; 2] MHz and HSMB for [2; 5] MHz. Modulators for the two lowest frequency ranges have single-bit output whereas modulators for the highest frequency ranges have a 5-bit multi-bit output. Only one modulator can operate at a time since the output interface is shared and to reduce power consumption. A digital circuitry called 'out-code packer' packages 20 consecutive conversions for the single-bit modulators or 4 consecutive conversions for the multi-bit modulators, in a 20-bit out-code to reduce the frequency of the digital output. CVB001 is controlled and configured through SPI. A 16-channel analogue test bus allows the monitoring of internal critical nets as the output of the regulators and the bandgap reference.

B. CVC001 block diagram

The simplified block diagram of CVC001 ASIC is depicted in figure 2.

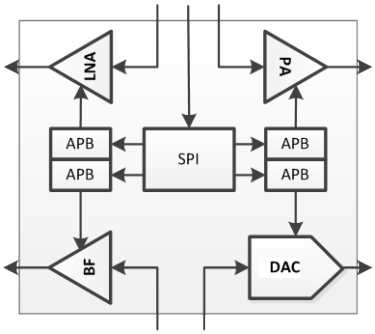

Figure 2: CVC001 block diagram

CVC001 is composed by a Bessel filter a digital-to-analogue converter, a low-noise programmable amplifier and a power amplifier. All the blocks can operate independently and powered-down if their use is not required. CVC001 is controlled and configured through SPI. A 16-channel analogue test bus allows the monitoring of internal critical nets as the output of the regulators and the bandgap reference. Two 16-channel digital test buses allow the monitoring and comparison of internal digital signals to trim clock signals delays and frequencies.

III. RADIATION HARDENING TECHNIQUES

As commented before, the technology used for the development of these IPs is DARE/UMC180 Mix-mode. The DARE digital library was used to implement the digital configuration logic and the modulator output data packers. This library can handle perfectly the project radiation requirements as stated in [1] and [2].

For the analogue part and a few full custom digital cells directly placed on the ΣΔMs dedicated radiation hardening techniques were followed as the ones detailed in [3]

IV. VERIFICATION

Together with the power consumption, a single key parameter has been selected to represent the performance of each IP for convenience. In the case of the LSSB ΣΔM, the effective resolution calculated from the signal-to-noise and distortion ration (SINAD) has been selected. In the case of the amplifiers, their performances is dominated by distortion over noise, hence the total harmonic distortion was the selected parameter. Tables 7 to 9 collect the comparison between the core and the chip simulated performances for the LSSB ΣΔM, LNA and PA respectively.

Table 7: LSSB ΣΔM verification results

Parameter	Core	Chip	Unit
Effective resolution	18	15.5	bits
Consumption	11	15	mA

Table 8: LNA verification results

Parameter	Core	Chip	Unit
THD	88	80	dB
Consumption	24	25	mA

Table 9: PA verification results

Parameter	Core	Chip	Unit
THD	74	68	dB
Consumption	100	110	mA

Degradation in performances is observed at chip level mainly due to the parasitic effects of the pads and package. It shall be noted that in the frame of the activity standard off the shelf packages were envisaged.

V. VALIDATION

A. Tested silicon and packaging

The CVB and CVC chips were fabricated under the IMEC-Europractice service using a MPW run. The die area of both devices is 5x5 mm^2

In addition to these two dies an additional one fabricated under the same service in a mini-ASIC run and ordered directly by IMB-CSIC was also fabricated. This additional die contains an isolated version of the LLSB ΣΔM and was also packaged in the frame of the project for further analysis and comparison between the isolated version of the LLSB modulator and the one sharing silicon with the rest of the modulators (in the CVB chip).

Regarding packages, the CVB chip was packaged using a plastic QFN64 and the CVC a plastic LQFP120. These packages were selected for having the lowest inductance possible from the list of available ones considering the

number of pins required for each case. Finally the LSSB ASIC was encapsulated on a QFN40 package.

Dice microphotographs are depicted in figures 3 to 5.

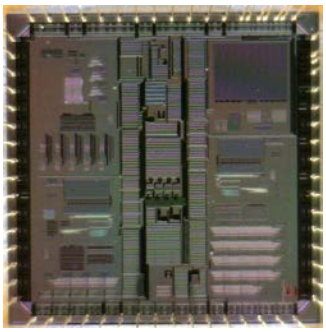

Figure 3: CVB001 die microphotograph

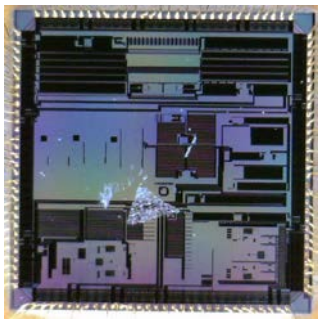

Figure 4: CVC001 die microphotograph

Figure 5: LSSB die microphotograph

B. Measurement boards

A few boards have been designed in the frame of the project to validate the functionality and the performances of the ASICs.

The objective of the CVB&CVC board 1 was to allow functional validation of the ASICs and perform preliminary measurements on each of the IPs. After this stage was completed the design was upgraded evolving in the CVB&CVC board 2. The main objective of the second board was to extend the functional validation capabilities of the setup, to allow the connection of high precision signal sources and to reduce the overall noise floor.

The objective of the LLSB board 1 was to be able to measure the high performance of the modulator. After mounting and debugging, the noise floor measured was around 20dB higher than was required and the distortion 10dB. In any case the measurements performed with this board proved to show the very good behaviour of the LLSB ΣΔM as will be discussed later. The board was upgraded to further improve the overall noise and distortion figures.

Boards are depicted in figures 6 to 9.

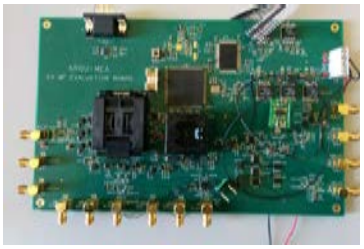

Figure 6: CVB&CVC board 1

Figure 7: CVB&CVC board 2

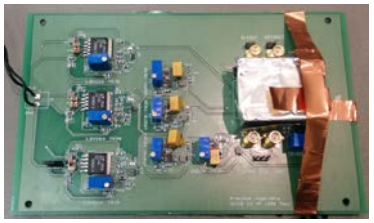

Figure 8: LSSB board 1

Figure 9: LSSB board 2

C. Signal source and measurement equipment

For the [0; 200] kHz range, the analogue input signal was generated with DS360 Standard Research Systems high quality source; for the [0.2; 5] MHz range, BK PRECISION 4064 source was used. The former can achieve 100dB of SNDR but can only go up to 200 kHz; the latter can reach higher frequencies but only achieves 80dB of SNDR. Keysight DSOS204A oscilloscope was used to monitor time domain signal and to perform a quick but moderate accuracy frequency analysis (up to 60dB of SNDR). Analogue Devices EVAL-AD7960FMCZ and EVAL-SDP-CH1Z boards were used to perform high accuracy frequency analysis (up to 90dB of SNDR).

D. Results

A summary of the main features measured on each of the selected IPs is shown in tables 10 to 12.

With regards to the LLSB ΣΔM, as can be seen in the tables, a slight degradation on its performance is observed between the version included in CVB and the standalone one. Additionally, the resolution reached is lower than the one predicted by the core simulations but in line with the chip level verification which indicates that the degradation is probably linked to pad and package limitations. Additional reults of the LLSB modulator can be found in [5].

LNA results indicate a THD lower than expected, which is currently being investigated. The most probable hypothesis is that the degradation is also linked to the influence of pad and package parasitics.

PA results show a very good correlation between verification and validation.

Table 10: LSSB ΣΔM in CVB validation results

Parameter	**Value**	**Unit**
Effective resolution	14	bits
Area	1.325 x 1.485	mm^2
Consumption	16	mA

Table 11: LSSB ΣΔM alone validation results

Parameter	**Value**	**Unit**
Effective resolution	15.5	Bits
Area	1.325 x 1.485	mm^2
Consumption	15	mA

Table 12: LNA validation results

Parameter	**Value**	**Unit**
THD	63	dB
Area	0.995 x 1.07	mm^2
Consumption	25	mA

Table 13: PA validation results

Parameter	**Value**	**Unit**
THD	73	dB
Area	0.61 x 1520	mm^2
Consumption	110	mA

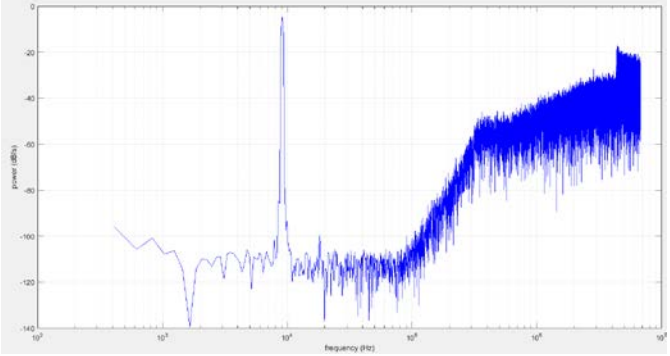

Figure 10: FFT of the LSSB ΣΔM in LSSB board 2

VI. CONCLUSIONS

A set of high performance and highly configurable IPs have been designed, verified and electrically validated in the frame of ESA's Cosmic Vision MF activity showing promising results. A single silicon run was used to implement the designs showing a very good correlation between verification and validation.

Further work on the IPs could tune or adapt performances for particular applications and further testing of the ASICs would allow additional data on all possible configuration modes.

VII. REFERENCES

[1] S.Redant, M. Hollriser (2002). A radiation-tolerant standard-cell library for a commercial deep sub-micron technology. RADECS 2002 procedings.

[2] S.Redant, R. Marec, L. Baguena, E. Liegeon, J. Soucarre, B. Van Thielen, G. Beeckman, P. Ribeiro, A. Fernandez-Leon. B. Glass. (2004). The design against radiation effects (DARE) library. RADECS 2004 procedings.

[3] ESA-ESTEC Data Systems Division/Microelectronics Sextion (2011, December). Space engineering product assurance-Techniques for Radiation Effects Mitigation in ASICs and FPGAs.

[4] Stepan Sutula (2015, November). Low Power High Resolution CMOS Switched Capacitor Delta Sigma Analog to Digital Converters for Sensor Applications. PhD Thesis.