

DSP and FPGA – Competition, Synergy, and Future Integration

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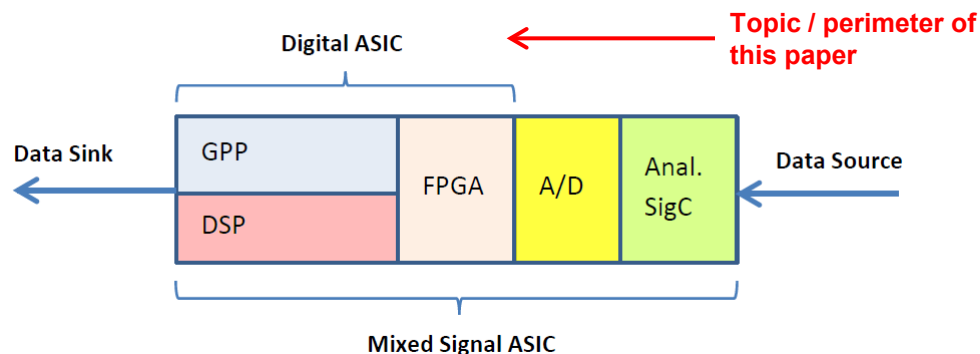
Presentation Overview

- Background - Signal Processing Chains & Technology Evolution
- DSP ASIC vs. FPGA - Strengths and Weaknesses
- Application cases for integrated DSP & FPGA
- Trade spaces and recent developments / future steps
- An architecture proposal for an FPGA- assisted DSP
- Summary

Signal Processing Chains and Technology Evolution

Signal processing chains typically include several of the following elements:

- Sensor devices / signal sources
 - Analogue signal conditioning
 - Analogue/Digital conversion
 - Interfacing to data converters
 - Digital Signal Processing
 - Application control and related processing
- traditional DSP ASICs, or GPP, and / or FPGA



The evolution of technology moves towards increasingly capable and complex SoCs, use of mixed signal (getting more and more of these elements onto the same piece of silicon) and use of reconfigurable logic (where flexibility is key)

=> These trends imply both challenges and opportunities for future DSPs

Processor ASICs have specific advantages in comparison to FPGA implementations of similar functions:

Speed – typically a processor (GPP/DSP) design is ~3-5 times faster when implemented in a dedicated hard IP / ASIC as compared to an FPGA implementation (same or similar technology node)

Example: LEON3 in ~180nm: 100 MHz in ASIC, 25 MHz in RTAX FPGA (150 nm)=> ~factor 4

Power consumption – typically a design in ASIC consumes a fraction of the equivalent FPGA implementation (same or similar technology node)

Example: LEON3 in ~180nm: ~0.8 Watts; in RTAX FPGA: ~2 Watts (scaled to same clock) => ~factor 3

Radiation hardness / ease of error mitigation - typically ASIC considered more reliable

Example: For critical applications, ASICs preferred to RAM-based FPGAs. Antifuse FPGAs however well accepted.

Price – typically an ASIC that sells in reasonable numbers costs much less than an FPGA big enough for a design of similar complexity

Example: LEON processor SoC ~25kEuro; Virtex or ACTEL ~50-70kEuro. For equipment manufacturers, cost of ASIC development is typically equivalent to buying several 10 large FPGAs => for several 10 products sold, ASIC preferable from a cost point of view

In return, rad-hard / rad-tolerant FPGAs have specific key advantages

Development time - for fast-turnaround, low-volume, or prototyping developments FPGAs are unbeatable (short term part availability, commercial equivalent ..)

Flexibility – processing hardware can be specifically adapted to project requirements. Trade-off between parallelism / speed and area / power consumption provides optimised designs.

Speed – any functionality that cannot be easily mapped on the available functions of ASSP ASIC are typically faster on FPGA.

Radiation hardness – superior to COTS solutions (which often are, in the absence of sufficiently performant rad-hard parts, the only alternative); typically acceptable for space

Price – for unique products or small volumes (up to several 10 pcs) even the large, expensive FPGAs are more cost efficient than dedicated ASICs

- ⇒ At the moment, schedule and foreseen production volumes decide whether FPGA or ASIC is better for a specific application
- ⇒ **For space-based Digital Signal Processing, a combination (hard IP and FPGA fabric) – ideally on the same chip - can combine the advantages of both, and lead to improved application performances**

In a combined DSP+ FPGA SoC*,

The hard IPs (GPP, DSP, NoC) can provide

- Reliable and efficient system control and FDIR functions for the application
- Software programmable processing power for algorithms that map well on these IPs
- Energy efficiency for major functional parts of the SoC
- Good real-time properties (very short reaction time in software via branch / interrupt)
- Management of the FPGA configuration

The FPGA fabric can provide

- Reconfigurable / quickly reprogrammable acceleration*
- Flexible logic for additional / specific (non-standard) interfaces, I/O
- Flexible glue logic for ADC / DAC, external companion devices

* Speed and cycle times depend on FPGA type (SRAM / Flash based FPGA)

Typical applications of an FPGA-equipped many-core DSP/GPP chip

Data Processing Units

- Very high and software reconfigurable processing performance
- High reliability (> COTS or ASIC + ext.FPGA), high power efficiency, uniform radiation hardness

Platform systems that need performance, high reliability, and design flexibility

- Future platform OBC that cover significant subsystem functions
- Star trackers, controllers for electro-optical/electro-mechanical/robotics systems, exploration OBCs

Payload Instruments

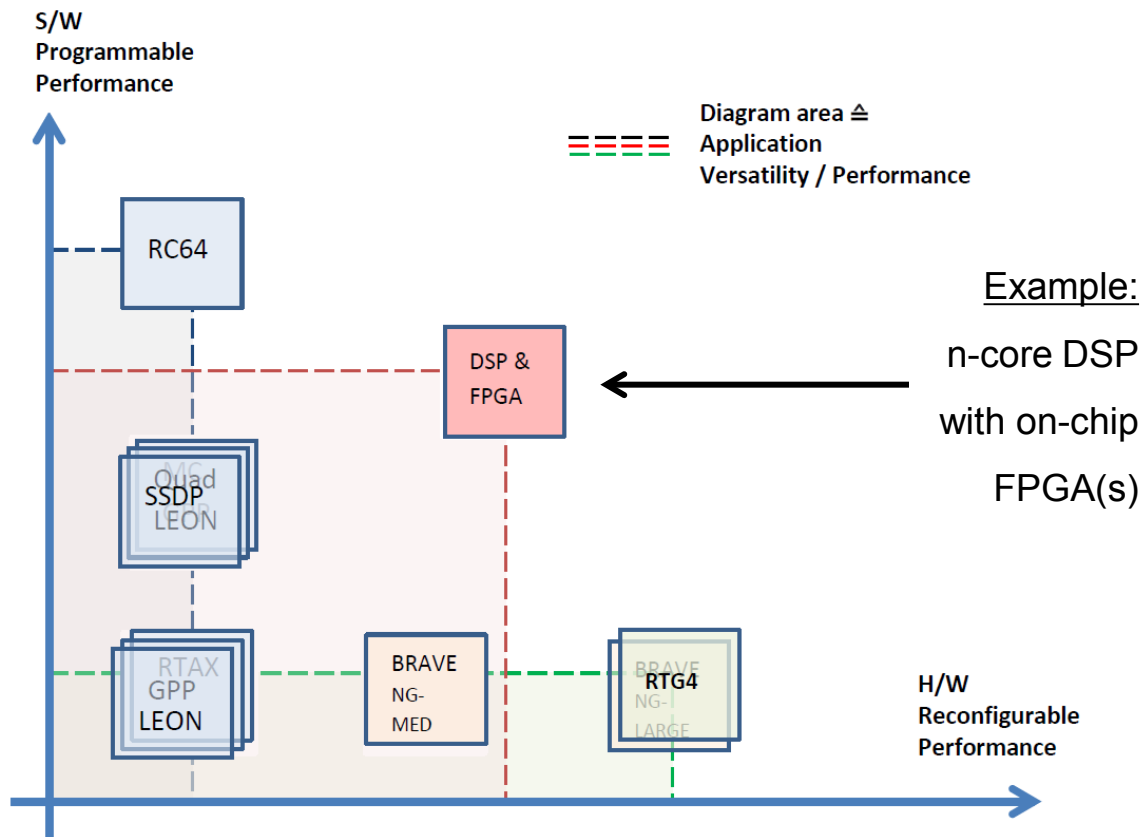
- On-chip FPGA saves dedicated separate FPGA chips for interfacing with ADC, DAC, detectors
- High power efficiency, high processing performance, small footprint

Telecom Systems

- High reliability, high performance, high on-chip / off-chip bandwidth applications
- Easy, SW-based reconfiguration of high performance blocks during mission (codecs, etc)

DSP+FPGA: Trade Spaces (1/2)

Recent developments in both the space processor / DSP and FPGA areas mainly provide increasing performance, but there is a significant gap between these development lines that is often difficult to bridge (software / design re-use, power efficiency, etc.)



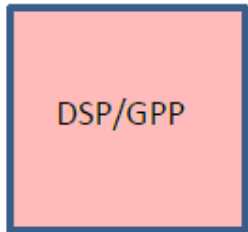
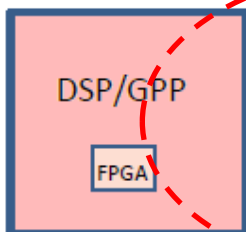
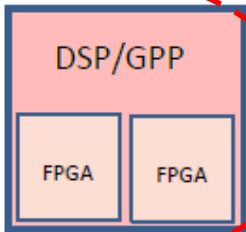
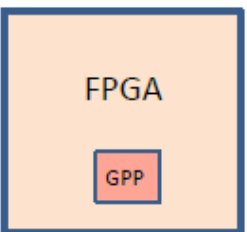
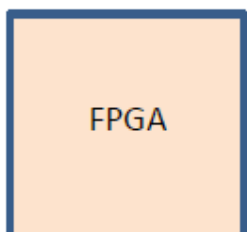
A combined DSP/GPP+FPGA SoC is expected to

- allow to combine the best of both worlds for many applications, in one device instead of two (like separate processor chip and FPGA -> single chip)
- support efficient co-development and re-use of both software and HDL IP
- Achieve the best balance between fixed and reconfigurable HW features

DSP+FPGA: Trade Spaces (2/2)

The trade-off space ranges from pure processor ASIC to pure FPGA. Intermediate products (mix of processor hard IP / FPGA fabric) are already existing (COTS) / planned (for space)

Optimum processor-FPGA mix range for maximized device attractiveness (power, application speed, functionality, versatility) ?

				
Pure DSP/GPP ASIC	DSP/GPP with on-chip small FPGA	Many-core with comparable size on-chip FPGA(s)	FPGA with on-chip processor core(s)	Pure FPGA
Examples: Space: LEONx, SSSDP, RC64 ... COTS: Many	Examples: Space: - (Next GPP?) COTS: -	Examples: Space: - (Next GSP ?) COTS: Xilinx Zynq	Examples: Space: - (NG-Large?) COTS: Many; Xilinx Virtex	Examples: Space: Virtex5, NG-MEDIUM, RTG4 ... COTS: Many

The following relevant technology developments are currently on-going in Europe (ESA supported R&D contracts):

DSP chips and related IP

- SSDP incl. FMs (TASE+RECORE+IMEC+Arquimea, CG, 2630kEuro, 2014-2018)
- Floating point DSP core development (RECORE, 300kEuro, 2016-2017)
- Improved NoC IP development (RECORE+CG, 350k, 2015-2017)

FPGA IP and chip developments

- BRAVE NG-MEDIUM (NanoXplore+STM, 3.6 MEuro, 2015-2018 TBC)
- BRAVE-NG-LARGE (NanoXplore+STM, details TBC)

Possible future steps enabled by these developments

- High-performance many-core DSP development (with or without FPGA) ?
- Large FPGA with embedded processor IP ? Processor with embedded FPGA ?

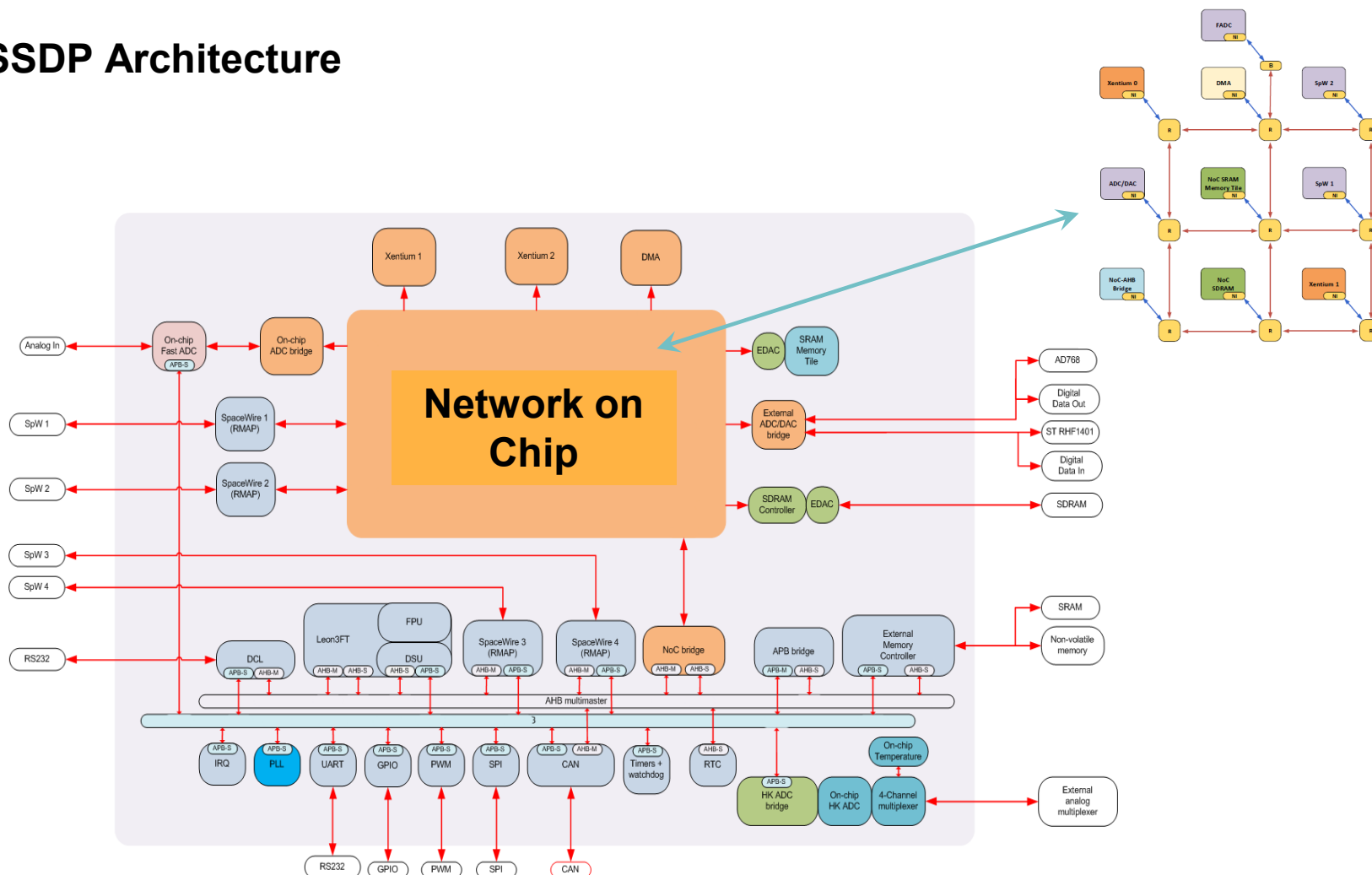
Needed for both DSP and FPGA

- Efficient, user friendly, compatible development environments !!!

Presentation Overview

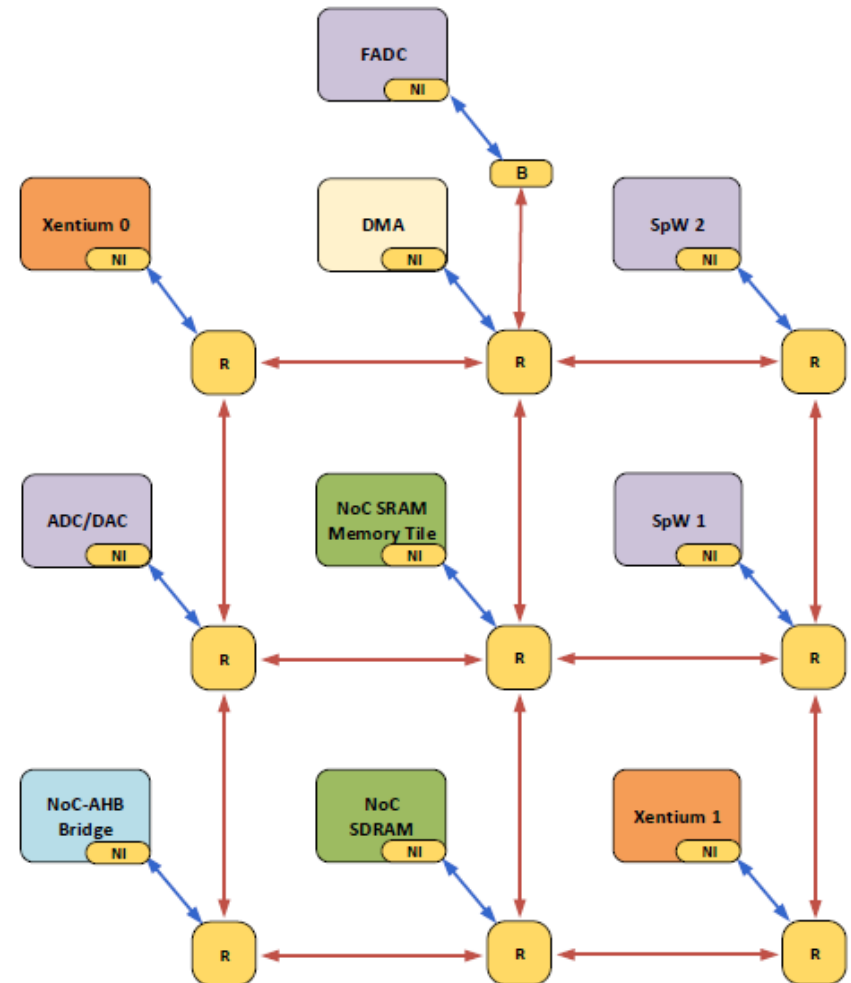
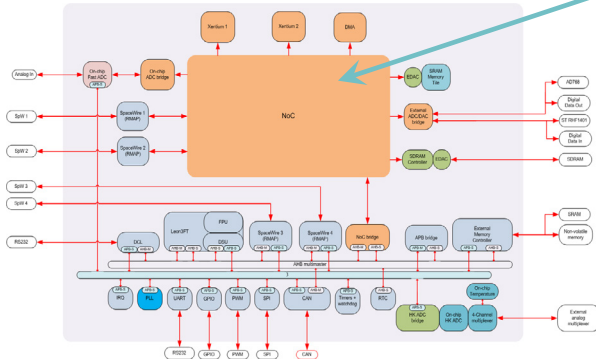
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- **An architecture concept for a new European FPGA-equipped DSP**
 - Background: SSDP architecture and typical programming model
 - Proposed FPGA integration in a NoC-based many-core DSP
- **Summary**

SSDP Architecture



SSDP NoC Architecture

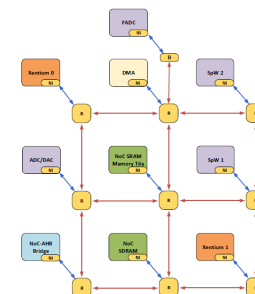
- 9 routers, 2 DSP cores
- Bi-dir 32bit NoC lanes @ sys speed
- SRAM, SDRAM, DMA
- SpW interfaces, ext ADC/DAC I/F
- All connected to NoC via memory mapped network interfaces (NI) that provide ctrl registers



Scalable Sensor Data Processor (SSDP) ASIC

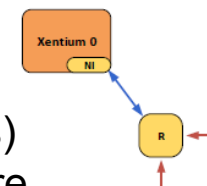
Key Specifications

- 180 nm mixed signal ASIC, 100 MHz, max 1700 MOps
- LEON3 GPP with typical peripherals
- NoC with 9 routers, lots of bridges to GPP, ADC/DAC, fast interfaces ...
- 2 Xentium VLIW DSPs => max 800 16 bit MOPs / max 400 32 bit MOPs per core
- Capable DMAs with stride, endian-ness handling in bridges / network interfaces



User SW aspects / programming model

- Memory mapping for all NoC / GPP connected elements (except DSP i-caches)
- Simple use of DSP cores for processing data, controlled by GPP processor core
 - Write data and / or configuration / ctrl parameters to DSP's local data memory or network interface register (mailbox)
 - Write application code address to DSP's network interface register (mailbox): NI then fetches code, DSP starts code execution in line with provided configuration
 - When DSP kernel completes, GPP interrupt is raised, DSP goes to idle / waits for new code address in MB
 - Input / output data transfers to/from DSP data memories typically per DMA which can be managed either per GPP or by the DSP cores (typically to / from data buffers in memory tile, SDRAM, or I/F FIFO)
- Principle is agnostic to what exactly is behind the network interface: data fetched from provided address can be code for a DSP core, but could also be configuration bitstream for SRAM based FPGA fabric => DSP / FPGA tile could be used transparent way by GPP



Based on European IP that is existing or becoming available, the development of a powerful, flexible, FPGA equipped GPP/DSP SoC becomes possible

Preliminary high level requirements

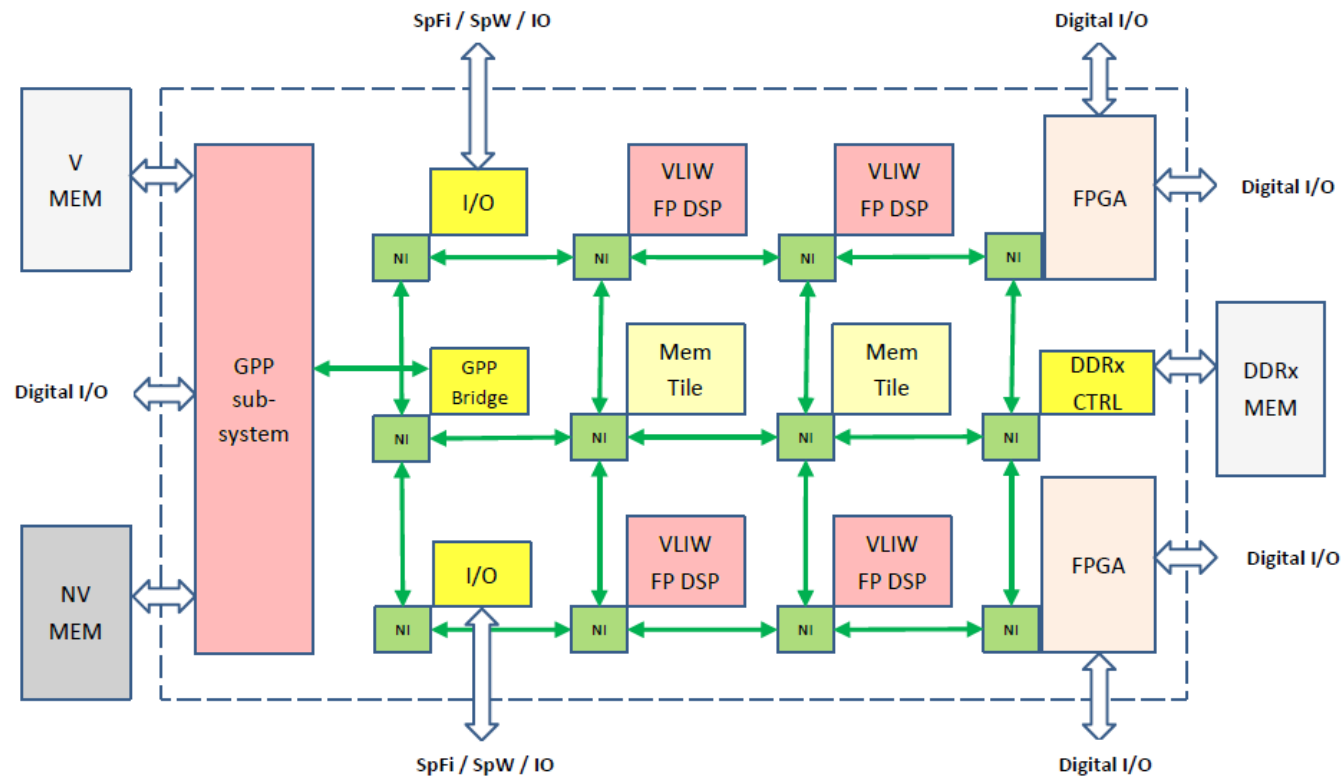
- Performance requirements derived from projected mission / application needs -> SoC performance is scalable via NoC & many-core
- Use of GPP core, floating point DSP IP, NoC IP from European sources / ESA IP portfolio
- Use of FPGA IP from European providers (NanoXplore, Menta, Adicsys)
- Re-use of general GPP – NoC architecture as in SSDP
- Re-use of GPP / DSP / FPGA software, tools, FPGA application HDL IP

Expected performances

- Very high processing performance, meeting application needs
- GPP-like real-time performance, FPGA-like flexibility
- Good power efficiency: tradeoff & optimization of FPGA size / number and type of hard IP blocks
- Reduced system resource needs: lower mass, footprint, power, cost

High level architecture: NoC-connected FPGA tiles in many-core DSP

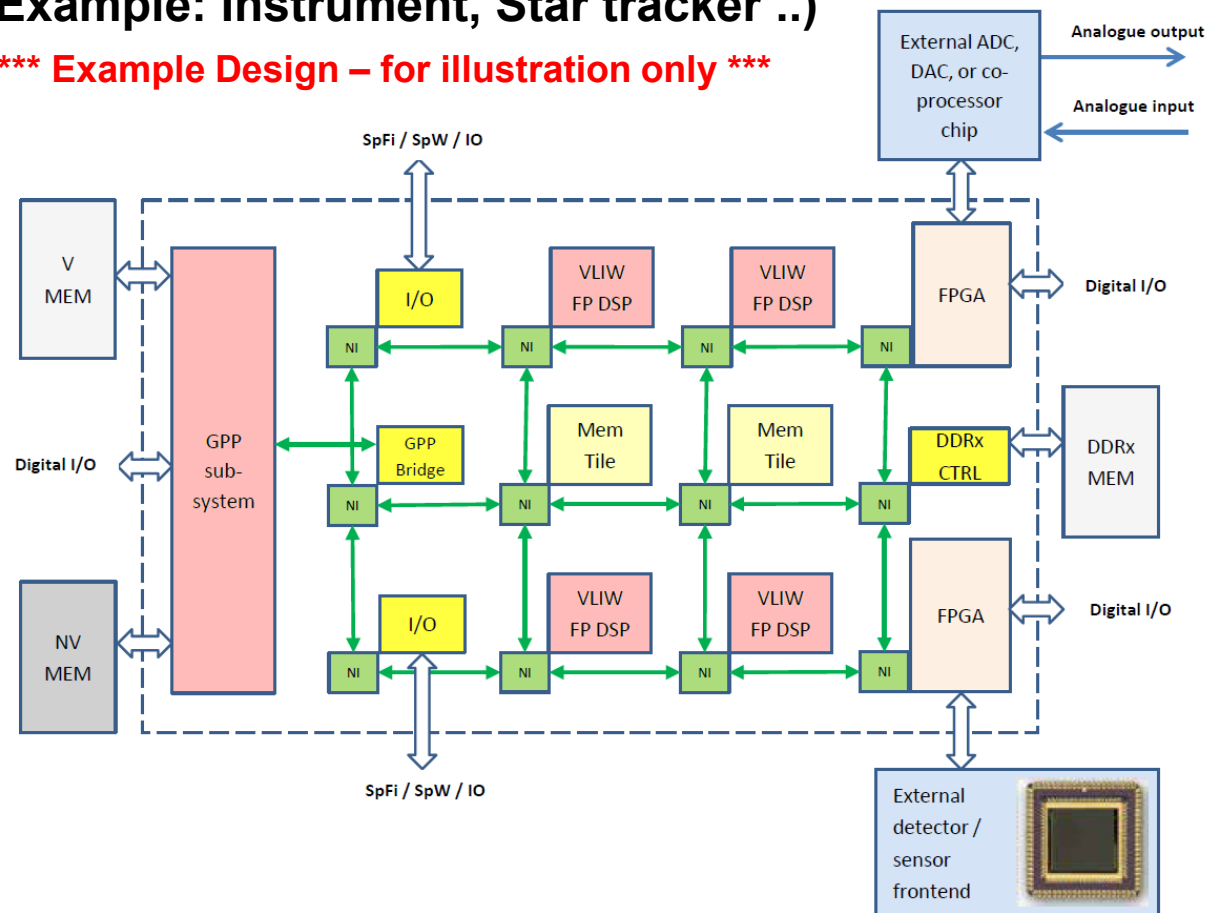
*** Example Design – for illustration only ***



- Number & type of DSP cores selected according to mission / application needs
- Size and number of FPGA tiles selected according to application needs
- Typically 1 memory tile per 2 DSP tiles
- At least 1 DDRx NoC connected memory, more possible
- HSSL/SpFi, SpW, GPIO via I/O bridges
- GPP subsystem incl peripherals (SPARC / ARM / RISC-V ?)

Using FPGA fabric as glue logic / simple pre-processor for external chips (Example: Instrument, Star tracker ..)

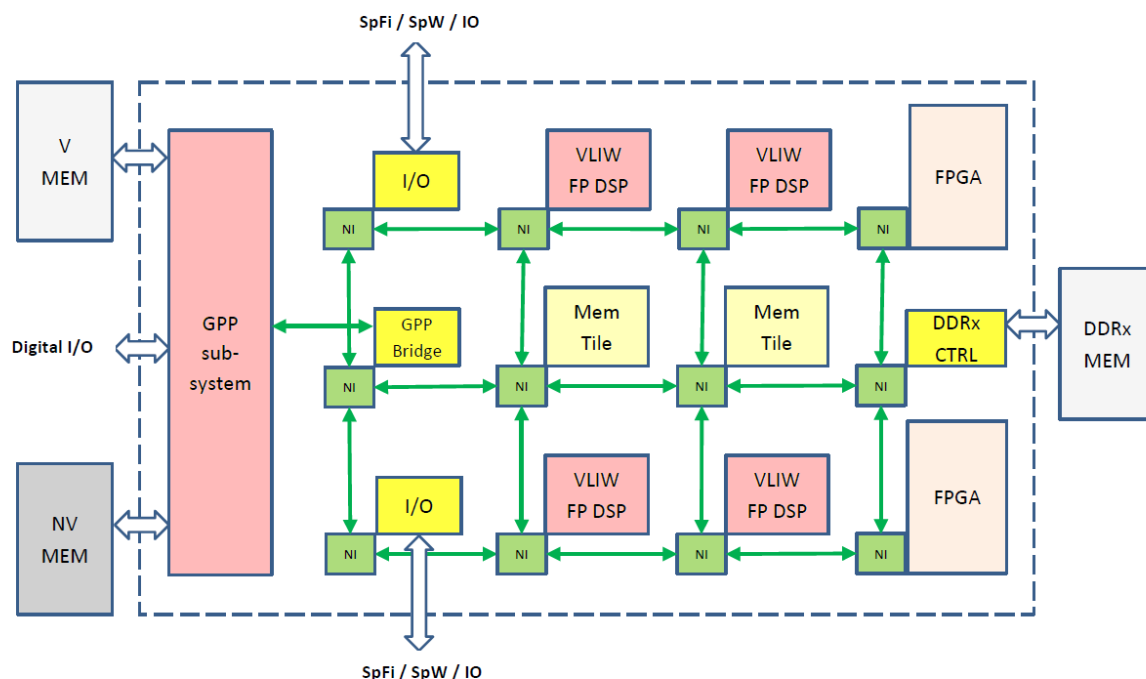
*** Example Design – for illustration only ***



- **General: FPGA configuration loaded at boot time, then maintained**
- **ADC, DAC interfacing**
- **Simple signal filters, adjustment of control signals**
- **Custom interfaces to peripherals**
- **Codecs for data streaming**
- **Replace ext. anti-fuse FPGA ?**
- **Bitstreams provided with SDE ?**

Using FPGA fabric as re-programmable co-processor for GPP and DSPs (Example: Payload Data Processing Unit)

*** Example Design – for illustration only ***



- **General: FPGA tile configuration re-loaded periodically**
- **Use is transparent for GPP** (DSP core / FPGA tile have similar interface: GPP provides bitstream / DSP code location, data buffer location, starts process, receives interrupt when proc. finished)
- **Fast co-processing functions:** data compression, codecs, specialized algorithms, highly parallel functions
- **FPGA access** to SoC infrastructure and memories via NoC
- **System control, FDIR, real-time functions by GPP**

FPGA equipped flexible DSP (“FlexDSP”) - **example** characteristics

Example Design Specs	Example FlexDSP Performance
65nm STM process, flip-chip (28 nm SOI possible ?)	250 MHz system clock; 6 Gbps HSSL
1 General Purpose Processor (GPP) with typical peripherals and memories (SPARC, ARM, other possible)	SPARC or ARM; 32/32 kByte D/I caches; CAN, Milibus, SPI, PWM, UART, GPIO etc.; NV memory + SRAM or SDRAM/DDR _x ,
N floating point DSP cores, 2 FP MACs / clock cycle	8 floating point cores => 8 GFLOP / 16 GOps software programmable performance
M FLASH or (more likely ?) SRAM based FPGA tiles	2 medium size FPGA tiles (NG-MEDIUM, RTAX-2000 like ?) => some 10 GOps configurable application performance
On-chip memory tiles (advised: 1 memory tile per 2 DSP cores), caches	1 AHB + 4 NoC mem tiles a' 256 or 512 kByte DSP: 64 kByte i-cache, 128 kByte d-memory
32-bit parallel, bi-directional NoC, running at system clock, feature rich DMA, packet switched, QoS, x-y R	NoC supports 8 Gbps bi-directional at 250 MHz; 24 DMA channels
High speed serial links - 2 platform + n payload Medium speed links (SpW) 2 platform + n payload	4 SpFi, each 6.25 Gbps gross / 5 Gbps net 4 SpW More / specific I/F possible in FPGA fabric
1 or more DDR _x controllers on NoC	DDR2/3 on NoC, 64 bits, 250 Mhz, providing at least 32 Gbps memory bandwidth

- Digital Signal Processor and also GPP ASICs have been first complemented, then partially replaced by FPGAs
- FPGAs are cost effective when small to medium number of products are envisaged; however, power efficiency, radiation performance, other issues remain
- Processor (GPP / DSP) ASICs / hard IPs are good solutions when power efficiency, software performance, rad hardness are required, economy of scale applies
- For a future SoC, the ideal mix seems to be hard IPs (GPP, DSP cores, HSSL ..) where speed, power efficiency, reliability, Si area efficiency is needed, plus FPGA fabric where flexibility is desired. A large design tradeoff space exists that is waiting to be explored!
- GPP, DSP core, NoC IP is available or under advanced development in Europe; an GPP/DSP/NoC based ASIC design that combines these elements (SSDP) is under advanced development.
- FPGA technology is under development in Europe, with first prototypes (BRAVE NG-MEDIUM) expected Q4 2016
- An example many-core SoC design with on-chip FPGA tiles was introduced; other designs are possible and should be explored
- Development of a new type of powerful and flexible space processor becomes possible; expected to be attractive for DPUs, OBCs, payloads, subsystems, telecom. Significant re-use of existing European IP is possible -> detailed analysis / user requirements consolidation needed

- In general, future SoC developments (not only DSP but also others) can be expected to include FPGA fabric to add flexibility and application performance
 - Integration studies need to be performed to assess and evaluate the various FPGA fabric integration options
 - Memory mapped / NoC connected / standardized interface ?
 - Advantages of FPGA type (SRAM ? Flash ?) and related characteristics / utilization constraints
 - FPGA fabric size tradeoffs, and related logic / DSP / memory tradeoffs
 - Prototyping activities need to be started to test and demonstrate the various integration options, and investigate user / tool aspects and needs
 - Test FPGA fabric integration options (on large FPGA prototyping board, using eFPGA IP)
 - Integrate with GPP, DSP, NoC; test re-configuration, test task switching in application context, software aspects, FDIR
 - Assess ease of use / development environments and related integration / related improvement needs
- ⇒ If interest is confirmed by industry feedback, ESA will push for R&D activities covering these areas, to have results available on time for the following ASIC R&D cycle (TRP, other ESA programs)
- ⇒ **Companies interested in this type of work please feel free to contact roland.trautner@esa.int**