DSP Benchmark Results of the GR740 Rad-Hard Quad-Core LEON4FT

Cobham Gaisler
June 16, 2016

ESA DSP DAY 2016
Overview

GR740 high-level description

• GR740 is a new general purpose processor component for space
  - Developed by Cobham Gaisler with partners on STMicroelectronics
    C65SPACE 65nm technology platform
  - Development of GR740 has been supported by ESA

• Newest addition to the existing Cobham LEON product portfolio
  (GR712, UT699, UT700)
  - The GR740 will work with Cobham Gaisler ecosystem:
    • GRMON2
    • OS/Compilers
    • etc …
Overview

GR740 high-level description

• Higher computing performance and performance/watt ratio than earlier generation products
  – Process improvements as well as architectural improvements.

• Current work is under ESA contract “NGMP Phase 2: Development of Engineering Models and radiation testing”

• Development boards and prototype parts are available for purchase

Already available!
contact: sales@gaisler.com
Overview

Block diagram

- Architecture block diagram

M = Master interface(s)
S = Slave interface(s)
X = Snoop interface
Overview

Block diagram

• Architecture block diagram (simplified)
Features summary

Core components

- **4 x LEON4 fault tolerant CPU:s**
  - 16 KiB L1 instruction cache
  - 16 KiB L1 data cache
  - Memory Management Unit (MMU)
  - IEEE-754 Floating Point Unit (FPU)
  - Integer multiply and divide unit.

- **2 MiB Level-2 cache**
  - Shared between the 4 LEON4 cores
Features summary
Floating point unit

• Each Leon4FT core comprises a high-performance FPU
  – As defined in the IEEE-754 and the SPARC V8 standard (IEEE-1754).
  – Single and double precision floating-point numbers

• The design combines
  – a fully pipelined unit for most operations
  – a non-blocking iterative unit for execution of divide and square-root operations
Features summary

Floating point unit

• Types of floating-point operations:
  - addition, subtraction, multiplication, division and square-root, compare, convert and move

• Arithmetic operations have one clock cycle throughput and a latency of four clock cycles
  - Except divide and square-root operations that have a throughput of 16 - 25 clock cycles and latency of 16 - 25 clock cycles
  - Latency can be hidden by scheduling instructions

1: fmul A
2: fadd A

8 FLOP/8 cycles

1: fmul A
2: fmul B
3: fmul C
4: fmul D
5: fadd A
6: fadd B
7: fadd C
8: fadd D

2 FLOP/8 cycles
Features summary

Core components

• System-on-chip based on AHB bus infrastructure

• SDRAM controller with EDAC and scrubber

• PROM/IO controller with EDAC

• 5 x Timer, 5 x IRQ controller

• IOMMU for peripheral DMA

• Debug support and debug interfaces (for GRMON connection)
  – Ethernet EDCL (using either of the two MACs above)
  – JTAG
  – Spacewire RMAP (using separate GRSPW2 for debug only)
Features summary

Interfaces

• Communication Interfaces
  - 8-port Spacewire router with on-chip LVDS
  - 2 x 1Gbit/100Mbit Ethernet MAC
  - PCI master/target with DMA, 33 MHz
  - Dual-redundant CAN
  - MIL-STD-1553B interface (bus A/B)
  - 2 x UART
  - 16 x GPIO
Features summary

Fault tolerance

• Design is radiation hardened using multiple techniques
  - C65SPACE process and cell libraries designed and characterized for radiation hardness
  - Memories SEU-protected at design level using EDAC schemes.
  - TMR techniques used in selected parts of design

• Hardness to be validated by radiation testing (SEE, TID) on prototype.

• Baseline is to re-use exact same ASIC design and package for future flight models.
Key performances

Clock frequencies

• System clock (CPU:s, L2Cache, on-chip buses)
  - Nominal frequency is 250 MHz, generated by PLL from external 50 MHz clock (STA and prod. test)
  - Full temp range (-40 to +125 Tj) with margins for aging and clock jitter
  - 4 CPUs x 250 MHz x 1.7 DMIPS/MHz = 1700 DMIPS

• Memory clock
  - 100 MHz supported internally and achieved on evaluation board (using commercial SDRAMs and external clock buffer).

• Clock gating capabilities for unused interfaces and cores.
Key performances

Clock frequencies

• **Spacewire PHY: 400 MHz**
  - Generated by separate PLL from external clock input (50 MHz nom)
  - Receiver is sampling with DDR

• **Gigabit Ethernet**
GR740 Evaluation board

- Double eurocard form factor
- GR740 prototype device
- 256 MiB SDRAM with ECC
- 8 MiB NOR Flash
- Interfaces of the chip (2xEth, 8xSpW, PCI, UART, CAN, 1553, PROM/IO) available
- Use stand-alone with standard 5-12V power supply or mount in compact-PCI rack.
- Connect with GRMON using USB

See it live at our exhibit table in the break!

contact: sales@gaisler.com
Benchmarking effort on GR740

• A benchmarking campaign is currently ongoing
  - Mainstream CPU benchmarks: Dhrystone / Whetstone, CoreMark, EEMBC, SPEC2000, Parsec
  - Custom micro-benchmarks
  - Some of these benchmarks are interesting for a DSP-audience

• CoreMark result comparison:
  - UT699: 1.50 CoreMarks / MHz
  - GR712RC: 1.86 CoreMarks / MHz / core
  - GR740: 1.97 CoreMarks / MHz / core

• More results to be presented within next couple of months
• In addition, reference workloads to measure power consumption
EEMBC automotive/industrial benchmarks

Description

• EEMBC automotive contain several signal processing algorithms benchmarks interesting for a DSP audience
  – FIR and IIR filter
  – FFT and iFFT transformation
  – iDCT transformation
  – Basic integer and floating point arithmetic
  – Results can be compared with COTS devices in www.eembc.org
  – Results are obtained with out-of-the-box C code.
    • Better results are expected with optimized code
EEMBC automotive/industrial benchmarks

Basic arithmetic, FIR and IIR filter

• EEMBC Integer and floating point arithmetic:
  - Each iteration performs the following computation: \( \arctan(x) = x \times P(x^2)/Q(x^2) \), where P and Q are polynomials with 9 coefficients.
  - 1.67 usec per iteration

• EEMBC FIR filter:
  - Each iteration computes the result of a 35-tap FIR low pass and a 35-tap FIR high pass filter in series
  - 6 usec per iteration (85.7 nsec per tap)

• EEMBC IIR filter:
  - Each iteration computes the result of a Direct-Form II N-cascaded second-order High- and low-pass IIR filter.
  - 11.3 usec per iteration
EEMBC automotive/industrial benchmarks
FFT, iFFT and iDCT

• EEMBC FFT and iFFT:
  - Each iteration computes the result of 512 fft and ifft transform over and input signal with 4096 samples.
  - FFT: 1.1 ms per iteration
  - iFFT: 1 ms per iteration

• EEMBC iDCT:
  - Each iteration computes the result of a 8x8 block iDCT transformation on a 1KiB image.
  - 82.2 usec per iteration
EEMBC automotive/industrial benchmarks

Comparative

• EEMBC automotive compared to other processors

![Bar chart comparing processors](image)

- STMicro ST20C2 @ 50 MHz
- NXP i.MX21 @ 266 MHz
- NEC VR5000 @ 250 MHz
- Infineon TriCore/TC11IB @ 96 MHz
- Infineon TC1796 @ 150 MHz
- Cobham Gaisler GR740 @ 250 MHz

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Normalized iterations/sec</th>
</tr>
</thead>
<tbody>
<tr>
<td>STMicro ST20C2 @ 50 MHz</td>
<td></td>
</tr>
<tr>
<td>NXP i.MX21 @ 266 MHz</td>
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<td></td>
</tr>
<tr>
<td>Cobham Gaisler GR740 @ 250 MHz</td>
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</tbody>
</table>

• Benchmarks are not parallelized
  - We have run multiple instances in parallel using Linux support.
  - Due to their small size, that fits on the L1, they show almost a perfect scalability (4x).
### EEMBC automotive/industrial benchmarks

Comparison with other DSPs

- **Data provided by ESA**

<table>
<thead>
<tr>
<th>chip</th>
<th>TSC 21020 Rad-hard chip</th>
<th>DARE+MPBB demo chip</th>
<th>NGDSP example (21469 hardened)</th>
<th>TI 6713 - COTS based computer</th>
<th>GR740 (non-optimized code)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Max theor. Performance @ Clock</td>
<td>60 MFLOP (IEEE)</td>
<td>140 MFLOP (*)</td>
<td>1.35 GFLOPS (IEEE)</td>
<td>1.2 GFLOP (IEEE)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>20 MIPS @ 20 MHz</td>
<td>300 MIPS @ 100 MHz</td>
<td>225 MIPS @ 225 MHz</td>
<td>200 MIPS @ 200 MHz</td>
<td></td>
</tr>
<tr>
<td>Type</td>
<td>1 DSP</td>
<td>1 GPP + 2 DSP</td>
<td>1 DSP</td>
<td>1 DSP</td>
<td></td>
</tr>
<tr>
<td>1024 pt FFT</td>
<td>975 usec</td>
<td>47 usec</td>
<td>40.88 usec</td>
<td>142 usec</td>
<td></td>
</tr>
<tr>
<td>1 MAC (FIR 1 tap)</td>
<td>50 nsec</td>
<td>5 nsec</td>
<td>2.22 nsec</td>
<td>2.5 nsec</td>
<td></td>
</tr>
</tbody>
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CCSDS Lossless compression

Software provided by ESA

- **CCSDS 121 Lossless compression**
  - Lossless RICE compression according to the Recommended Standard CCSDS 121.0-B-2.
  - C reference software provided by ESA.
  - 2.06 seconds for 1 MiB input image (16-bit sample).

<table>
<thead>
<tr>
<th>TI 6727 DSP</th>
<th>GR740</th>
</tr>
</thead>
<tbody>
<tr>
<td>Msamples/s</td>
<td>0.592</td>
</tr>
</tbody>
</table>

- **CCSDS 123 Hyperspectral Compression**
  - Lossless compression for hyperspectral and multispectral images according to the Draft Recommended Standard CCSDS 123.0-R-1.
  - C reference software provided by ESA.
  - 644.21 seconds for 35 MiB input image.
Parallel applications on the GR740

PARSEC 2.1 results

• PARSEC are multithreaded benchmarks.
  - Representative of shared-memory programs for multiprocessors.
  - Evaluates performance of parallel applications

![PARSEC 2.1 benchmarks](image)
Interference on the GR740

• When multiple cores are running they compete for resources:
  – Shared CPU bus is the main source of interference

• Non-blocking L2 cache using SPLIT protocol
  – CPU waiting on an L2 cache miss does not block the bus.
  – Reduces interference.

• Micro-benchmarks show a 3.3x improvement in a extreme scenario
Conclusions

• The GR740 provides a significant performance increase compared to earlier generations of European space processors
  - High-speed interfaces on-chip
  - Improved support for profiling and debugging
  - Software tools and backward compatibility with existing SPARC V8 software

• The GR740 constitutes the engineering model of the ESA NGMP:
  - Developed under ESA contract
  - The GR740 is also fully developed in Europe

• The GR740 is the highest performing European space-grade processor to date
Product availability and schedule

- Development boards and prototype parts are available for purchase
- Additional characterization of silicon, resolving TBDs of datasheet values during 2016
- Radiation testing of prototypes during 2016
- Qualification phase expected 2016/2017
END OF PRESENTATION

• Thank you for listening!

Website: www.gaisler.com/gr740

For questions contact: sales@gaisler.com
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Presenter: Javier Jalle

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