RECORE
Many-core made easy

Multi-core DSP sub-system IP

Reliable on-board payload data processing

RECORE

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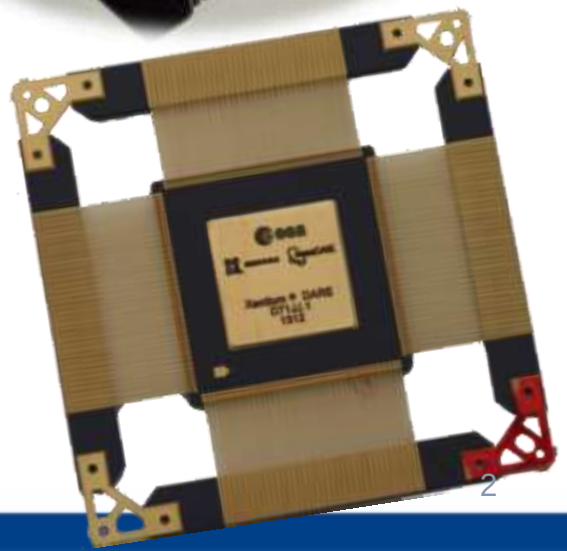
about Recore Systems BV

- Fabless semiconductor company
  - Based in Enschede, The Netherlands
  - Established in September 2005
- Business
  - Intellectual Property (IP) design & licensing
  - Platform devices (FlexaWare)
- Technology keywords
  - Digital Signal Processing
  - multi-/many-core System-on-Chip
- Focus
  - Payload data processing (e.g. space instruments)
  - Beamforming (e.g. advanced radar systems)



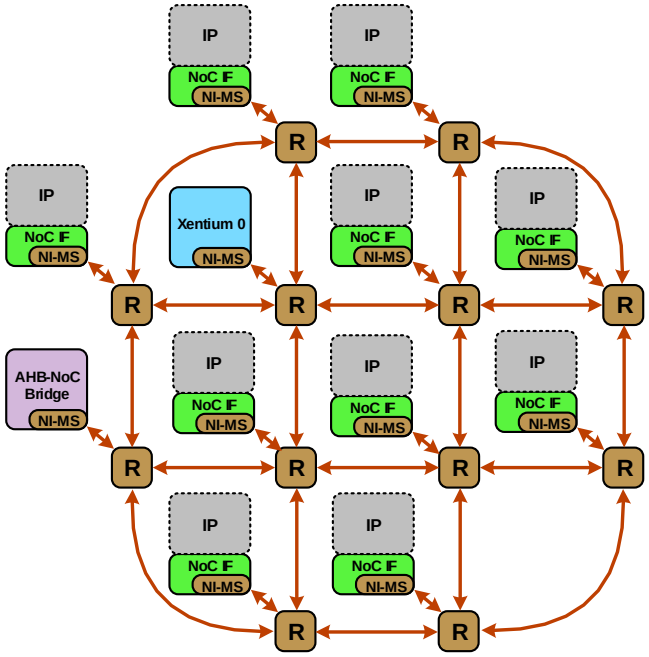
Quest for reliable processing power in space

- Need for more DSP processing for on-board payload data processing
  - To match sensor improvements
    - Increased diversity and versatility of sensors requires more control
  - Increased data rates and data volume
    - Requires increased processing performance and improve data compression
- Deep space science missions
  - Low transmission bandwidth
  - High radiation
  - Small power budget

Multi-core DSP needed

1) Xentium DSP IP
   – Powerful Digital Signal Processor

2) Network-on-Chip IP
   – Qualtity-of-Service on-chip interconnect



Multi-core DSP sub-system design expertise

- More processing power in chip!
- Fault-tolerant on-chip interconnect
- Heterogeneous processor platforms

On-going ESA activities

- ESA CTP activity:
  - Scalable Sensor Data Processor (2014 – 2017)
- ESA TRP activity:
  - MPPB firmware upgrade (2015-2016)
  - Data Compression Software on Xentium DSP (2015-2016)
  - Floating-point DSP development (2016 – 2017)
  - Fault-tolerant Network-on-Chip development (2015 – 2017)

Recore's step-wise approach into space

Fault-tolerant DSP subsystem combined with proven Leon subsystem:

- NoC-based Xentium DSP multi-core
- Heterogeneous and scalable

Step 1: Multi-core DSP prototype
Step 2: Rad.-hard prototype IC
Step 3: Rad.-hard multi-core DSP IC

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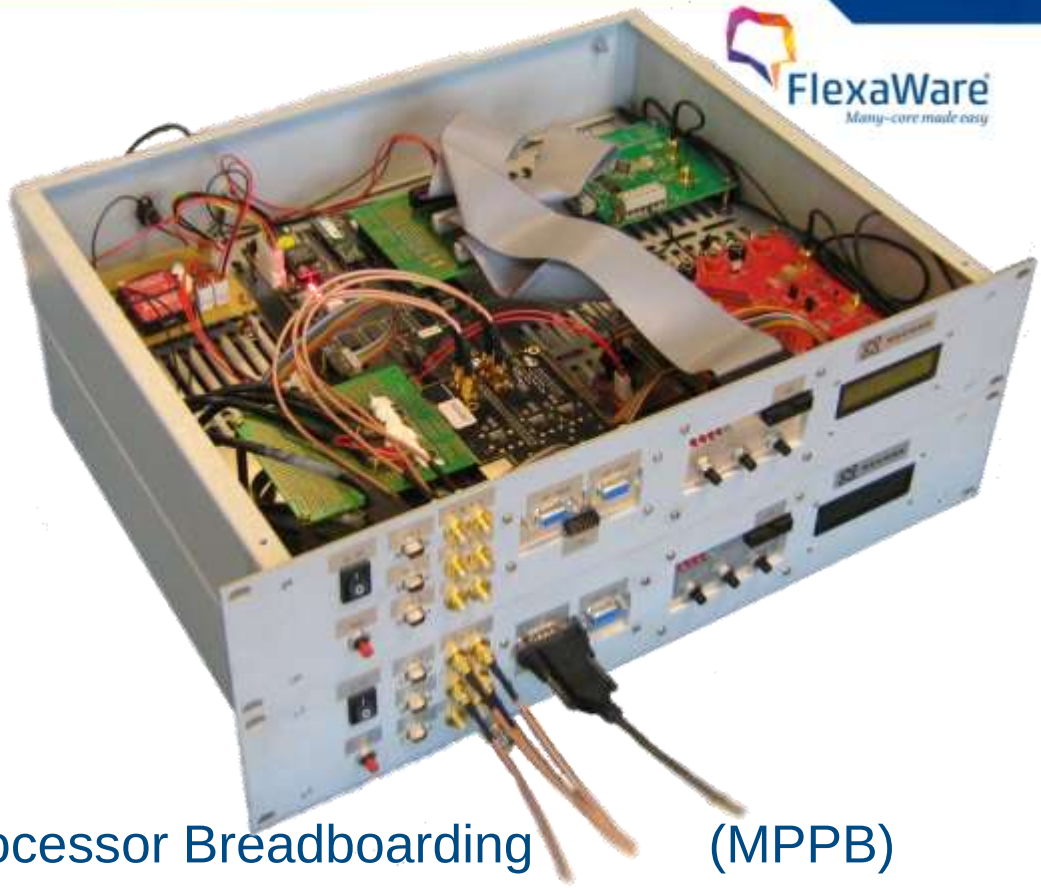
Demonstrated by

ThalesAlenia Space
A Thales / Finmeccanica Company

at ESA DSP day 2016



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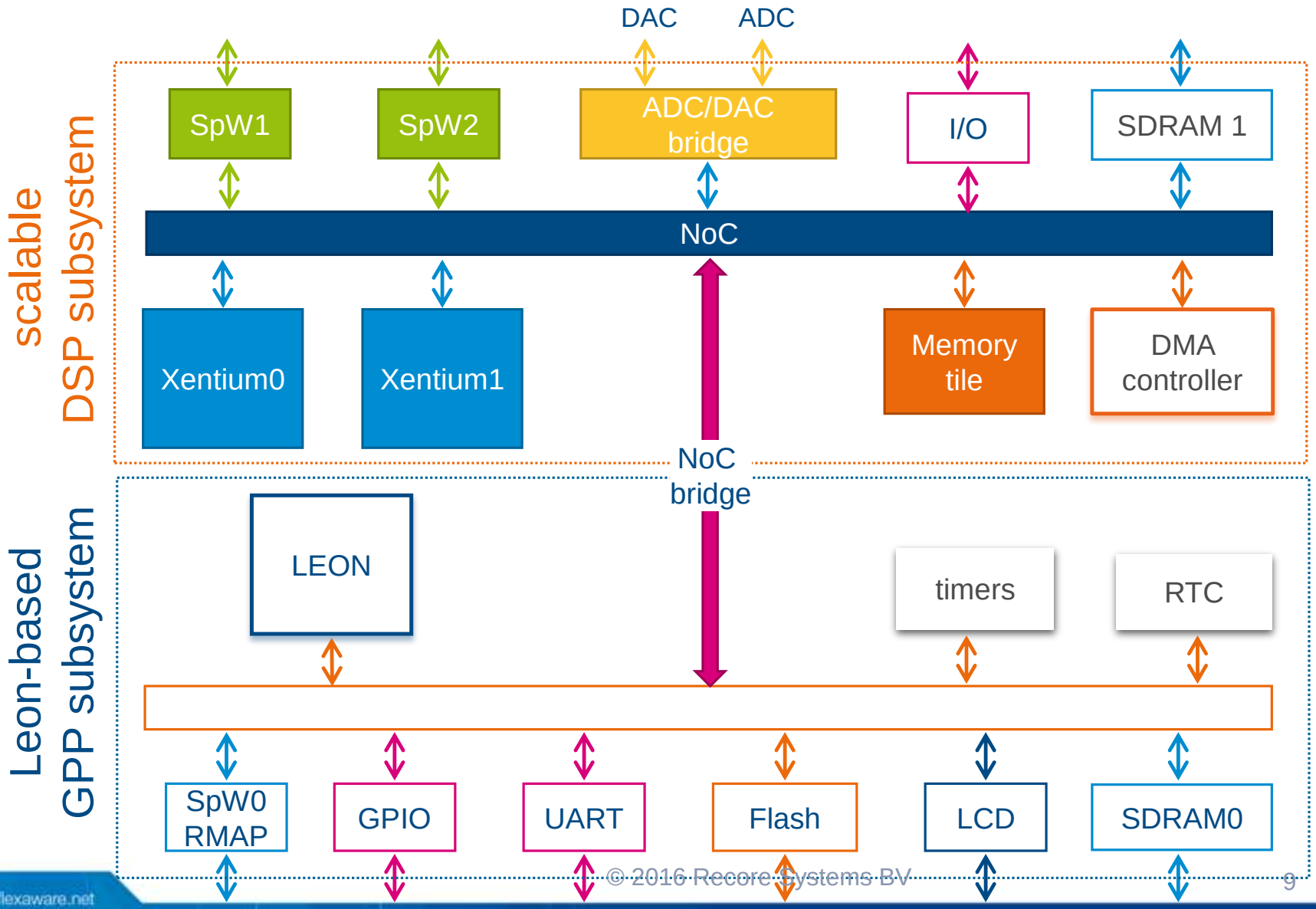
Step 1 – Massively Parallel Processor Breadboarding (MPPB)

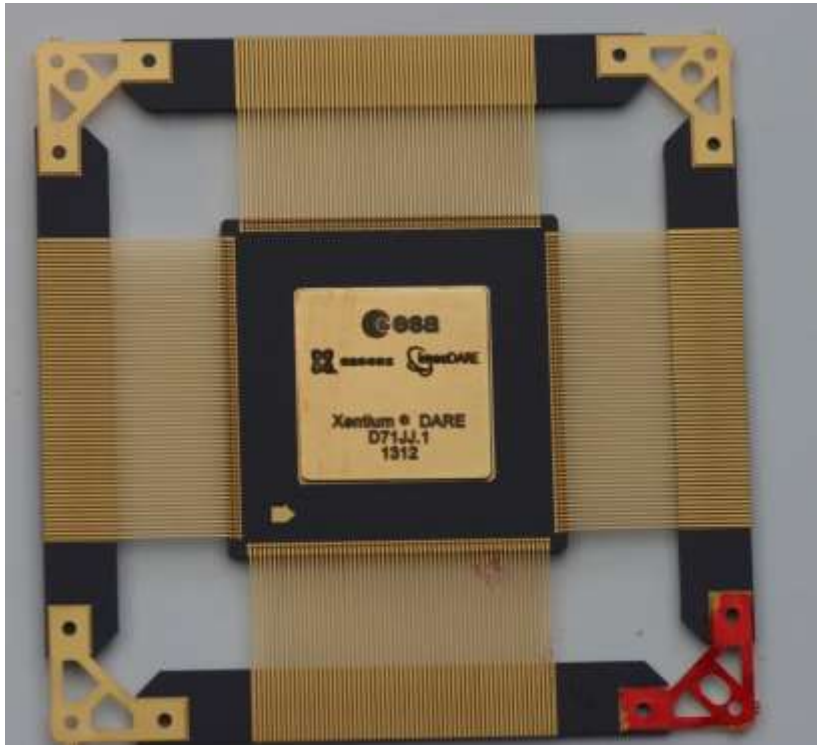
FUNCTIONAL PROTOTYPE

MPPB architecture



IP validated under radiation:

- Xentium IP
- NoC router
- NoC-SpW interface
- NoC-ADC/DAC interface



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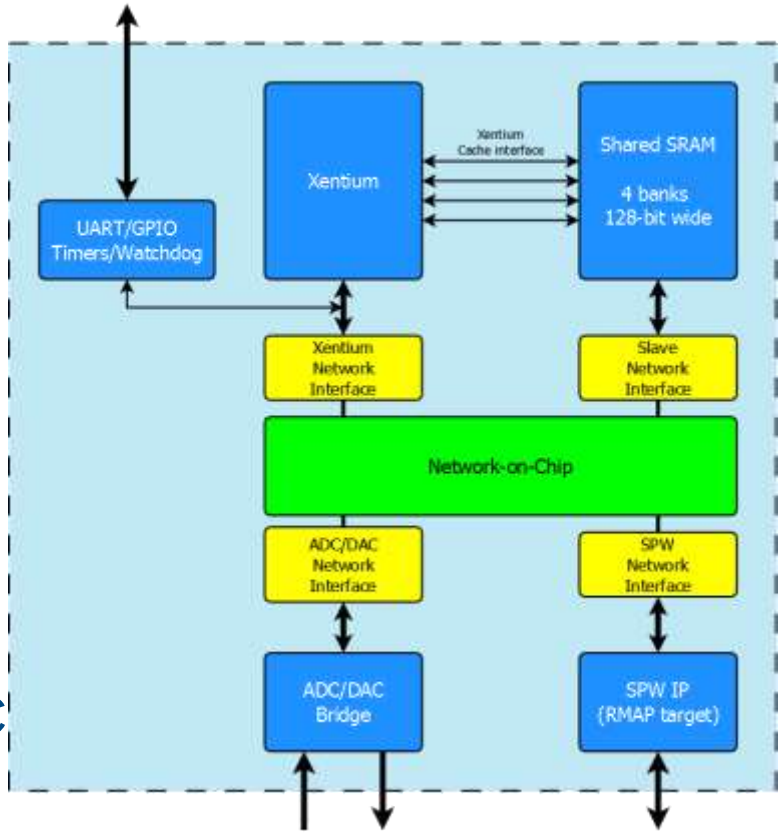
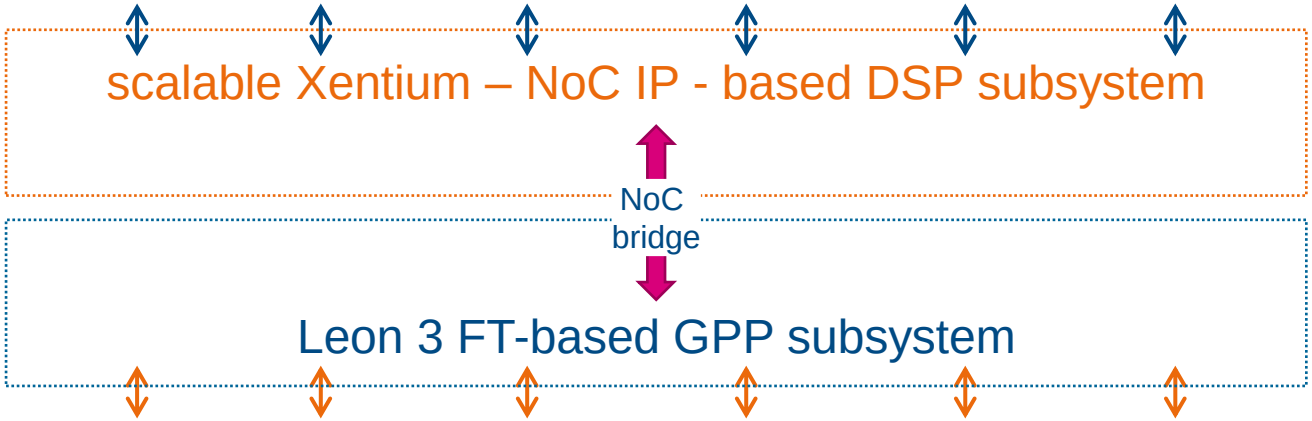
Step 2 – XentiumDARE

RAD.-HARD SILICON PROTOTYPE

Rad.-hard DSP and NoC prototyping in DARE180

- ASIC Prototype
  - –DARE180 CMOS technology
    - Available area: 5x10 mm^2
  - –Architecture
    - 1 Xentium core @**100MHz**
    - Network-on-Chip
    - SpW-RMAP interface
    - Bridge interface to external ADC/DAC
    - Small memory tile





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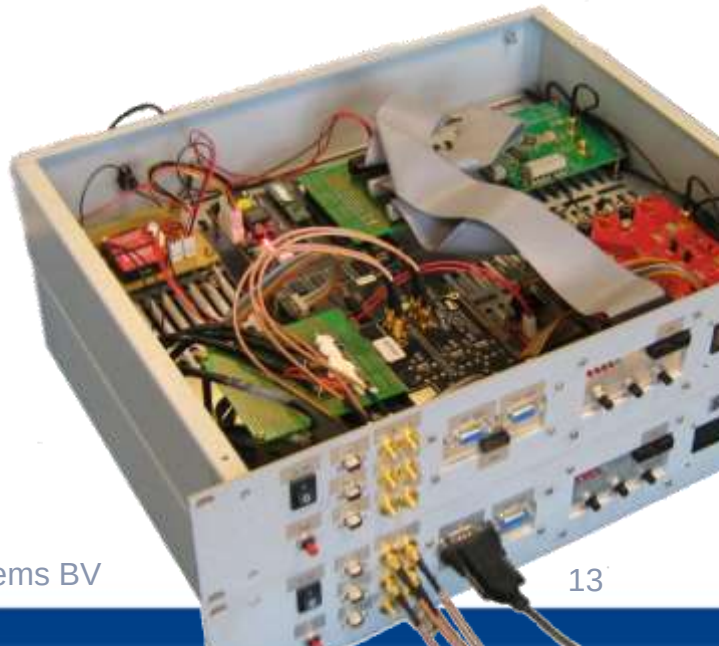
Step 3 – Scalable Sensor Data Processor (SSDP)

RAD.-HARD MULTI-CORE DSP

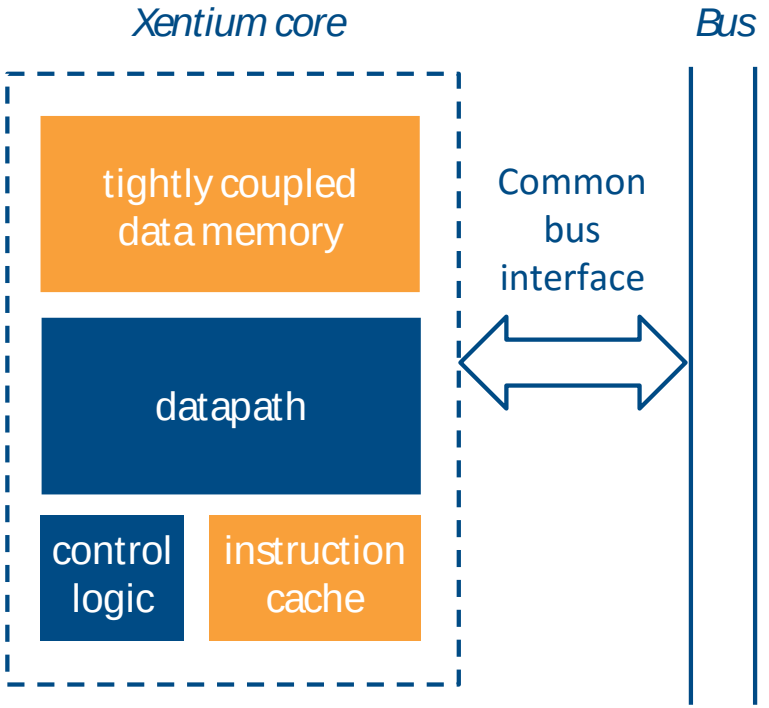
SSDP Architecture Improvements (available as MPPB 2.0)

- Xentium hardware debug support
  – GDB support: stepping, watchpoint, breakpoint, register view, …
- Multi-core debug support (Cross Trigger Unit)
  – Debug synchronisation between Xentium and Leon cores
- Xentium performance counters
  – Hardware profiling support
- 2D DMA support in Network-on-Chip
  – source and destination strides
- Chip2Chip interface
  – Off-chip NoC flow control



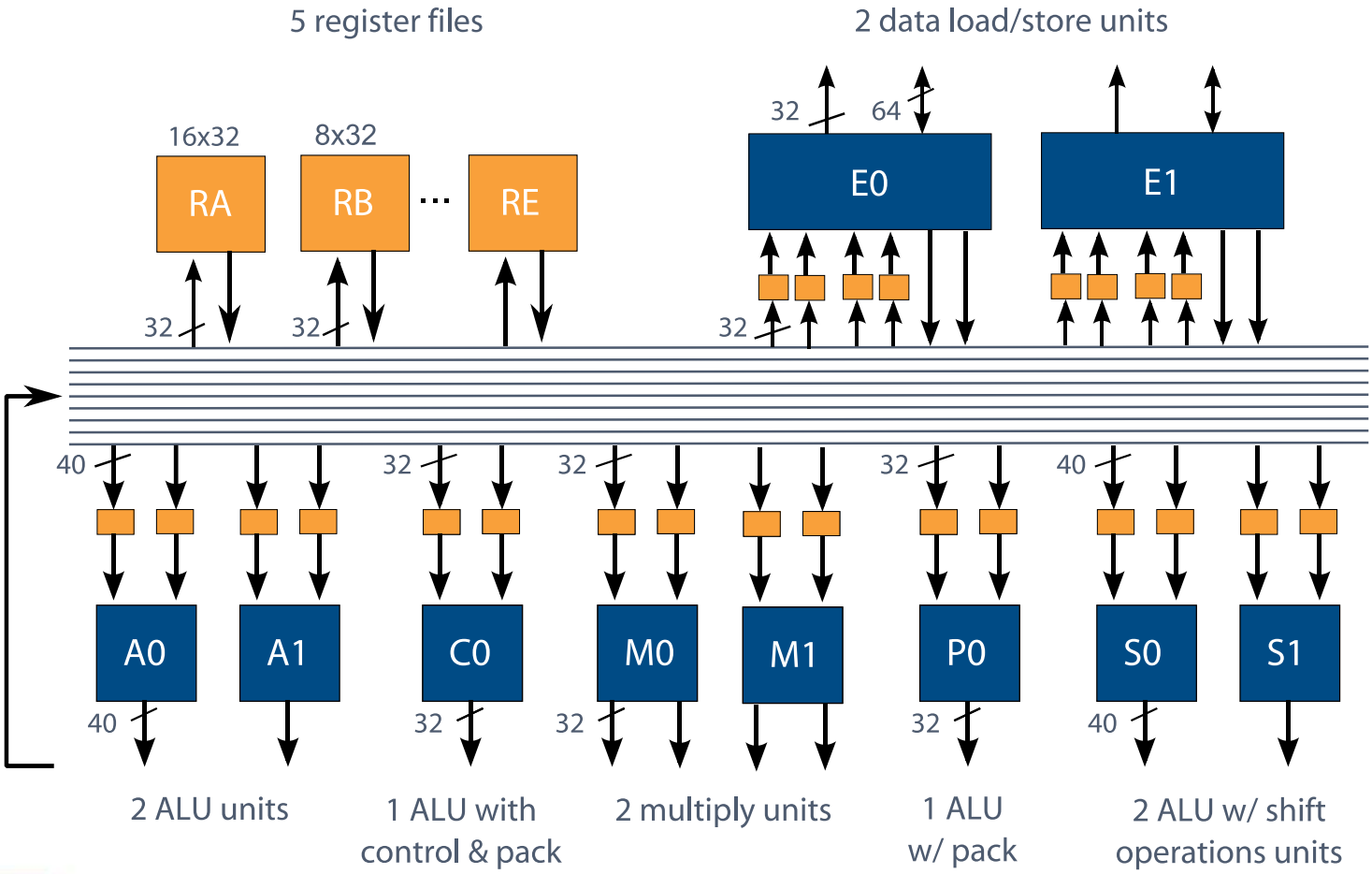
Xentium DSP - Highlights

- Programmable high-performance VLIW DSP:
  - 10 parallel execution units in datapath
  - 32/40-bit fixed-point datapath
  - 16-bit SIMD
- Features
  - Single cycle latency Data Memory
  - Single cycle instruction cache latency
  - Short 3-cycle pipeline
  - Efficient complex MAC execution: 2 16-bit **complex** MACs/cycle
  - Register bypassing (latency, energy efficiency, code size)
  - Loop buffer (energy efficiency, code size)
  - Hardware debug infrastructure

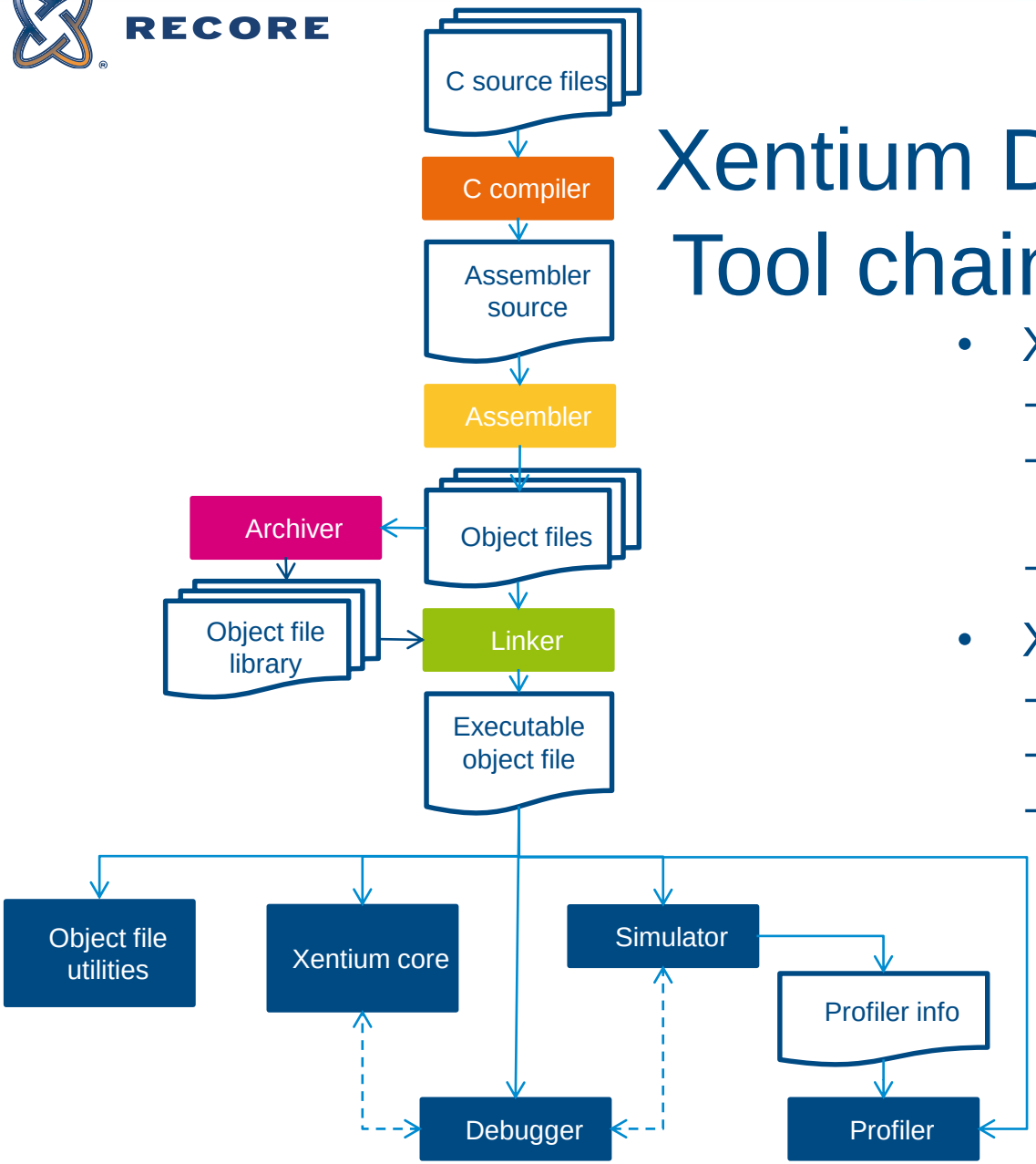


CMOS	GMAC/s	Clock
65 nm 90 nm	1.6 GMAC/s 0.88 GMAC/s	400 MHz 220 MHz

Xentium - datapath parallel execution units

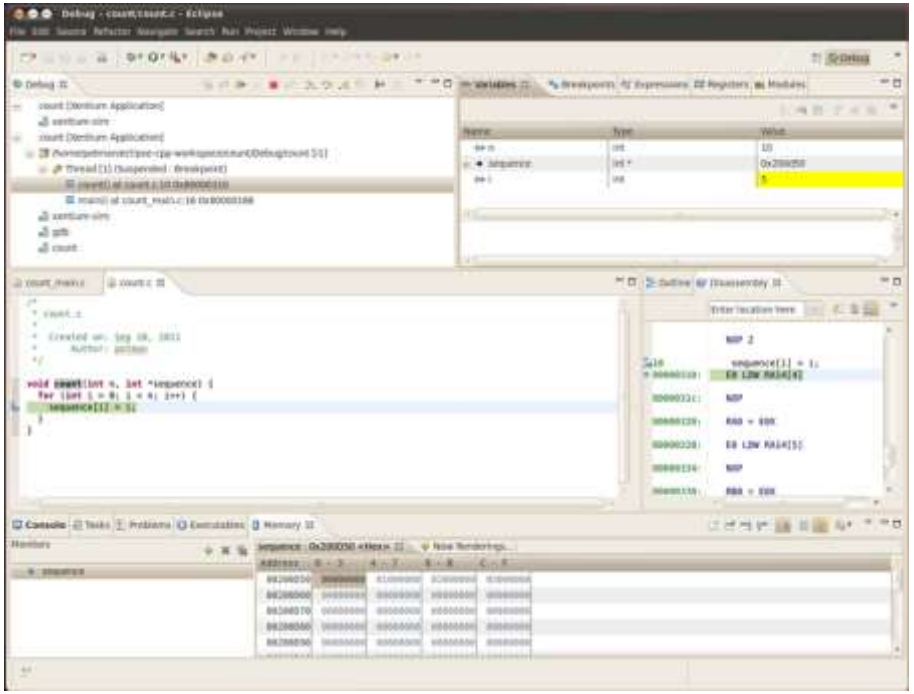


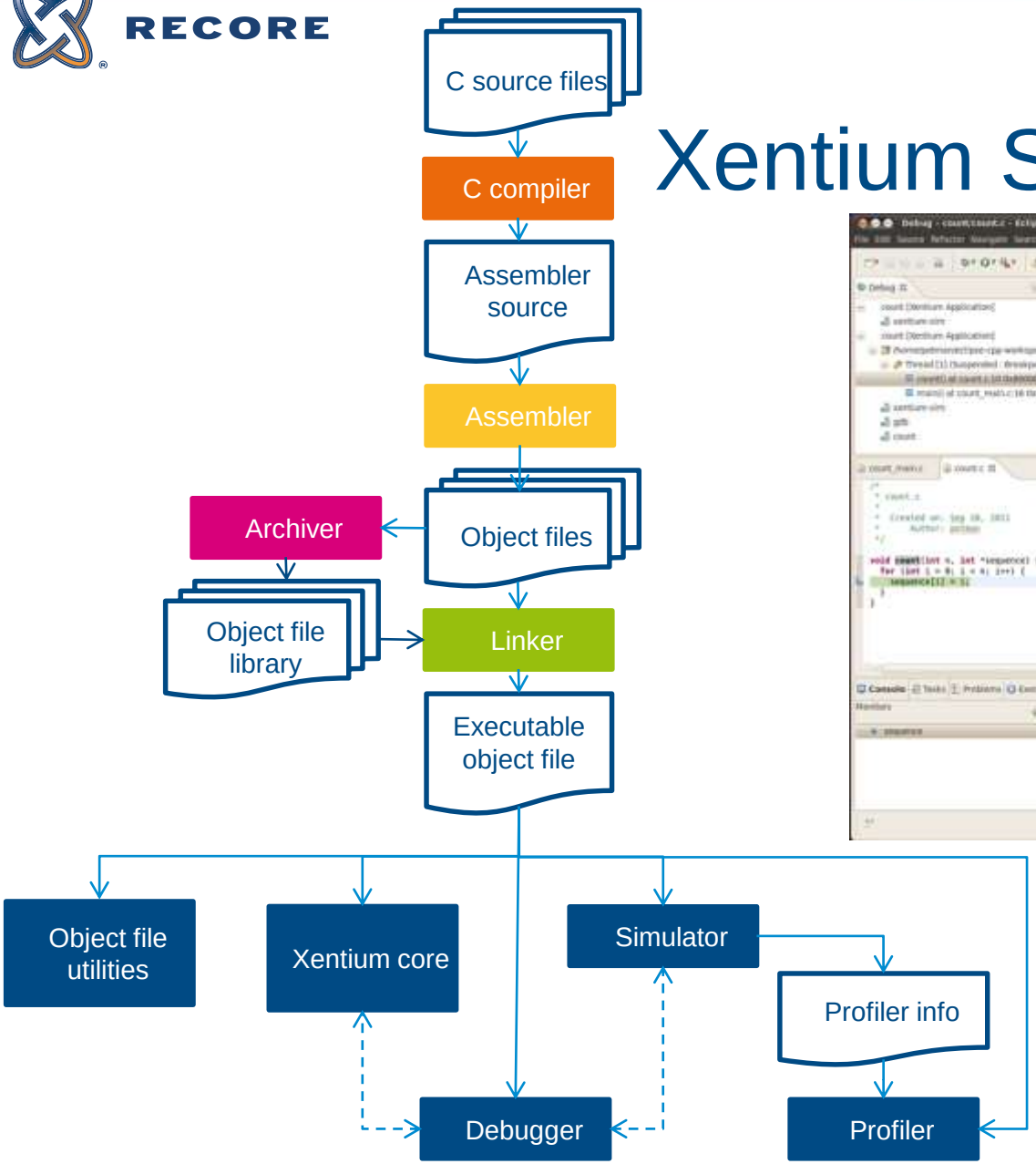
Xentium DSP Tool chain



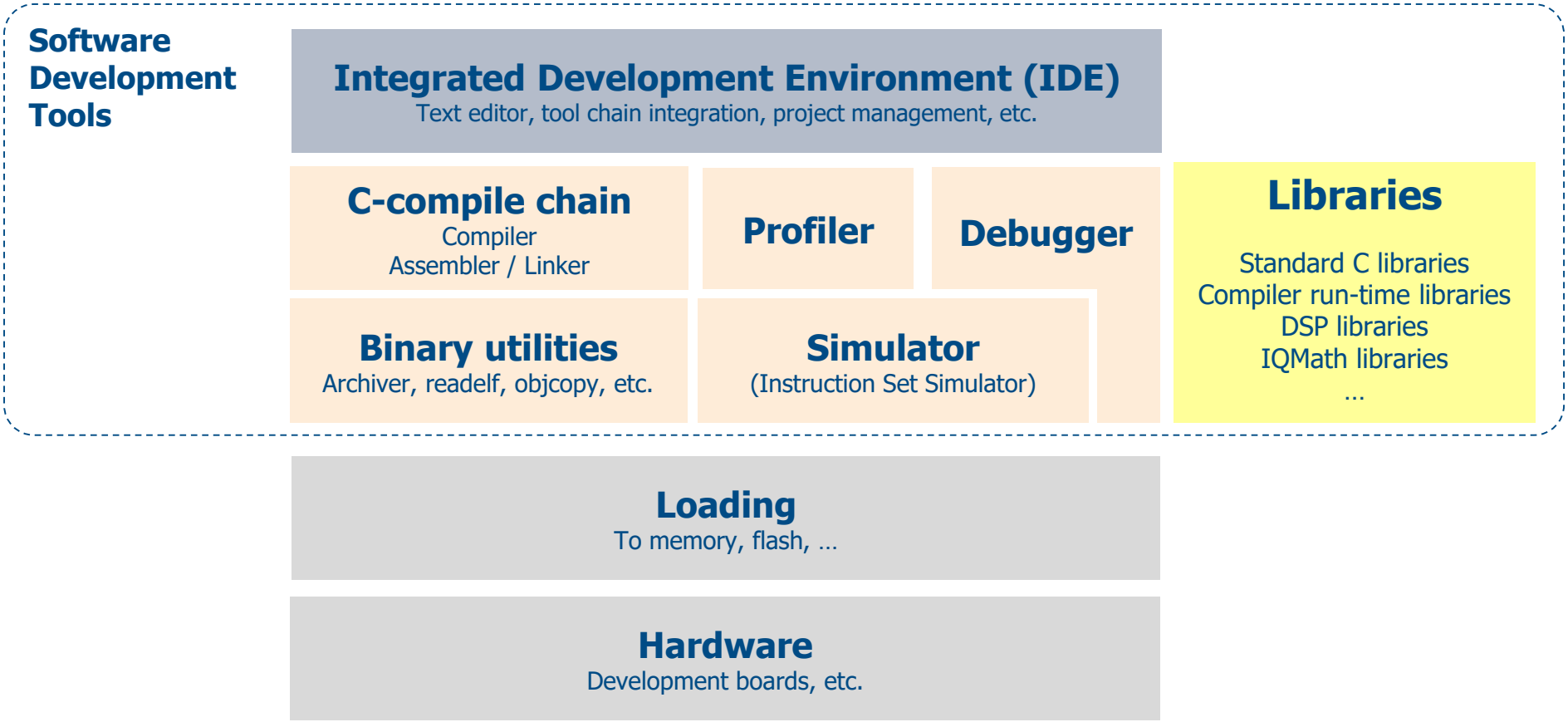
- Xentium C compiler
  - ANSI/ISO-standard C
  - Built-in functions for Xentium specific operations
  - Mix C and assembly functions calls
- Xentium assembler
  - Clean and readable
  - Extensive built-in preprocessor
  - Standard assembler directives
- Compile, assemble & link a program in a single step
- Xentium ISS
  - Trace program execution
  - Interactive debugging
  - Program profiling

Xentium SDE



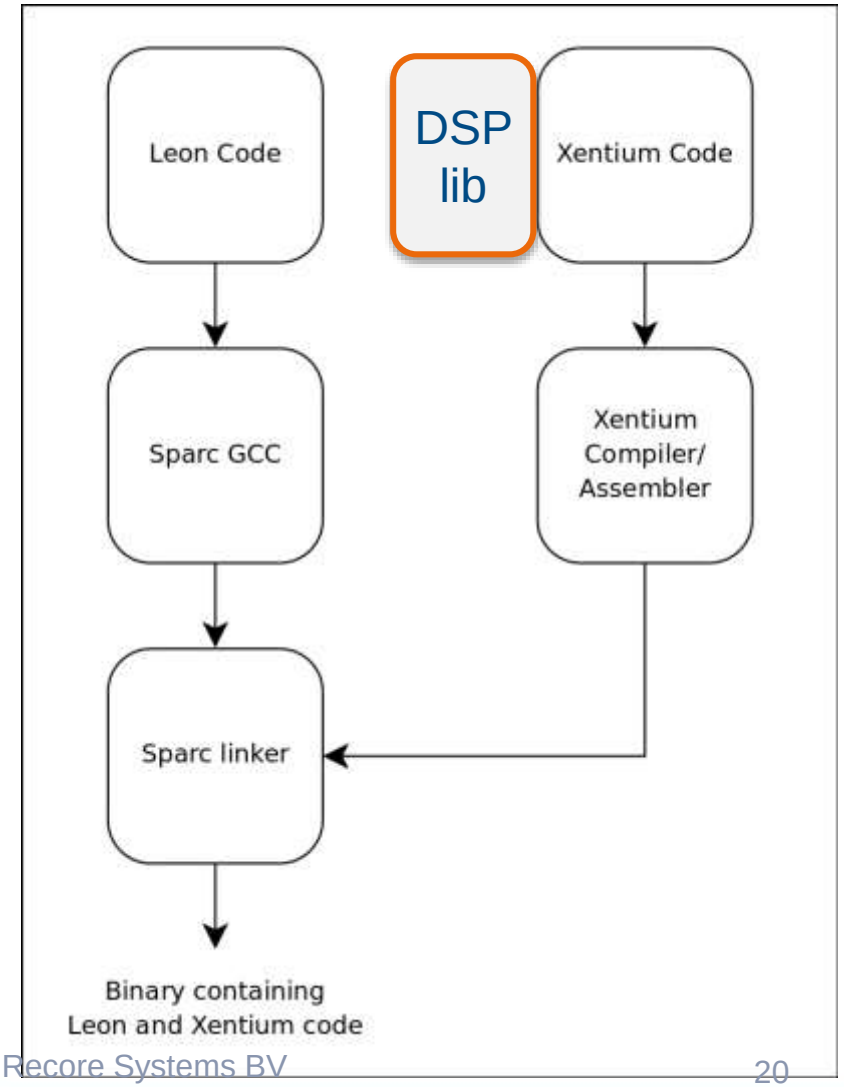


Xentium Studio software development tools



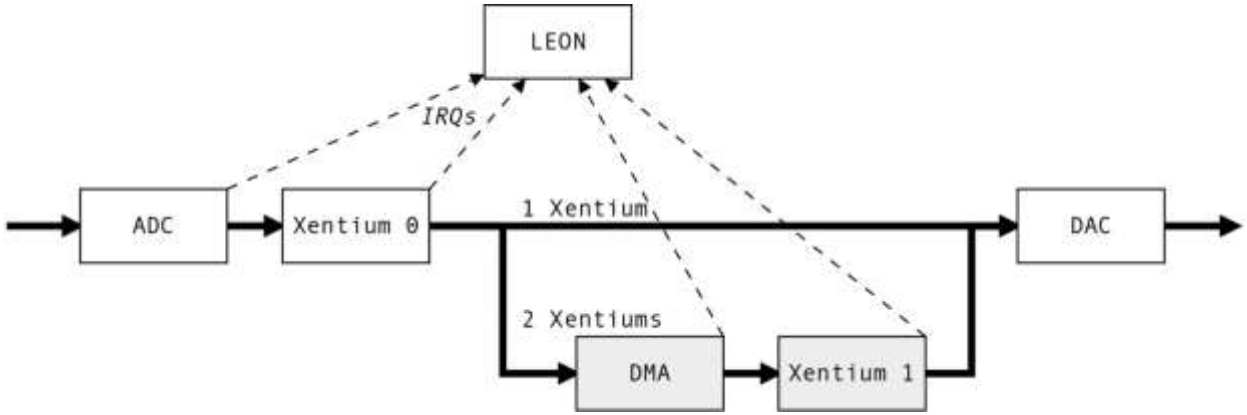
MPPB/SSDP software development

- Writing code
  - Leon
    - C or SPARC assembly
  - Xentium
    - C or Xentium assembly / DSP library
- Compiling code
  - Leon
    - sparc-elf-gcc
  - Xentium
    - Xentium C-Compiler or Xentium assembler
- Linking code
  - Xentium binaries are linked in the Leon binary



MPPB/SSDP Programming

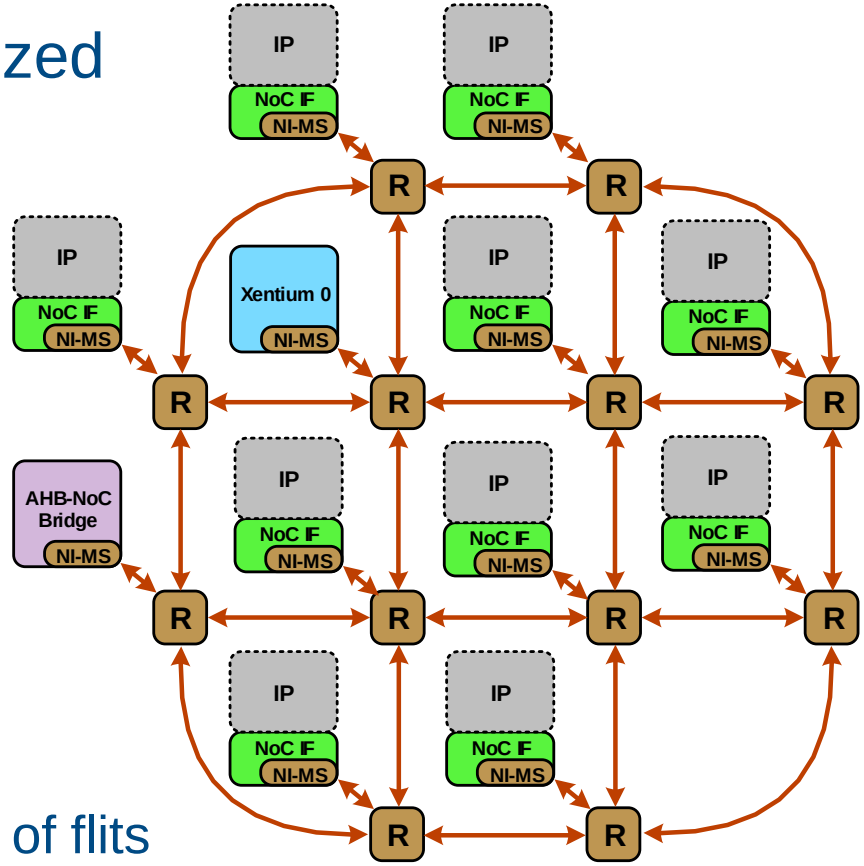
- Xentium applications
  - DSP Kernel accelerators
  - Seen as tasks, started from the LEON host processor



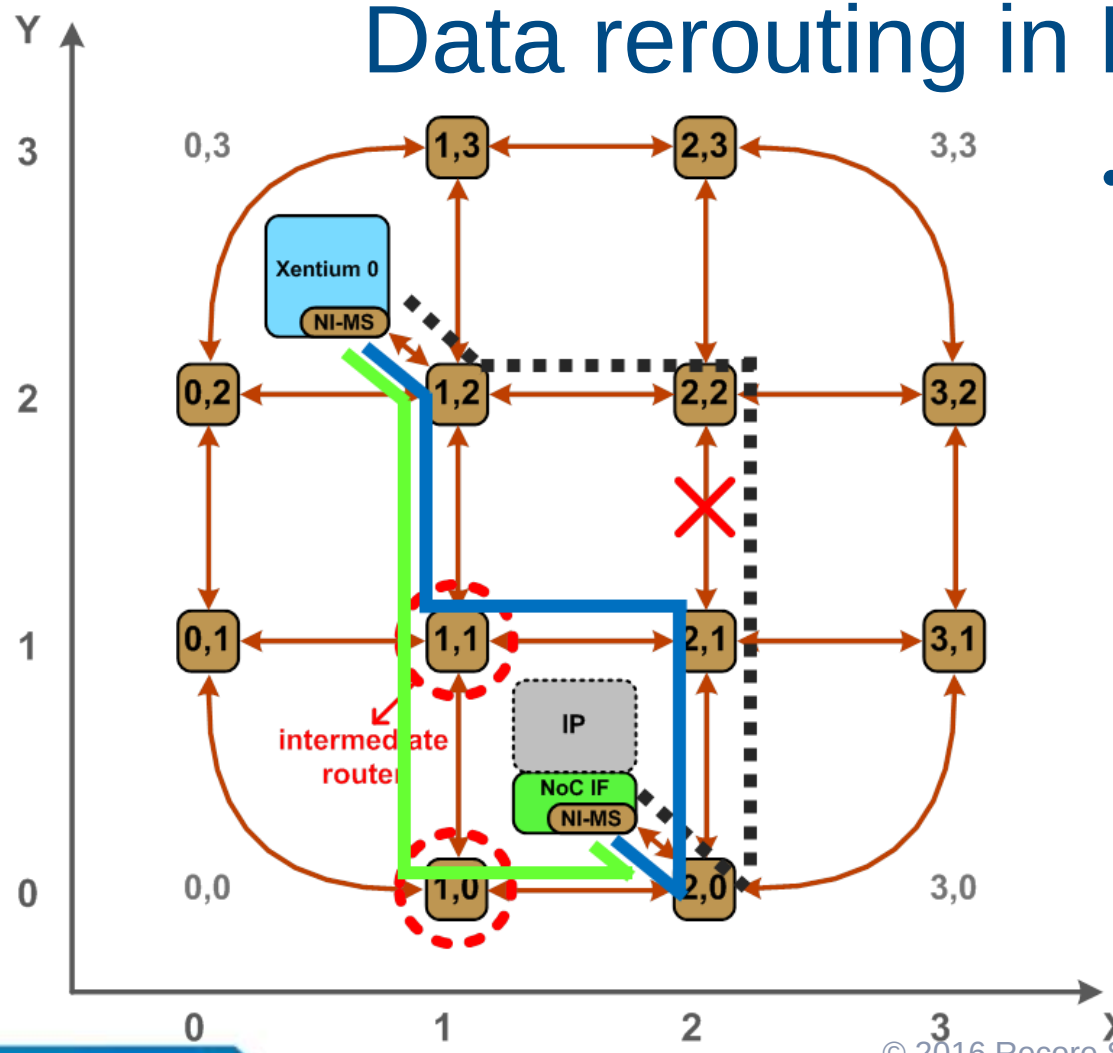
- Xentium API
  - Implements synchronization with Xentiums
    - Communication (interrupts/mailboxes)
    - Task queuing
  - Uses DMA to copy data to/from the Xentiums

Network-on-Chip

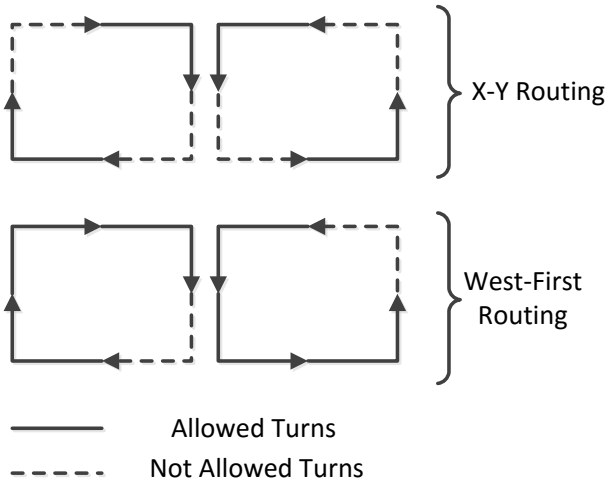
- 32-bit packet-switched 2D Mesh network
- XY-routing, deadlock free
- 5-port routers featuring 4 prioritized services (virtual channels)
- Quality of Service provided by the services
- Reliability
  - Adaptive XY-routing to provide data rerouting in the NoC
  - Flit-level flow control
  - Enable the insertion of EDAC on data links to increase robustness of flits



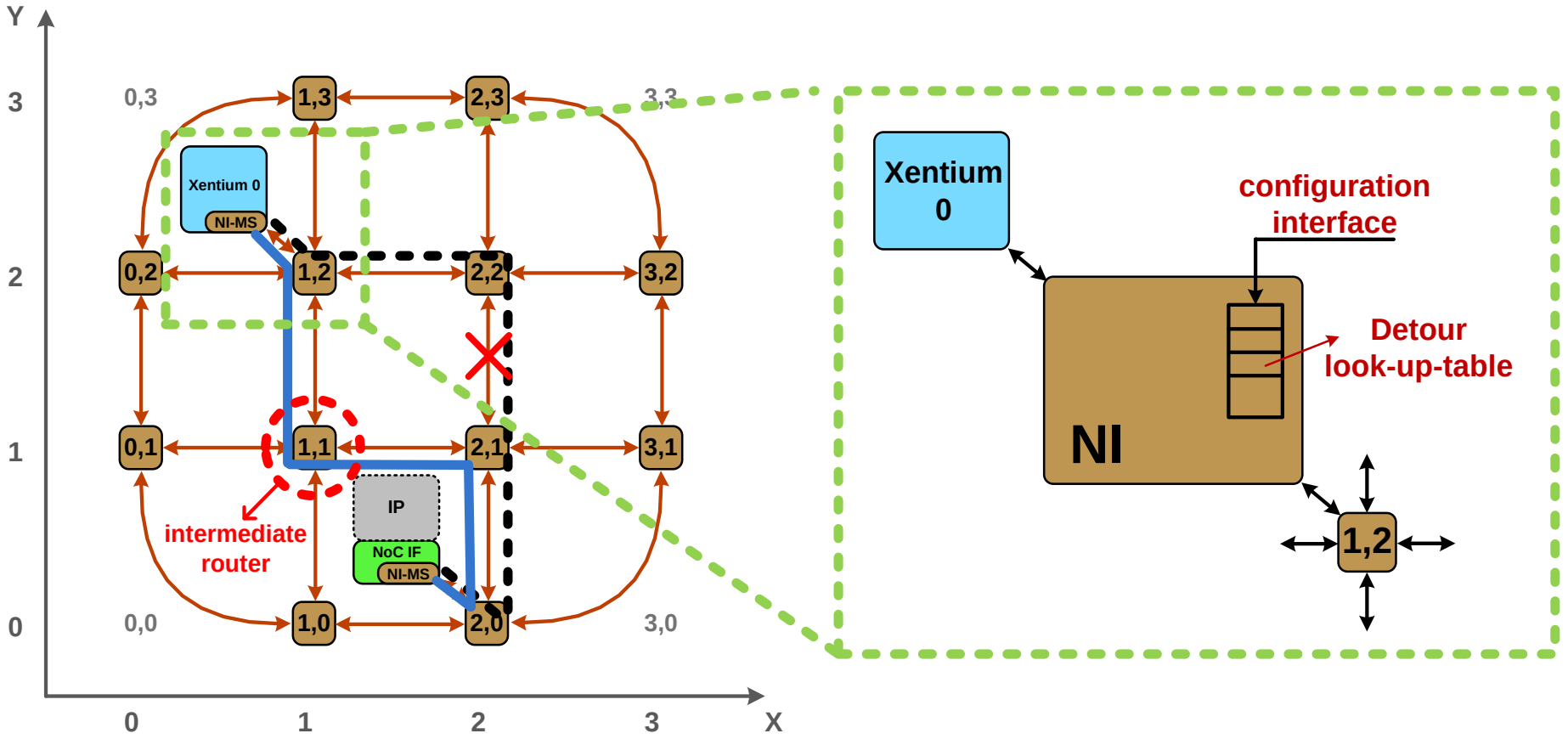
Adaptive XY-routing
Data rerouting in NoC (1/2)



- Xentium 0 → IP
  - X-Y routing
  - detour from (1, 1)
  - detour from (1, 0)



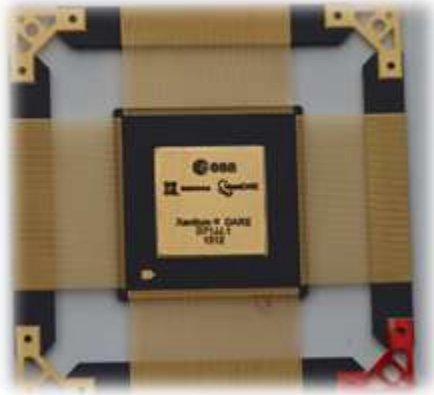
Adaptive XY-routing
Data rerouting in NoC (2/2)



Summarizing

- Recore IP used in the **first European multi-core DSP chip for space**
  - Validated in radiation-hard CMOS (XentiumDARE)
  - Integrated in Scalable Sensor Data Processor (Thales Alenia Space)

- European Space roadmap targets development of a **new powerful many-core floating point DSP** for space applications



Next step?
Heterogeneous many-core SoC

- Xentium VLIW DSP core in rad.-hard 65nm CMOS
  - Clock: 300 MHz
  - Performance: 1.2 GFLOPs/s
  - NoC per link: 9.6 Gbit/s
  - Area: 1.1 mm^2
    - 75% gates utilization
    - Including NoC interface
- Many-core SoC example
  - 48 Xentium processing tiles
  - 16 memory tiles
  - 60 NoC routers
    - 8×8 mesh

→60 Giga MACs/s
→60 GFLOPs/s