Approval Process of an ESCC Qualified ASIC Supply Chain based on a Mixed-Signal IP Library

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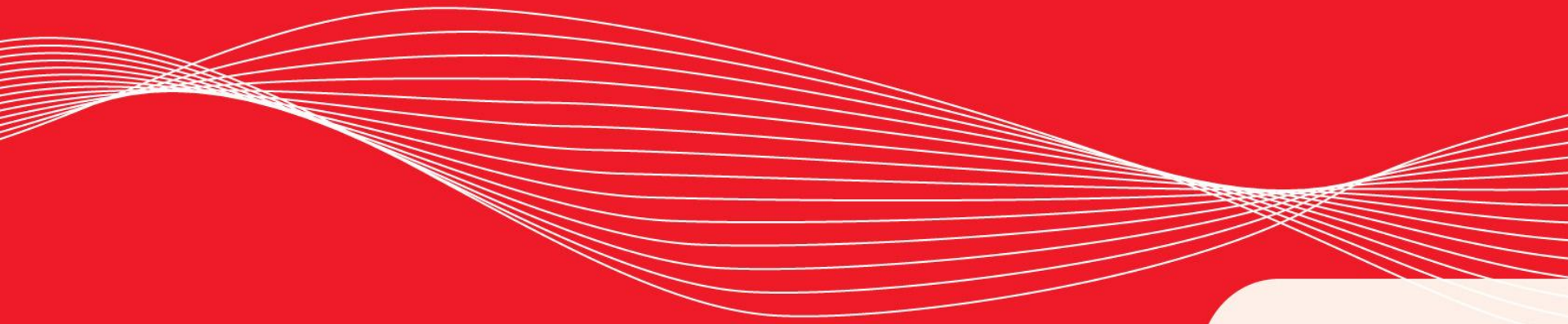


AMICSA: 15.06.2016

Overview

- Motivation
- Introduction of the ASIC Supply Chain
- HARD Library Elements IP List
- Evaluation Test Flow
  - Preliminary SEE and TID Test Results
- Outlook

Motivation

- *Capability Approval* for an ASIC Supply Chain under the ESCC system
  - Reduction on development time
  - Lower Risk and Costs
  - Trade-off between:
    - Full custom design with full qualification
    - Semi optimized Product based on available standard ICs

- First introduction of this ASIC Supply Chain on the AMICSA 2014:
  - 180 nm CMOS Mixed-Signal Radiation Hard Library as base for a full ASIC supply chain

ASIC Supply Chain

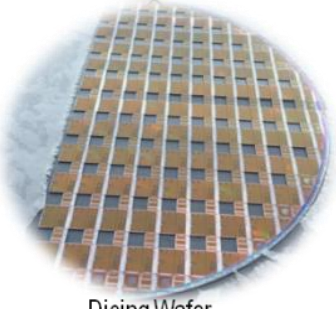
Design &Layout with Hard Lib

- IMST
- Customer optional digital

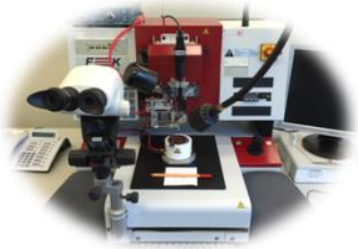
Wafer Manufacturer

- XFAB

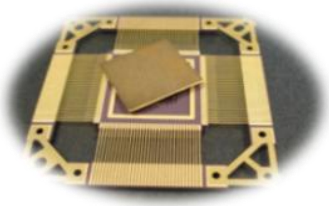
Wafer Test



Dicing Wafer



Die assembly



ASIC Specification

- IMST
- Customer

Package Test & Screening

Lead forming

- optional

Qualified ASIC

ASIC Supply Chain

- I/O Lib
- IP Library for analog and mixed-signal IPs
  - Cover a wide range of application
  - Contains .lef, .lib, VHDL entity and VHDL models
    - For P&R tools
    - Available for customers without schematic and layout view
- Script to implement TMR structures and scan chains
  - Will be used by IMST for customer or IMST designed netlists
- CQFP Package family is available for:
  - Pin count 32 up to 256
  - Die size 2.2 mm^2 up to 100 mm^2

IP Library Elements

- Technology
  - XFABs XH018 has been validated to be suitable for RadHard designs
  - Support for customers with low wafer numbers
- Radiation Hardness specification:
  - Single event latch-up free up to LET of 80 MeV/mg/cm² and 125°C, according to ESCC 25100
  - SEU/SET test, according to ESCC 25100
  - TID test for total dose > 300krads (Si) according to ESCC 22900 Specification

HARD Library IP blocks

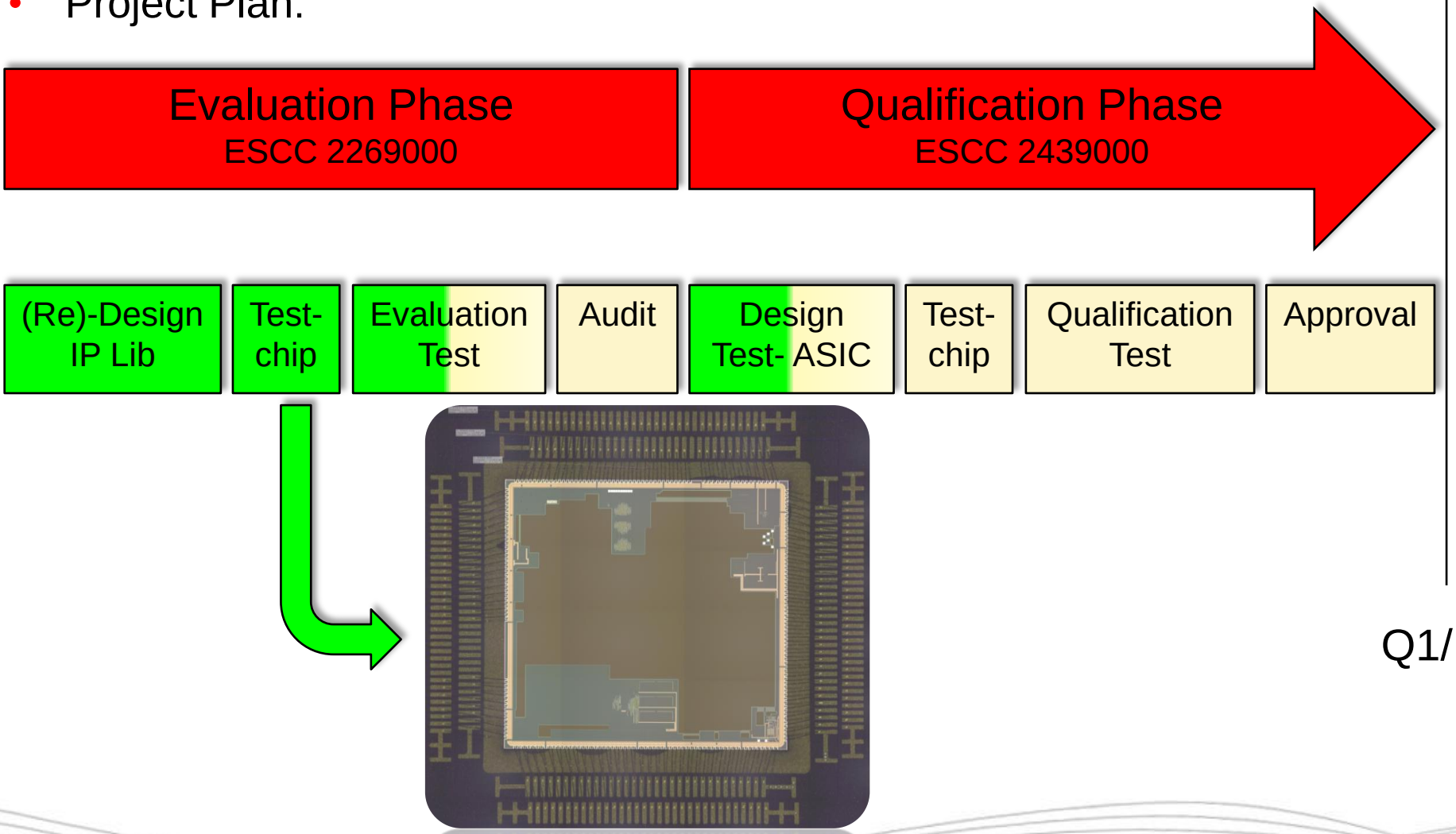
IP Block	Main Characteristics
4-Wire SPI Interface	1.8V, extendible register bank with 8 register and 16 bit, each. Refresh logic for SEE mitigation implemented
I/O Cells	3.3V & 5.0V digital + Analog I/O, TMR In/Out
LVDS Driver	1.8V, Fmax=622 MHz
LVDS Receiver	1.8V and 3.3V, Fmax=622 MHz
Reconfigurable Multifunctional Operational Amplifier	•Inverting OpAmp with variable gain: -10 dB … +30 dB; 1dB step size •Non inverting OpAmp with variable gain: -10 dB … +30 dB; 1dB step size •LPF; 3 different cut off frequencies •I/U Converter with different input ranges •Schmitt Trigger •Voltage buffer •Open Loop configuration
Bandgaps	1.8V & 3.3V trimable
Reference Bias Generators	1.8V & 3.3V with PtoPR and constant currents & adjustable voltage references
Temperature sensor	1.8V, temperature range from -40°C…+150°C
POR Generator	POR delay: 5µs
LDO	Input voltage: 3.3V Output Voltage: 1.8V with adjustable short protection, 150mA I max

HARD Library IP blocks

IP Block	Main Characteristics
Level shifter High-Low	input signals with 0V…1.8V output signals with -5V…-3.2V
Level shifter Low- High	input signals with -5V…-3.2V output signals with 0V…1.8V
Digital Level shifter High-Low	3.3V-1.8V
Digital Level shifter Low- High	1.8V - 3.3V
16bit MUX	Max. signal frequency: 800 MHz
12 bit ADC	charge-scaling SAR ADC fast mode: 200 KS/s
SRAM	2k x 32 bit SP-SRAM module Clock frequency: 50 MHz.
12 bit DAC	segmented current steering DAC
Trim Cell	64 bit OTP
Serializer / Deserializer	Data Rates: 600 Mbps with a reference clock Power: <500 mW
Clock PLL	16 bit 2nd order SDM fractional-N divider period jitter: 50ps (PK-PK)
DCXO	Supports 5 MHz … 50 MHz crystals
VCO with frequency divider bank	VCO frequency from 80 MHz – 600 MHz Divider bank ration from 1 to 128
CQFP package family	•Pin count: 256, 208, 132, 64 and 32 •100 Ω differential ports for LVDS interfaces •Die size from 2.2 mm^2 up to 100 mm^2

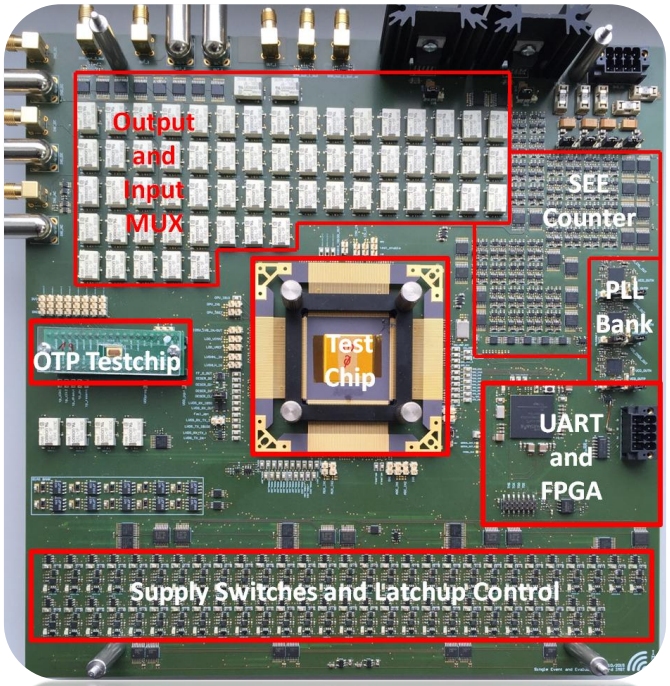
Evaluation Test Programme

- Project Plan:



Evaluation Test Programme

- Inspection
  - Dimensions
  - Weight
  - Electrical Measurement
  - External Visual Inspections
  - Particle Impact Noise Detection (PIND)
  - Radiographic Inspection
  - Hermeticitiy
  - Marking and Serialisation
- Initial Electrical measurements according to Detailed Spec
- Destructive Tests
  - Step-Stress-Test
  - Radiation Tests
  - Construction Analysis
  - Package Tests
  - ESD Test
- Endurance Tests
  - Accelerated Electrical Endurance
    - 1000 hrs @ tbd °C
    - 500 hrs @ tbd °C
    - 168 hrs @ tbd °C



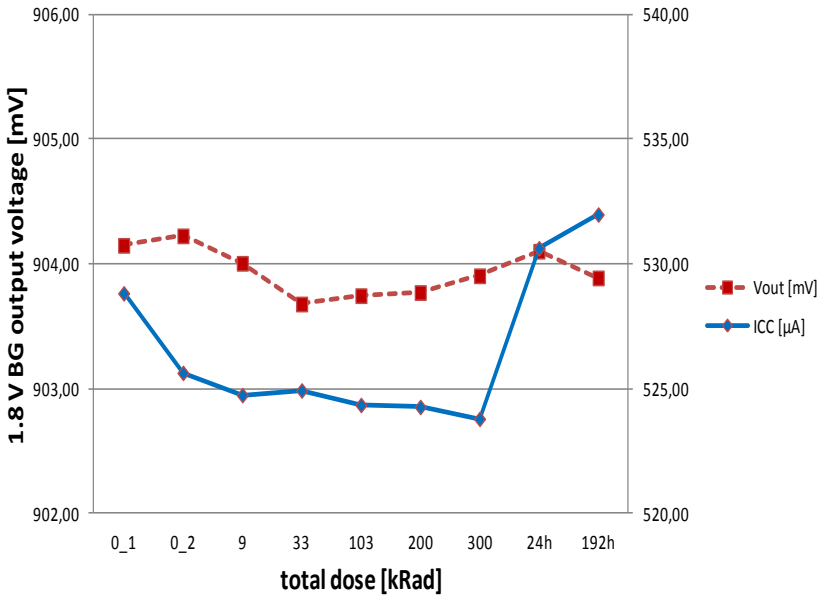
TID Test

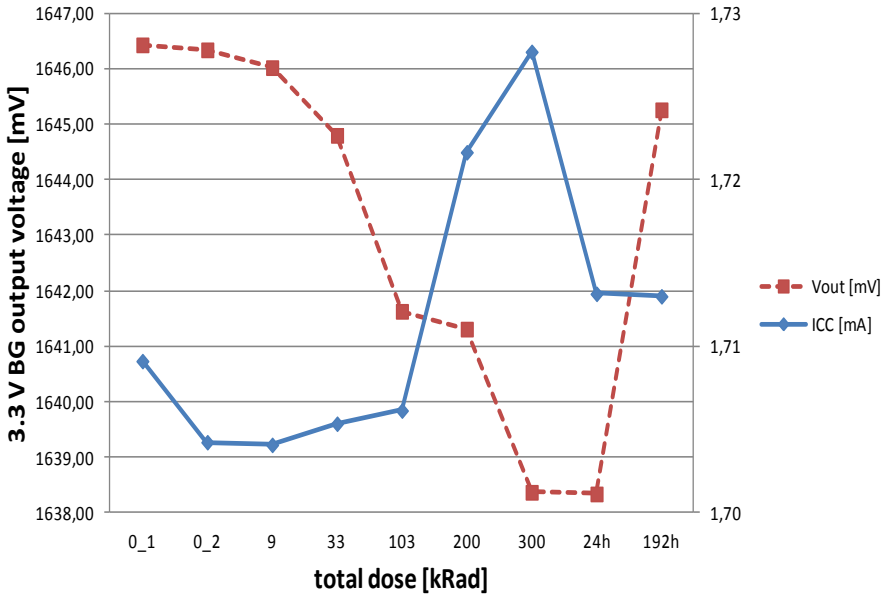
- Facility of ESTEC:
  - Co60 Gamma ray source
- Radiation Test Plan:

Total Dose [krad] (Si)	Dose Rate [krad/hrs] (Si)
0_1	0
0_2	0
9	0.275
33	0.275
104	0.275
200	3.3
300	3.3
24h annealing	0
192 h annealing	0

Preliminary TID Test results

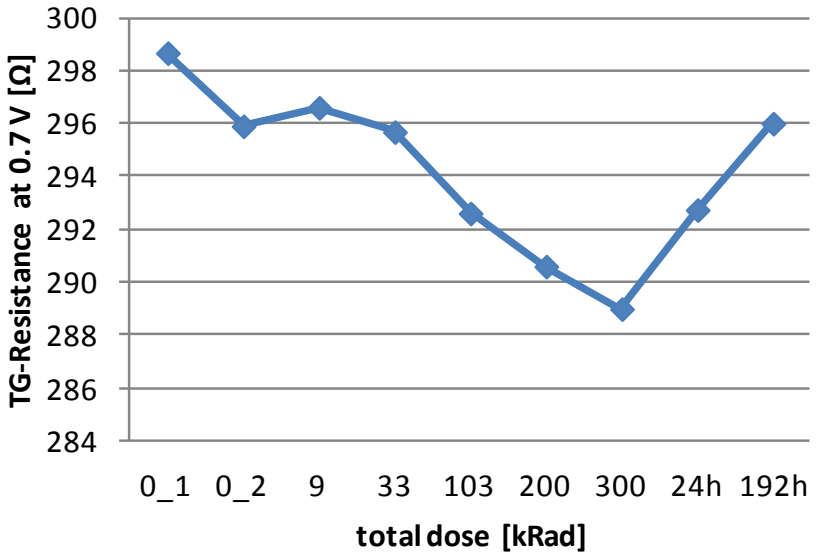
- 1.8 V Bandgap vs. 3.3 V Bandgap
  - 1.8 V Transistors with thinner gate oxide have less TID effects compared to the 3.3 V Transistors





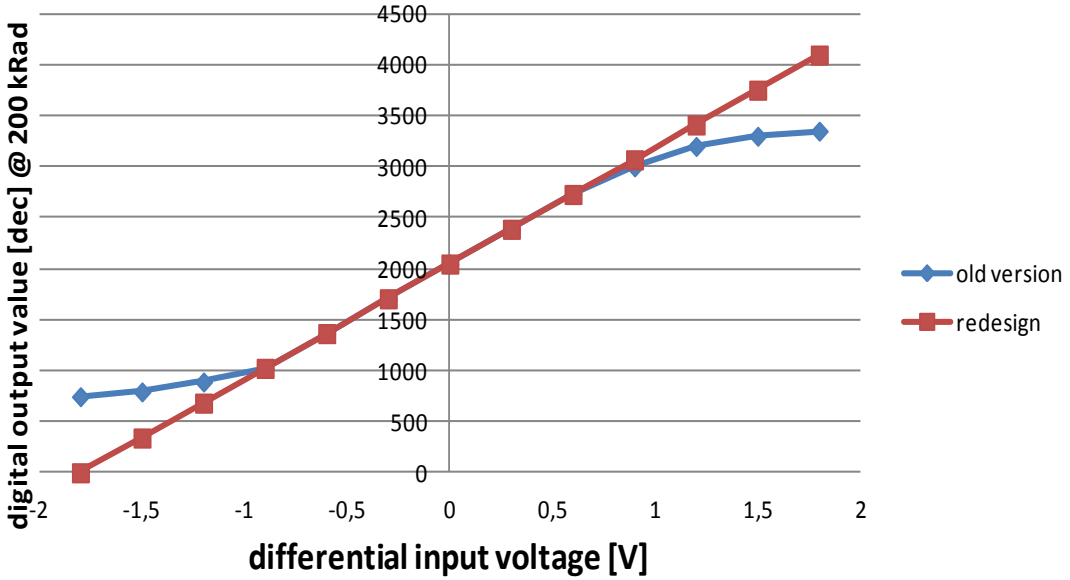
Preliminary TID Test results

- Resistance of a Transmission Gate with 3.3 V Transistors
  - On-resistance at 700 mV Bias
  - Resistance drops versus higher total dose and returns to initial value after annealing



Preliminary TID Test results

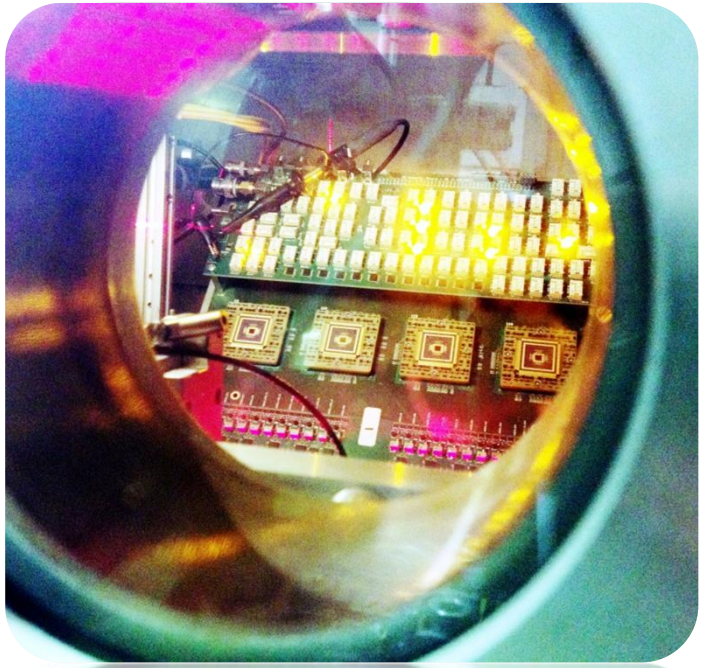
- Transfer function of the ADC @ 200 kRad: 1st Design vs. Re-design
  - At high input voltages, the stored energy is leaking during conversion
  - Even for 1.8 V transistors low leakage is detected
    - Effect on Low Power Circuits
  - Effect can be eliminated by proper switch designs



SEE Test

- SEE Test for this test campaign need to be done
  - Results from previous project is available
- Facility Cyclon Resource Center L-l-N
  - CYCLONE110
- Test Conditions:

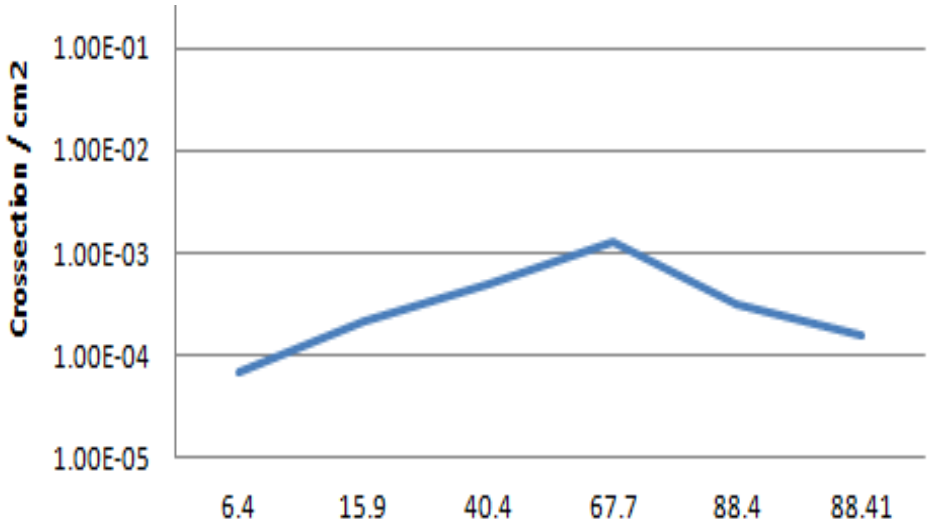
Test	Ion M/Q=5	Energ. (MeV)	∢	Range (µm)	LET(MeV/mg/cm^2)	Temp [°C]
1	^{20} Ne $^{4+}$	78	0	45	6.4	20
2	^{40} Ar $^{8+}$	151	0	40	15.9	20
3	^{84} Kr $^{17+}$	305	0	39	40.4	20
4	^{124} Xe $^{25+}$	420	0	37	67.7	20
5	^{125} Xe $^{25+}$	420	40	28.34	88.4	20
6	^{125} Xe $^{25+}$	420	40	28.34	88.4	125



SEE Test Results

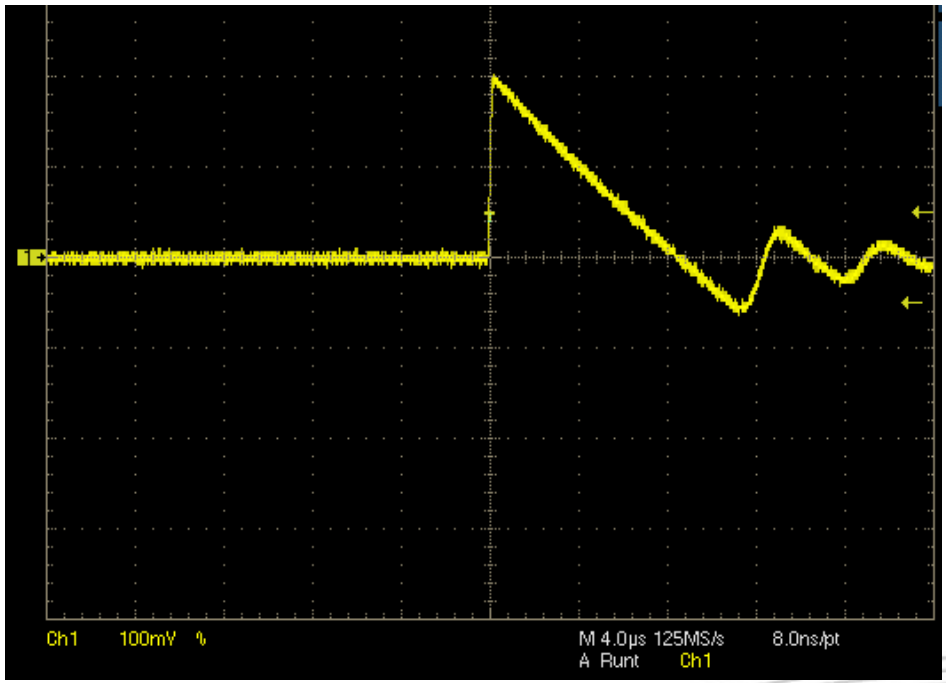
- Representative Results shown for the 1.8 V Bandgap
  - Comparators are counting SETs with a magnitude of ±50 mV
  - SEU detected in SPI controller input pad
    - Enable bit and other control bits are randomly changed
    - Consequently counter values are not valid for LETs > 67.7 MeV
    - Problem has been fixed in current design, but need to be validated

LET (MeV/mg/cm^2)	hits
6.4	9
15.9	17
40.4	61
67.7	76
88.4	31
88.4 @ 125 °C	10



SEE Test Results

- SETs have been monitored by an oscilloscope, too
- Magnitude and wave form varies for different LETs
- Representative plot for Argon Ion resulting in a 200 mV pulse
- Redesign has been improved for less SET sensitivity, but needs to be validated



Outlook

- Finishing Evaluation Phase with Audit
- Finishing Qualification Phase
  - Capability Approval in Q1/2017
- Become an ASIC fabless manufacturer following ESCC rules
- Providing a space qualified technology & supply chain for Mixed-Signal ASICs

Acknowledgement

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DLR Qualitäts- und Produktsicherung

TESAT SPACECOM is project partner

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