TESAT SPACECOM

PIONEERING WITH PASSION

# Using a Standard Commercial Process for Full Custom Rad Hard Mixed-Signal Design

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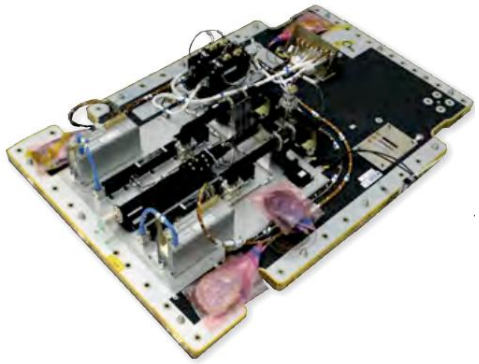
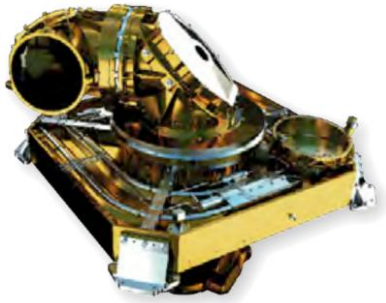
# Overview

- Motivation for and special requirements for AMS-ASIC-Design at Tesat
- Choices and Decisions
- Process Selection
- Design Flow
- Hardening Approach
- Example
- Acknowledgements

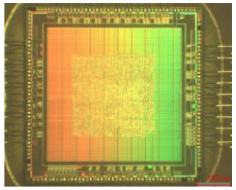
# Motivation and Requirements


- Tesat is „just an equipment supplier“
- Improvement of equipment needs higher integration of functionality
- Effort to be concentated to main competence
- ASIC design concentrated on own applications



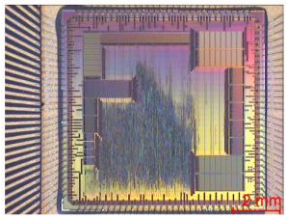


# History - where Tesat comes from

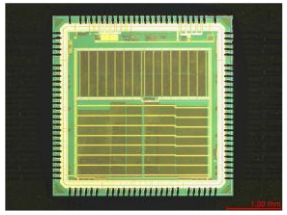


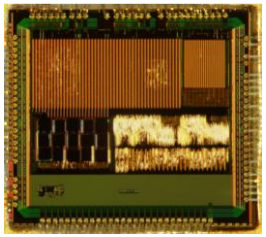
- Pure digital ASIC/FPGA design using space qualified processes
  - AT4, Atmel 0.5 µ CMOS 5V digital

- First mixed signal designs using analog IPs and radiation hardened digital library (DARE), qualified
  - Knut, UMC 180 nm, CMOS, 3.3V, Mixed Signal



- First mixed signal test designs using own analog circuits and non-hardened library elements, hardened on design level , tlfa1, Lfoundry 180 nm
- Mixed signal ASIC design approach using analog Ips
  - txfa1, XFab 180 nm
  - lama, XFab 180 nm





# Choices and Decisions

„Make“

„Buy“

Analog-on-Top

Digital-on-Top

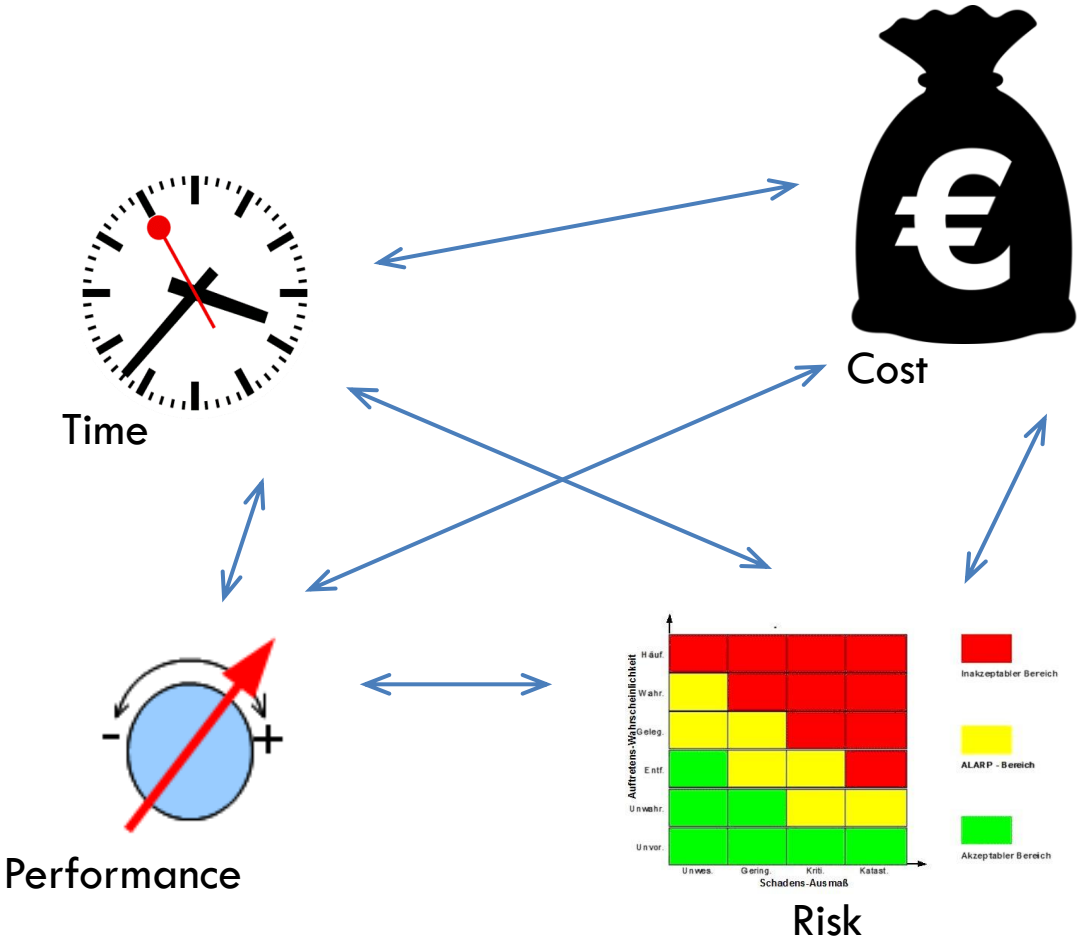
„commercial process“

„space qualified process“

Hardening by Process / Device / Design ?

0.5µm, 0.35µm, 250nm, … 90nm, 60nm

# Choices and Decisions - Criteria

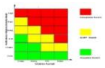
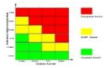


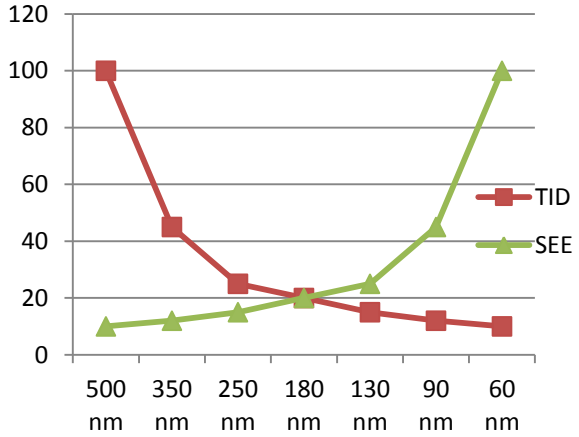
# Choices & Decisions

# Make or Buy?

| | Pro | Contra |
|---|---|---|
| Make | » Independent<br>» Easy adaption to modified requirements<br>» Own experience grows<br>» Detailed information on implementation | » Need for qualified personel and tools<br>» Increased qualification effort<br>» Increased procurement effort |
| Buy | » No internal effort in tools and qualified manpower<br>» Experience from supplier can be used<br>» Existing designs might be reused<br>» Access to suppliers technologies | » Worse communication than make<br>» Worse reuse than make<br>» Dependency on supplier<br>» No internal details known |

# Process Selection

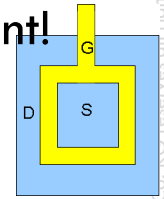
- Select node that most convinient with respect to
  - TID  
  - SEE
  - Cost 
  - Voltages 
  - Toolset 
- Select process that supports MPWs 
- Select process that supports small quantities 
- Select process with good foundry support 



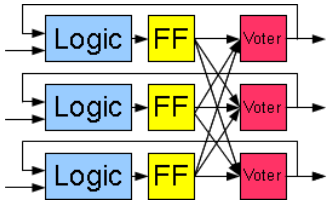
# Hardening Approach

» On process level → much too expensive

» On primitive device level → results in expensive Library development!



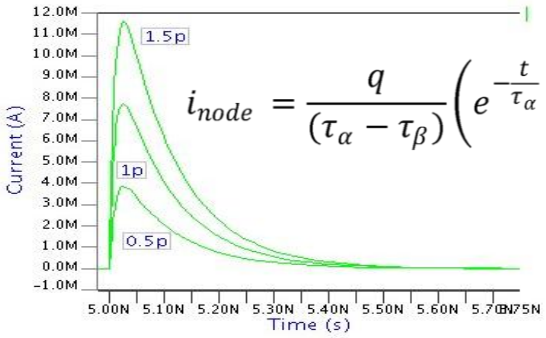

» On design level / system level → „less optimal“ than on device level
„waste“ of silicon area and power




» Hardening on design level provides solution with minimum investment and easiest transfer to other technologies!

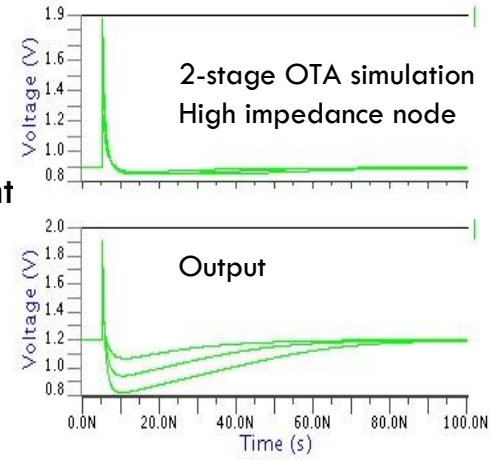
# Hardening Approach

- Digital Section:
  - Check library primitives by testing for radiation hardness
  - Select only suitable ones and apply hardening on design level
  - ➔ Tesat implemented full TMR by automated netlist modification after ordinary Synthesis




$$i_{node} = \frac{q}{(\tau_\alpha - \tau_\beta)}\left(e^{-\frac{t}{\tau_\alpha}} - e^{-\frac{t}{\tau_\beta}}\right)$$

- Analog Section:
  - Check primitives by testing for radiation hardness
  - Select only suitalble ones and take degradation into account
  - Perform SEE-simulation on sensitive nodes
    - by SEE-Pulse simulation and optimize circuit parameters



# Analog or digital „on-top“?

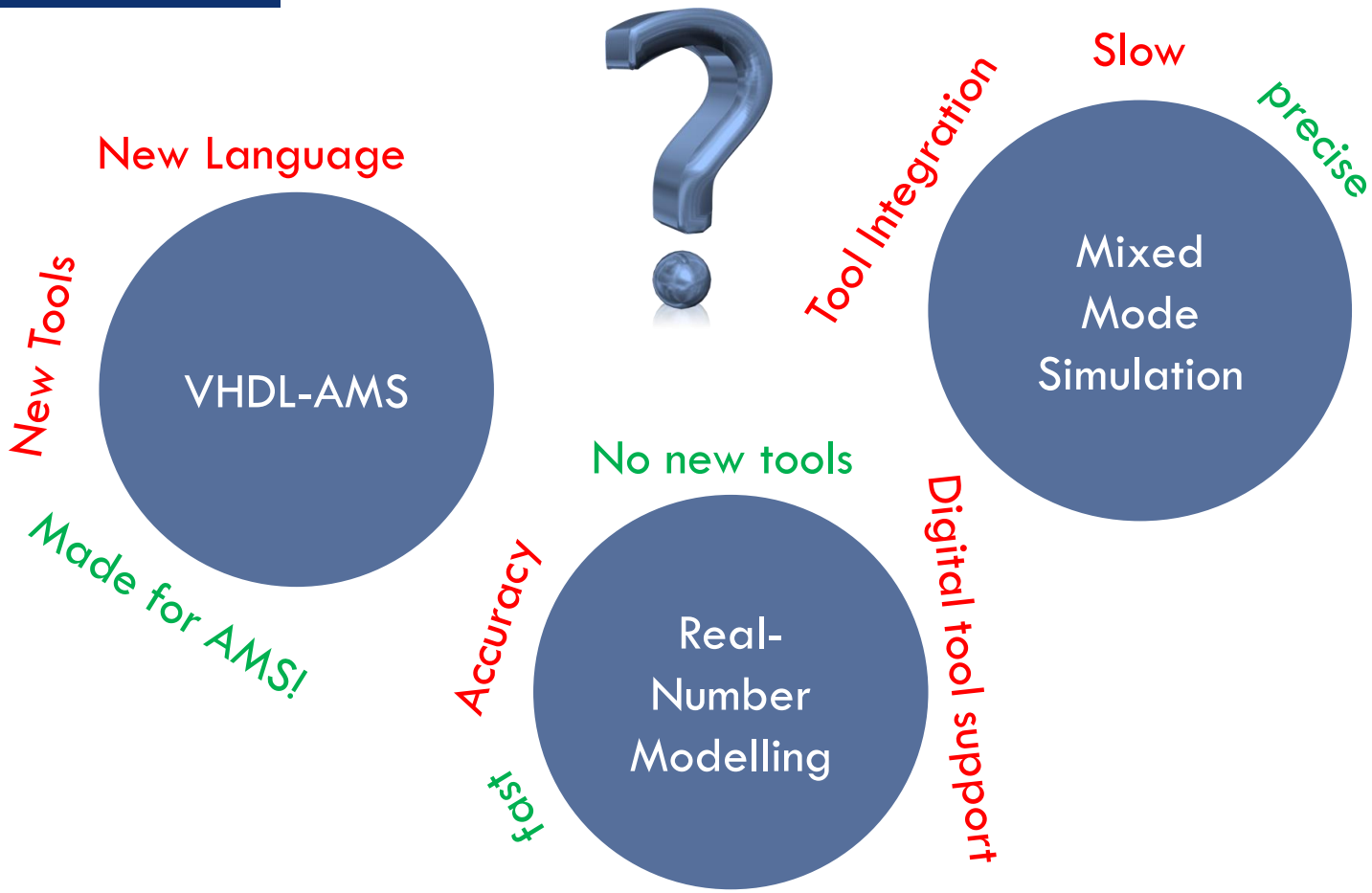
| | Pro | Contra |
|---|---|---|
| Analog on top | » well known by analog designers<br>» adapted to designs with rather small digital part and<br>» Easy | » High effort and lots of manual work |
| Digital on top | » Good tooling support for P&R<br>» Easy backannotation from external pins | » Integration of analog blocks not state of the art<br>» Integration of analog models into simulation and synthesis not state of the art<br>» Requires additional effort for integration of analog functions into digital design flow<br>» Worse support by tools and suppliers |

# Analog or digital „on-top“?

- Hot topics for „digital-on-top“:
  - What should top-netlist contain?
    - How about Power supplies, not usual in digital netlists.
  - How to pass analog signals through synthesis
    - How to model analog signals for simulation
  - How to manage wire width for analog signals during P&R?

  - How to characterize analog cells efficiently for digital design flow

# Modelling Decision

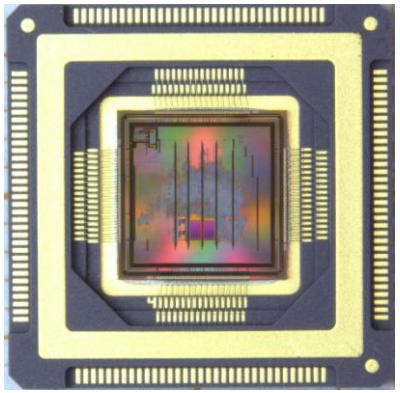


# Example

» Luca, TM/TC device for LCamp application, providing Bias point regulation for RF-chain

» Technology: Xfab XH180
» Die Size: 6x6 mm²
» Gate Count: 500 kGates incl. full-TMR
» Clock domains: 1x 16 MHz
» Analog Functions: DAC, ADC, analog regulation, Power Supply
» Supply ranges: -5 V … +8 V

» Radiation Hardness issues solved: SEU-hardness improved by provision of TMR-IO-Buffer



# Actual Decisions

- Make, not buy
- Commercial, not space qualified
- Digital, not analog on top
- Real number modelling and mixed-mode simulation,  not AMS
- Hardening on design and system level
- IP reuse, not copy & paste
- Accept deficiencies, don‘t try to change things you cannot change

# What is missing?

- Helpful Design rules for analog / mixed-signal Design
- ECSS-Q-ST-60-02 seems not to really cover development of devices using commercial technologies
- Standard Toolset used for mixed-Signal Design for Analog-on-Top and/or Digital-on-Top design approach

# Acknowledgements

» I want to thank my coauthors for their contribution to that paper and much more for all the effort they and my whole team take to make mixed signal ASIC designs as shown before real

» I want to thank ESA for support during the last mixed signal development in frame of the ARTES 5.2 „New Lcamp Technologies“ project ESTEC contract. no. 4000111633/14/NL/EM)

» I want to thank the audience for the attention

# Any Questions