Using a Standard Commercial Process for Full Custom Rad Hard Mixed-Signal Design

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Abstract

A mixed signal design flow aiming at rad hard, qualifiable designs on a commercial unhardened process is presented[1] This is done by analyzing deficiencies of the process concerning radiation and mitigation on system, circuit and concept level. Methods of analyzing possible weak points already in the design or prototype phase without irradiation are presented.

I. Introduction

Mixed-signal design allows integration of further external discrete components and hence continues the dividend of integration. However, implementation of a mixed-signal flow into an operating digital or analog design flow is not a straight forward task. In space applications in addition, radiation is always an issue and ways need to be found to mitigate its effect on the circuit. Libraries using modified specialized layouts exist to create rad hard designs for digital and analog functions [1]. Companies offer complete flows from design to supply chain using pre-designed building blocks to qualified devices using proprietary libraries[2][3].

Indeed, these solutions can be very efficient and minimize the risk as used library components might be working in several other designs. However, if application constraints the design to other requirements than implemented within the library cells, full custom solutions might be required to obtain the full benefit of mixed-signal. In addition to the limited availability of analog library cells for space application at the beginning of design, this has been one of the main reasons for the necessity of full custom design in our applications.

We start with a short introduction into our design flow followed by radiation hardening / awareness approaches on system, module and process level. Afterwards we give a short sample of a design currently in development. The paper is closed by a short outlook into supply chain implementation.

II. Design Flow

Before going mixed-signal, our design flow has been focused on digital designs only and several digital ASICs and FPGAs have been successfully created. One of the main requirements was that the new analog functionality should integrate into the digital flow while preserving it. In addition, our mixed-signal designs usually have a huge amount of digital cells integrated. Consequently, the decision has been to work with a digital-on-top flow. The major design reference is a VHDL-netlist and the final layout is done using a place-and-route tool and not the full custom analog layout tool. This way, the timing information between digital sub-cells like IO-cells, a possible digital core and memory macros is in control of the digital tools and not a full custom designer only. SDF-based verification on top-level remains possible. Furthermore, the exact shape of the digital core can be adjusted easily to fit into the remaining area after placement of the analog macros. Long parallel digital interconnection buses do not have to be drawn manually with a large effort, but are drawn by the place-and-route tool.

A. Working with analog IP

The digital on top flow with instantiated analog macros offers to work with analog IPs on the long term. As a matter of principle, the operation of implementing a memory macro can be similar to the implementation of an ADC for instance. It is instantiated within the digital netlist as a black box, with possible interface description or model and no dedicated analog tool chain would be required anymore.

Indeed, modeling of these analog IP is a challenge here. The straight forward way of using the spice netlist in a mixed signal design is costly on the on hand concerning license costs and simulation time. On the other hand, the spice netlist might not be available at all – for instance because it has not been developed or because the actual circuit hat to be kept secret from the user of the library. Hence, an alternative has to be found. This could be done by using AMS-models for instance, which would at least close the availability issue and possibly improve simulation time. However, if more abstract modeling is sufficient, a way might be to work with real number modeling. Indeed, here compatibility to tools like synthesis and mixed signal simulation need to be retained. Routing of analog signals through digital modules in mixed signal simulations can be prevented by the use of resolved real signals for instance.

A simple way of modeling is to keep the interfaces of mixed modules digital while working with real signals internally. This way, an ADC could be modeled for instance. However, this approach can be too abstract.

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B. Space dedicated standards for analog/mixed signal ASIC development

The ECSS standard for ASIC and FPGA development [6] fits best for digital designs and seems to be evolved on digital design bases. Lots of effort had to be spend to develop a design approach allowing e.g. concurrent engineering with layout and circuit design while still being conform to [6]. Furthermore, the while there are lots of guidelines / best practices concerning digital rad hard ASIC design, guidelines for analog designs are still evolving. An ECSS handbook is currently under development [5].

III. Radiation Hardening

The next question is how to obtain a qualifiable rad hard design. Here the approach has been to work with an available commercial process which is tolerant enough for TID and do mitigation for SEE on system and design level rather than modifying the process or its devices. Furthermore, no dedicated rad hard digital standard cell lib should be designed and radiation tolerance should be given at netlist level. This way flexibility to adapt to other processes is retained in principle.

A. Process evaluation

However, not all insufficiencies of the process can be taken care of at system or netlist level. This is why radiation behavior of the process needs to be observed during process choice. Individually checked devices have been white listed concerning total dose and SEE behavior. Our result has been that we can work with our technology applying the netlist mitigation techniques on digital cells. Further devices or macros which might be required have to be observed, in addition.

In our evaluated process, 3.3 Volts transistors and lower voltage devices could be used basically without total dose concerns. Significant drifts will occur at higher voltage devices. Consequently, they should be avoided where possible and should not be used in analog macros where the exact parameters are important.

On device level, no latch-up issues arose during single event testing.

B. Digital design

On the digital side we work with triple mode redundancy of memory and logic elements. This procedure keeps the devices clean from single events up to a certain threshold. However, as IO-cells might be a bottleneck in this case, we had to develop an own redundant IO cell to keep the complete path redundant. Possibly necessary macro cells have be treated with special care dependent on the application and their radiation behavior.

1) Mitigation on standard cells

Usually the standard cell registers will be sensitive to single event upsets. As no errors are allowed to remain within the operating design, the original state of a register has to be recovered. This can be done by developing dedicated redundant self recovering full custom standard cell registers. This might be the most efficient way concerning area and power consumption. However, it is expensive concerning the development effort and a process change would require new full custom cells. A cheaper way is to build redundancy using already available commercial standard cells. As cost efficiency has been one of the key parameters during our design decisions, this has been our way to go.

There are several ways of adding triple mode redundancy on netlist level. A straight forward way would be to instantiate the top level digital module three times and compare the results of the three instances. This way, the effort would be little more than three times the cells necessary in the un hardened design. However, the mitigation is limited as the designs would need to be synchronized at least after a hit. This procedure might not be possible. A periodic hit independent synchronization would enlarge the cross-section drastically.

Another way of adding redundancy is to compare the results after each register. This way synchronization is done at each clock cycle which minimizes the cross-section. However, this way of redundancy is expensive as comparison elements are necessary for each of the registers of the circuit. It is the closest to a full custom self-redundant register.

Redundancy at register level is implemented in our design. As a manual modification of the netlist would be error prone, the synthesized netlist is modified automatically. Margin has to be included in the timing of the not redundant netlist to retain a valid timing after redundancy insertion. Indeed, normally optimizations are not possible any more after insertion. Redundancy could be removed in this case.

2) IO-Cells

Early radiation test showed SEE sensitivity of standard IO cells available for our process. In addition, the redundancy approach done on register level is not possible on IO-Cell level at least for outputs. There has to be a position, where the triple-mode redundant signal is converted into a single signal.

The straight forward way of implementing three input cells, for each input is hardly feasible, as the IO-cell count and the required pad ring area would increase drastically. However, in core limited designs with a small pin count, it might still be possible.

Our way to get out of this misery is to develop an own IO-cell consisting of 3 standard IO-cells from the library. The pad and its ESD-structure are implemented without redundancy. However, starting with the first input buffer, the signal is redundant. This way a hit in any buffer in the IO-cell will not influence the calculations done within the ASIC. Unfortunately, this implementation is not possible for the output paths. Here a voting circuit would be necessary at least upstream the final IO-driver.

3) Macrocells

Similar to IO-cells, digital memory macros implemented as IP cannot be implemented with triple mode redundancy on a

low level, as they are fixed. A procedure here could be to work with EDAC. However it cannot be assured a hit only changes one bit of a word, as close by bits might be affected, too. If multi-bit upsets are expected, an EDAC might not be sufficient. Consequently memory macros need to be implemented redundant as block and ways to maintain the data have to be applied.

One way of data maintaining is to regenerate the data periodically. If the probability of an upset at the same bits of two memory blocks is sufficiently small, within this period, upsets are mitigated. However, usually it is not possible to regenerate the complete data. Here, a periodic refresh has to be performed. All memory cells are read and rewritten again. Evaluation of the redundancy assures correction of single event upsets. Again, the probability of a hit on the same bit of two macros needs to be sufficiently small. A clear disadvantage of this procedure is the occupation of a memory port during refresh. If only one port is available, this will enlarge access time drastically depending on the refresh period and scheduling of the mechanism.

If latch-ups in IPs like memory macros occur, there are several different methods of treatment. If a destructive latch-up occurs during normal operation, the macro cannot be used in normal operation. However, it still might be used for a very short time during start-up for instance as latch-up probability of the system would hardly be affected this way. During normal operation, the macro would need to be disconnected from power.

If non-destructive latch-ups occur, it might be possible to power-down one instance of a redundant memory after latch-up detection. After powering-up the macro again, the data can be refreshed automatically by one of the mechanisms above. Indeed redundancy would not be given any more during a power cycle and the following refresh of one instance. Single bit upsets might be stored in all three instances during refresh. Again, this vulnerable time needs to be kept short enough to sustain a sufficiently low upset probability.

Unfortunately, the radiation performance of IP macros will usually not be available before first prototypes are irradiated as no data is available for commercial IP not dedicated for space application. Evaluation of the function applied, or the necessity additional mitigation methods will arise after first prototyping. The risk of not being able to use a macro at all will remain, too until measurements have been performed.

C. Analog design

For analog cells, treating SEEs is less straight forward. As we are doing full custom design, we do not know the SEE behavior of the circuits before. There are mitigation techniques like enlarging time constants or working with analog redundancy. For analog redundancy, the analog signals can be voted e. g. by resistive networks interconnecting the outputs of redundant circuits. However, the complete circuit would be basically n times as big as the initial circuit and enlarging a circuit and its current can lead to the same results. The most important thing is radiation aware design. The possible impact needs to be taken into account.

We used several approaches to analyze the circuit for radiation aware design. One is to inject charge onto all nodes of few critical circuits during simulations, which is very extensive indeed. Furthermore we apply techniques on system level to mitigate SEE effects or to include them in the design. A third method is to include laser test in early prototyping stage to get a figure of the expected radiation behavior.

1) Charge injection simulation

The actual shape of the current pulse injected at a node during a single event differs when going to modern technologies with shorter channel lengths. We implement a model sufficient for older technologies which is presented in [4] for instance:

$$i_{node} = \frac{q}{(\tau_\alpha - \tau_\beta)}\left(e^{-t/\tau_\alpha} - e^{-t/\tau_\beta}\right)$$

The shape of the pulse for different amounts of charge can be found in the next figure:

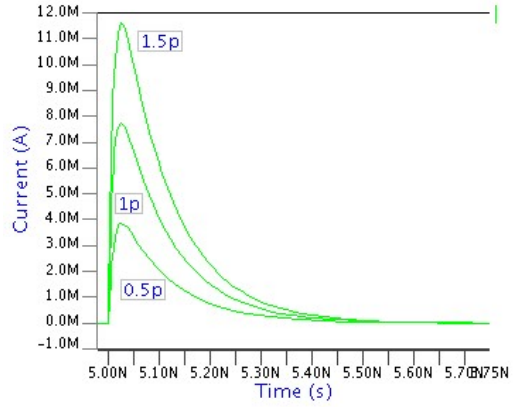

Figure 1: Current pulse for single event simulation

During our verification, we work with typical values of $\tau_\alpha = 100\,ps$ and $\tau_\beta = 10\,ps$. As charge, 1.5 pC have been taken which should correspondent to an LET of about 100 MeV/mg/cm³, however quantitative results are hard to rely on with this model. We use this method to get a rough view which nodes are vulnerable to get a starting point for mitigation. The parameters have been tuned to reproduce effects on inverter chains, which have been irradiated.

In practical simulation, a single transient simulation is done for each node of the circuit with a current source of i_{node} at the corresponding node. The insertion of the current sourced is done automatically after netlisting.

A sample simulation result, can be found in Figure 2:. Here a simple two stage OTA connected as buffer is simulated. Stimulation is done with the current pulse from Figure 1: at the high impedance output of the input stage, which is the most vulnerable node here.

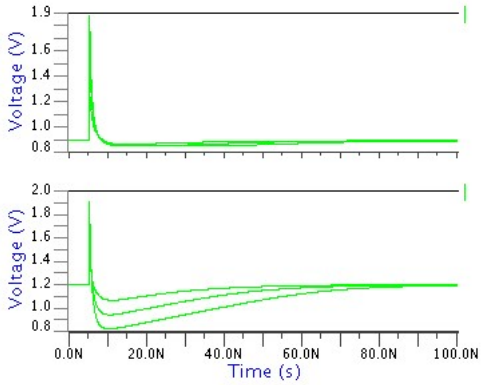

Figure 2: Single event simulation of a buffer connected two stage OTA at the high impedance node of the input stage (upper curve). The lower curve is the output of the OTA.

As the stimulated node is high impedance, the injected charge cannot be removed fast by the circuit, and the effect at the output is massive.

An issue occurring to this verification method is the simulation time. On the one side, the transient simulation has to be done for each node of the circuit. On the other hand, it has to be quite accurate as the time constants are small. The maximum time step of the simulation should be in the same order of magnitude. Else the current pulse might not have any effect on the circuit. Consequently, the simulation can only be performed for very critical circuits, like references, etc.

2) System level mitigation

Some level of mitigation of single event effects can already be done at system level. This is done by evaluation of allowed level of disruption caused by single event transients on analog signals for instance. Furthermore working with long time constants and large blocking capacitors at DAC outputs for instance will decrease the sensitivity against SETs. Measured values from ADCs on the other hand can be read several times to exclude incorrect measurements.

IV. Radiation tests

In addition to the necessary heavy ion tests and total dose tests, we are working with laser tests to get qualitative figures of possible weak spots of the ASIC. Indeed, the shape of the charge pulse created by a laser pulse might differ a lot from the pulse created by heavy ion irradiation. The length of the pulse might be different from Figure 1: for instance.

However, experiments have shown that it is possible to reproduce see effects on dedicated circuits using our laser test method. Consequently, our laser tests are a valid method to do SEE analysis before or after heavy ion irradiation. A great advantage here is the ability to do local stimulation. This way it is possible to locate the specific source of globally measures SEE-effects like latch-ups for instance.

V. Design example

A mixed signal ASIC has been designed were most of the discussed methods have already been applied. A first prototype of this ASIC exists and is currently in the lab for evaluation. Some key parameters of this ASIC can be found in Table 1:. A photo of the die is shown in Figure 3:.

Table 1: Key parameters of mixed-signal ASIC

Parameter	Qantity
Process	180 nn XFAB
Size	6 mm x 6 mm
Pins	132
Digital complexity	>150k Standard Cells
Third party macros	2
12 Bit DACs	24
12 Bit ADC	3
Analog regulator	10
Analog sensing	2
linear regulator	4
Power domains	>5

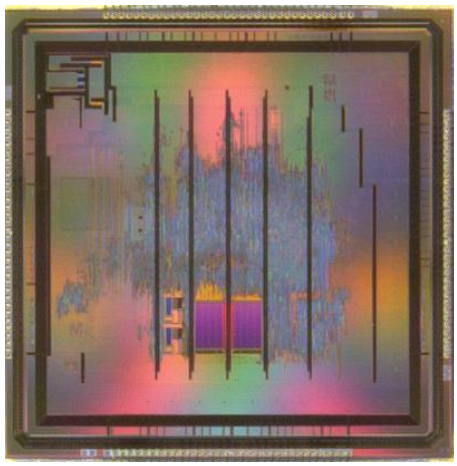

Figure 3: Die photograph of mixed signal ASIC

VI. Outlook: Supply Chain

Indeed, design life only starts with the finalization of the prototype into the production design. Finally, a complete supply chain has to be build. However, as this step is not part of the development it-self, it is not covered by the ECSS-Q-ST-60-02C [6].

Here we see at least two different ways of proceeding: Using the supply chain of external subcontractors who supply completely tested and packaged dies, or building up an own supply chain. The latter one might be more complex at the beginning, but this way all steps of e. g. qualification remain under control.

VII. Conclusion

We have presented our approach of developing mixed signal ASICS for space applications working on a commercial

process. Different ways of mitigating occurring radiation issues on system and circuit level have been shown.

Remaining challenges are efficient modeling of IP-like analog circuits within digital simulations and systematic hardening during analog design. Implementation of fixed Macros is a challenge, too, as radiation performance cannot be evaluated before testing and systematic approaches are limited as the IP cannot be changed.

The next step will be application of all concepts in a first prototype and finally qualification this device.

VIII. ACKNOWLEDGEMENTS

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IX. REFERENCES

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