MEMS gyroscope demonstration for space application, using a DPC

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Abstract

This paper reports the prototyping and performance evaluation of a MEMS Coriolis Vibrating Gyroscope developed by ONERA, connected to the Digital Programmable Controller (DPC) delivered by Thales-Belgium (TAS-B), in a gyroscope application.

The electronic architecture of the gyroscope has been mapped on the DPC cores and peripherals, and main functions developed and characterized. First a Direct Digital Synthesizer (DDS) has been implemented with a resolution better than 0.001 Hz, in order to accurately drive at resonance the high quality factor vibrating cell. A pair of ADC are operated synchronously with the synthesizer to acquire the amplitude and phase of Drive and Sense signals coming out of the vibrating cell, that are digitally demodulated in real time (over 200 kHz) using the hardware Multiplier/Accumulator of the DPC, and deliver in-phase and quadrature components to the second DPC core.

Further processing is then performed, such as an embedded PLL for the resonator, and a decimation filter to scale down the raw data stream to the sampling rate configured by the user, which takes place in a standard desktop computer running the demonstration OBC software. The gyroscope data frames are composed and transmitted by the third core on a serial port.

I. MEMS GYROSCOPES FOR SPACE APPLICATION

The main sensor of an Attitude and Orbit Control System (AOCS) in a satellite platform is a star tracker. These optical instruments are very accurate on a long term since they deliver absolute angles of the satellite reference frame with respect to far stars (the *attitude* of the satellite). However, in some cases, an inertial gyroscope (blind) may complement the star tracker :

- At the beginning of flight operations (orbit insertion), detumbling of the satellite in order to allow star trackers to acquire stellar fields;
- During operations, when star trackers are temporarily dazzled by Moon or Sun, or shadowed by Earth;
- Other safe modes, when star trackers are unavailable.

Low to Medium performance Angular Rate sensors (gyroscopes) are used for such assistance. Several technologies are available, such as Fibre Optic Gyroscopes (FOG) and Ring Laser Gyroscopes (RLG), both based on Sagnac effect, or Hemispherical Resonating Gyroscopes (HRG) based on Coriolis effect.

Performance improvements of MEMS CVG, another family based on Coriolis effect, associated with their native advantages in small size and low power consumption, led to their progressive introduction into markets dominated by other technologies. The replacement of low to medium performance gyros by MEMS CVG is today foreseen in a growing number of systems [1] [3], including space applications, from micro satellites, obviously, to medium size or even geostationary platforms [3].

II. CORIOLIS VIBRATING GYROSCOPE

The CVG sensor head is a mechanical resonator vibrating at resonance using the In-plane Drive mode (Figure 1). When the gyroscope is exposed to an angular rate in the z-direction, the Coriolis acceleration ($\overrightarrow{A_c} = 2\vec{\Omega} \wedge \vec{V}$) initiates the Out-of-plane Sense mode. Although it is forced to the drive pulsation ω_x, (Sense mode resonance pulsation is ω_y), the amplitude Y of this vibration is significant (ω_x and ω_y are close to one another), and proportional to the input angular rate Ω. This architecture requires very little subsystems and is known as the Open Loop mode.

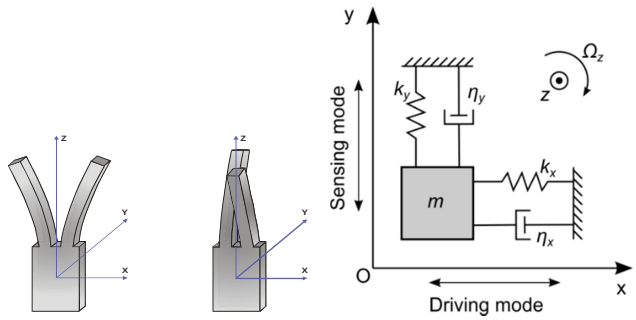

Figure 1 : Tuning fork gyroscope principle (left), showing Drive and Sense modes. Equivalent mechanical system (right), with two degrees of freedom.

Other more sophisticated modes are available, for higher performance, as *force rebalance* or *closed loop* (controlled sense mode), and *whole angle* (no difference between drive and sense, isotropic vibration) [4].

ONERA has been developing vibrating MEMS inertial sensors for various applications. The VIA cell (Vibrating Beam Accelerometer family) is already in use in the French civil and defence industry. The VIG cell (Coriolis Vibrating Gyroscope family) has been proposed for low cost assistance gyroscope in the frame of the NEOSAT program (Figure 2).

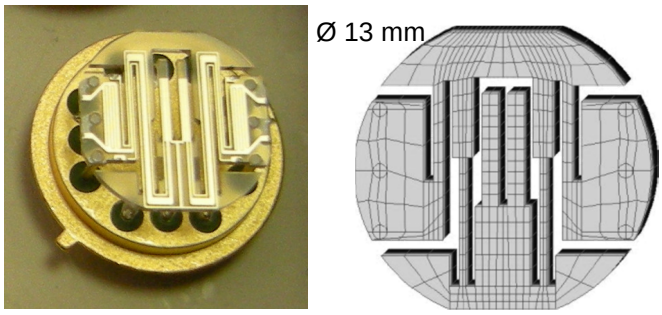

Figure 2 : VIG quartz cell mounted on socket (left). Mechanical model for Finite Element simulations (right).

During previous activities several aspects of the VIG have been investigated, in the objective of a future qualification. The gyroscope quartz cells endured radiations successfully up to geostationary dose (100 krad), and could also withstand launcher vibrations. Shocks were also acceptable with intercalated passive damping layer. Concerning electronics, the design and realization of an ASIC was initiated, but prohibitive cost prevented from further development. Nevertheless it was assessed that the electronic architecture of the ONERA gyroscope was compatible with the Digital Programmable Controller (DPC) developed by TAS-B. Once the chip was released last year, the opportunity to build a demonstrator was found with CNES, the French space agency.

III. ONERA MEMS CVG ARCHITECTURE

The piezoelectric material of the resonator allows both action and detection, using respectively the reverse (voltage to force) and direct (deformation to charges) piezoelectric effects (n_x on Figure 3). Electric charges are collected by gold electrodes and converted to voltage by charge amplifiers and demodulated. The Drive in-phase signal (Φ) is controlled down to zero by the Phase Locked Loop (PLL), to ensure Drive resonance at all time. The Drive quadrature signal (Q) is optionally used in an independent Automatic Gain Correction (ACG) loop. The "cos θ" and "sin θ" coupling terms take into account little errors of cell realization, in the etching process, whose overall effect is a rotation of mechanical vibration axes with respect to the electrode frame. A small amount of Drive motion may thus be coupled into Sense signal, which is known as *quadrature error* [5].

At least a passive re-injection of Drive voltage (V_D) through a tuned impedance is necessary to avoid voltage saturation at Sense amplifier level, before processing. Quadrature residuals are then efficiently rejected by the synchronous demodulation.

Apart from charge amplifiers, which are simply built on discrete operational amplifiers, all other functions are digital, including analog-to-digital converters.

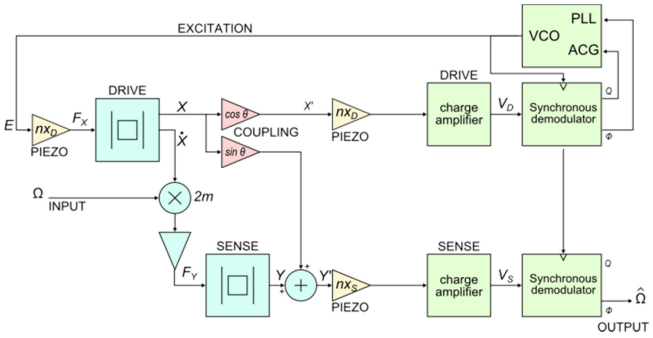

Figure 3 : Coriolis gyroscope architecture. Blue : mechanical resonators; yellow : action and detection transduction; green : electronics

IV. DPC INSIDE

The DPC is an innovative highly integrated mixed signals controller. It targets several applications mostly related to sensing and power conditioning. This includes power conversion (DC-DC, AC-DC, DC-AC, AC-AC), motor control (DC, stepper motors, AC with up to 6 phases), multi-standard communication between several clients and protocol translation, and remote sensors [6].

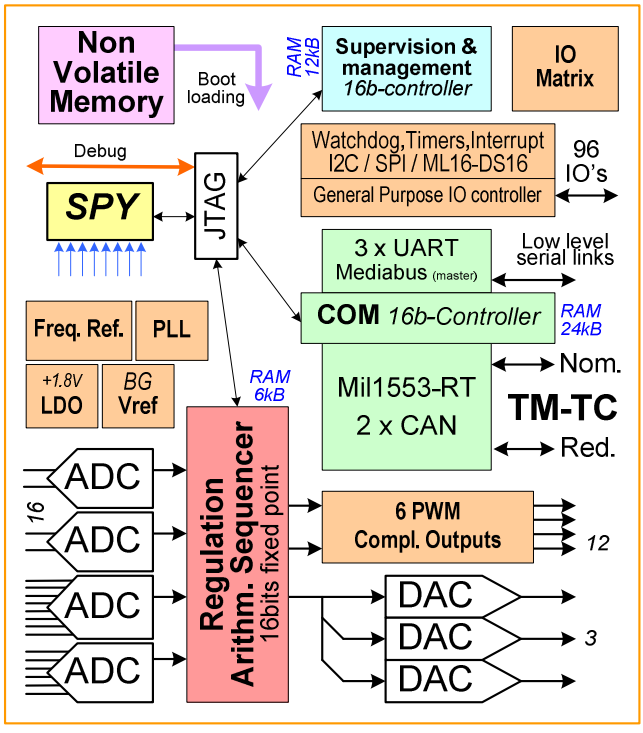

Figure 4 : DPC architecture. Three specialised cores can run simultaneously : RAS, SSM, and COM. The fourth core, SPY, is intended for debug.

The microprocessor architecture, MSP 430, may be considered “old fashioned”, but actually answers two issues :

- After 10 years development, 10 years production, and 15 years in orbit, compiler tools shall be still available to upload new software; only an open source architecture can guarantee this.
- Modern 32 bits architectures are versatile and attractive, but also RAM consuming, and features like memory management for multi-task OS are out of scope for the targeted applications. Here a 16 bits architecture was a good trade-off

Besides, the architecture is not orthogonal and the three cores are actually dedicated to their peripherals.

Knowing that, electronic architecture of the gyroscope has been mapped on the DPC cores and peripherals, and requirements set in terms of A/D D/A converters, voltages, CPU usage, and communication with host.

At the lowest level, but also at the highest sampling rate, the sinusoidal excitation signal is calculated by the RAS core and output to the DAC. Two channels are used, to form a differential pair, avoiding an external inverter.

The quartz resonator delivers two signals, in response to the excitation above : drive and sense. They need to be sampled and acquired with strictly synchronised ADC. This is possible in the DPC, where ADC3 and ADC4 (differential voltage input) share a common sequencer, clocked by RAS. As all signals are carried by the resonance frequency, the synchronous demodulation is also performed by RAS.

At higher level, the SSM core is in charge of the decimation, from the sequencer frequency (higher than the sensor head resonance), down to the desired instrument sampling rate. SSM is also in charge of various long term control loops, the most important being the PLL to keep the mechanical head resonating. Processing is more complex, but at lower rate.

When decimation occurs, the SSM data are transferred to the COM core, which will build the data frame to be sent to the OBC on a digital link. Various UART protocols are supported by the DPC, as well as CAN and 1553 buses. COM will also receive and decode commands from OBC.

V. Frequency Synthesis

The first critical function is the frequency synthesizer, based on Direct Digital Synthesis (DDS). Such a synthesizer makes use of a phase accumulator, delivering the instantaneous phase of the desired signal by adding at each sampling time a phase increment. The phase then enters a Look Up Table (LUT) to get the output waveform, generally a sine wave, which finally feeds the DAC. If NA is the binary word size of the phase accumulator (so that 2^{NA} is equivalent to 2π), F_{RAS} the interrupt rate of the RAS core, and W the phase increment, then the output frequency is

$$F = W \frac{F_{RAS}}{2^{NA}} \qquad (1)$$

The best code allowed the RAS job to complete in 5.6 µs, which means a rate of 180 kHz. Coupled with a phase increment word size of 32 bits, the resolution of the synthesizer was 40 µHz, which looks extremely accurate but is actually only acceptable compared to the resonance bandwidth of the quartz cell. The quality factor is indeed around 200 000, so that the resonance bandwidth is 45 mHz, and the synthesizer frequency step shall be small with respect to this value.

When sampling the desired frequency at a fixed rate, the signal is not rigorously periodic, and aliasing occurs : spectral lines of the sampling frequency and multiples are folded back close to the target frequency.

We used a modified version of the DDS, where the number of steps per signal period is fixed integer and the sampling frequency is tuned to match the target. This is done in the DPC by modulating the duration of the RAS main sequencer, which is set by division of the internal 120 MHz reference clock. The RAS cycle can now run up to 220 kHz, leaving 12 samples per period at 17 kHz, the vibrating cell Drive resonance. A 32 bits word is used for the RAS cycle, so that the frequency synthesis resolution is now 85 µHz at RAS level, which means 85 / 12 ≈ 7 µHz on the target frequency.

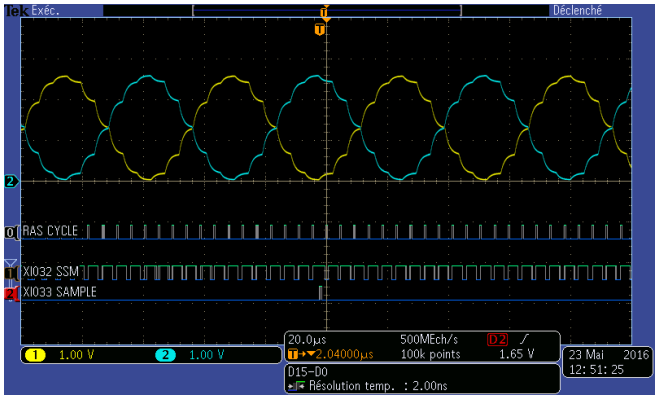

Figure 5 : Sine waveform generated by RAS core, 12 symmetric samples per period, on DAC1 and DAC2. F_{RAS} = 220 kHz max.

VI. Digital Demodulation

Both Drive and Sense signals need to be acquired simultaneously and synchronously. This was the main expected feature of the DPC for the gyroscope architecture : two parallel and identical ADC channels, together with a hardware Multiply/Accumulate unit (MACC).

Let x_k be a sine signal composed of an In-Phase term XP and a Quadrature term XQ, and sampled at the rate Ts ($\theta = 2\pi.F.Ts$) :

$$x_k = XP \cos k\theta + XQ \sin k\theta \qquad (2)$$

The demodulation of x consists in multiplying it with $\cos k\theta$ and accumulate, to get the Phase term, and with $\sin k\theta$ and accumulate, to get the Quadrature term.

$$\widehat{XP} = \frac{2}{N}\sum_{k=0}^{N-1} x_k \cos k\theta$$
$$= XP + \underbrace{\frac{XP}{2N}\sum_{k=0}^{N-1}\cos 2k\theta}_{\Sigma C} + \underbrace{\frac{XQ}{2N}\sum_{k=0}^{N-1}\cos k\theta \sin k\theta}_{\Sigma CS} \quad (3)$$

ΣC and ΣCS will naturally cancel when $N\theta$ is a multiple of 2π (an integer number of periods is covered). For this reason, when the decimation occurs, the SSM just waits for the next end of period to complete the sum, so that it is performed on the expected integer number of complete periods, and the estimators of XP and XQ are accurate. The phase jitter of the instrument sampling time due to this fraction of carrier period is negligible, with respect to the data frame transmission for example.

The DPC designers implemented a MACC function in the RAS on purpose (a second one in the SSM), but unfortunately, the accumulator can only remember one sum; here four accumulators are needed for Drive/Sense, Phase/Quadrature terms. As reloading the accumulator and saving the result each time would have wasted the code performance, the running sums are performed by software. Actually an addition is performed in one CPU cycle, the same as just moving the data.

To keep the high throughput, RAS and SSM have been pipelined (Figure 6) :

- Data transfer from RAS to SSM using mail box;
- Synchronisation using trigger signals between cores (RAS is master)

Therefore the CPU power is doubled for the main operation (low level, high data rate). The resulting data rate is 1.3 Msps (3 acquisition slots per sampling period, 2 channels), the data processing rate is 880 kMACC/s and the inter CPU data flow is 35 Mbit/s.

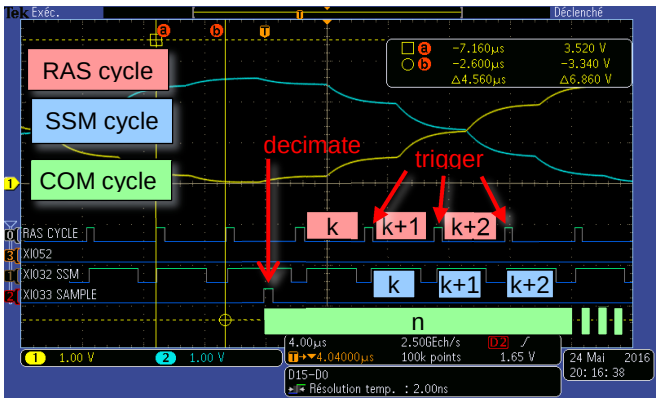

Figure 6 : Pipeline between RAS and SSM. Sampling interval is 4.56 µs (220 kHz). End of RAS activity triggers SSM.

At the decimation rate (~30 Hz for the instrument output), a snapshot of the demodulation accumulators is transferred from SSM to COM. The latter performs data frame formatting for transfer to OBC, via the selected interface. In this study, an RS232 UART was implemented, but CAN, or 1553 are also available.

VII. EXPERIMENTS

A. *Development board*

The board is a DPC Reference Kit (DRK), designed and distributed by TAS-B. . It consists in a true qualified DPC, mounted on an evaluation board with power supplies, I/O connectors and programmer access through JTAG. All I/O signals in the DPC, logic and analog, are accessible on the board connectors (Figure 7, Figure 10).

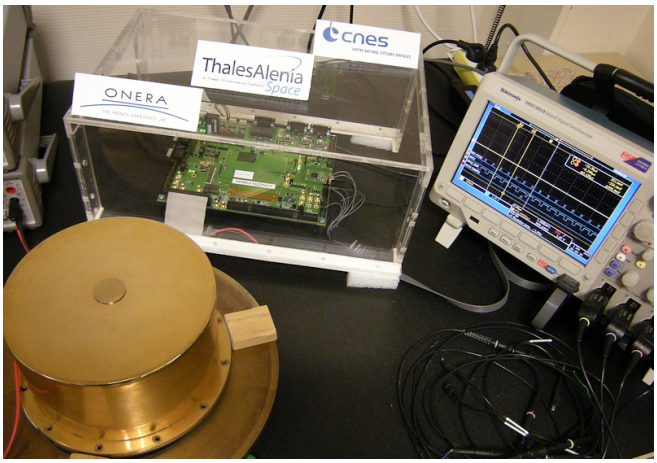

Figure 7 : DRK (under plexiglass case). Digital signals as well as analog signals on the scope are available. The golden cylinder on the lower left is a vacuum chamber for the gyroscope.

B. *Software tools*

The DRK comes together with software tools (compiler, debugger, configuration manager), offering the developer a complete toolchain from C source code to oscilloscope view of signals. Two desktop computers are in place to manage the DRK (Figure 8) :

- The PC-DPC contains software tools for application development : Eclipse based IDE, gnu compilers, JTAG and debug tools;
- The PC-OBC is dedicated to the user application. When embedded codes for all cores are finalized and uploaded in DRK, only PC-OBC is in use.

The PC-OBC should be representative of an on-board computer. For this demonstrator, PC-OBC is able to send commands for parameters, using a basic ASCII format :

S xxxx ↵	set the decimation rate
L xxxx ↵	close / open the PLL
F xxxxxxxx ↵	set synthesizer frequency

Parameters xxxx are written in hexadecimal, which is a good tradeoff between human readability on a terminal and encoding/decoding efficiency in the microcontroller.

The PC-OBC also reads data frames to depacket, plot, analyse and save the gyrometric data. The same

hexadecimal readable ASCII format is used for the frame encoding. Baud rate is not critical and a standard 115200 baud UART can handle the application.

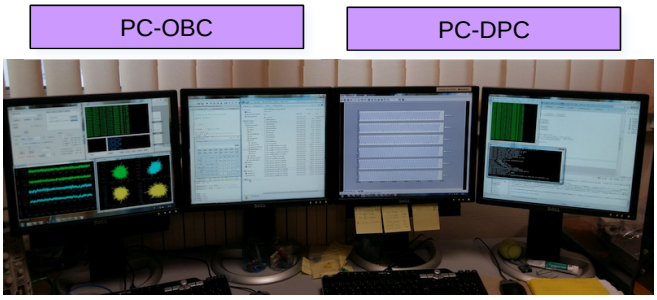

Figure 8 : PC-DPC (embedded software development and debug), and PC-OBC (data collect and line plot).

A graphical user interface has been developed with Python/Qt, so that commands and data can be managed directly from the interface, or scripted in a batch mode.

C. *Gyroscope Demonstration Model*

The VIG quartz cell is mounted on a socket (Figure 2, left), which is then soldered in a copper case. A small pipe allows pumping and offgassing at high temperature, so that the vacuum chamber can be definitely sealed by a pinch-off operation. This is an easy and efficient vacuum encapsulation. The proximity electronics are reduced to front end amplifiers, and are made of operational amplifiers (low noise, low input capacitance). All other functions are in the DPC (Figure 9).

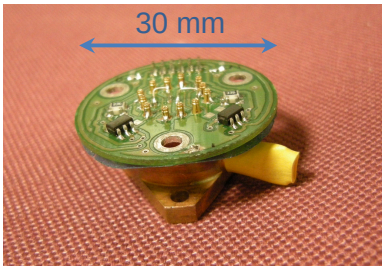

Figure 9 : VIG gyroscope in a copper vacuum package and connected to proximity electronics.

In this Demonstration Model, all analog signals (excitation from DAC and pre-amplified signals to ADC) are connected to the DRK through one of the six ribbon cable available (Figure 10). Obviously this is not an ideal connection and a possible Engineering Model designed for the DPC Plugin Module (DPM) for example, or in this range of size, would be more stable, with shorter wire length, avoiding coupling and stray capacitances.

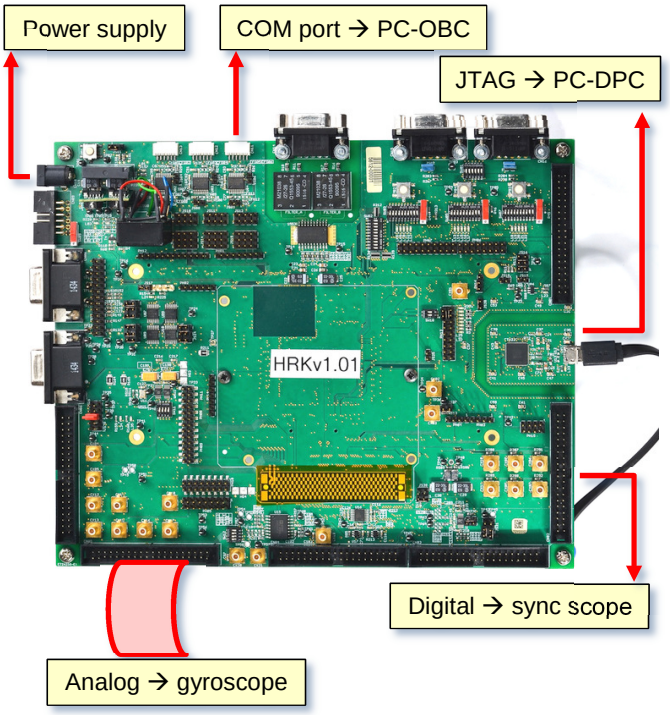

Figure 10 : DRK setup. The upper face is for the DPC Plugin Module (DPM), and the lower face is for a standalone DPC.

One important characteristic of the CVG has to be explained here. Back to Figure 3, the Sense signal, *Y'*, includes Coriolis information as well as a coupling term from the Drive amplitude, which is extensively discussed in the literature [5]. But both are carried by the Drive vibration *X*, amplitude and phase.

$$Y' = \frac{2m\Omega}{\Delta\omega}\dot{X} + \sin\theta \; X \qquad (4)$$

where Ω is the input angular rate, m is the equivalent vibrating mass of the resonator, and $\frac{1}{\Delta\omega}$ is the gain of the Sense transfer function, which is not exactly working at resonance, but $\Delta\omega$ apart. Consequently, dividing Y' by X' (complex division) naturally normalizes the Coriolis detection with respect to Drive fluctuations. No control loop is needed on the Drive amplitude, and PLL stability (the phase of *X*) can be released.

Fortunately, this division occurs only on final samples, after demodulation and decimation, at a low rate, so that it can be handled by the OBC, marking the boundary between low level - simple arithmetic - fast rate operations (inside DPC), and high level - complex arithmetic - low rate post processing (inside OBC). The data frame then transfers Drive Phase, Drive quadrature, Sense Phase, Sense Quadrature to the OBC (Figure 11). Other parameters are for debug : resonant frequency tracking, number of samples in decimation, various multiplexed monitoring values.

The Coriolis signal, result of the division in OBC is plotted on Figure 12. Despite fluctuations of the PLL, that are due to

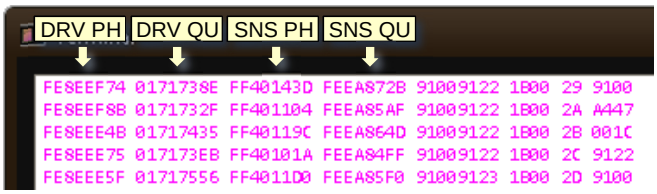

Figure 11 Data frames from DPC to OBC on the UART port (115200 bauds).

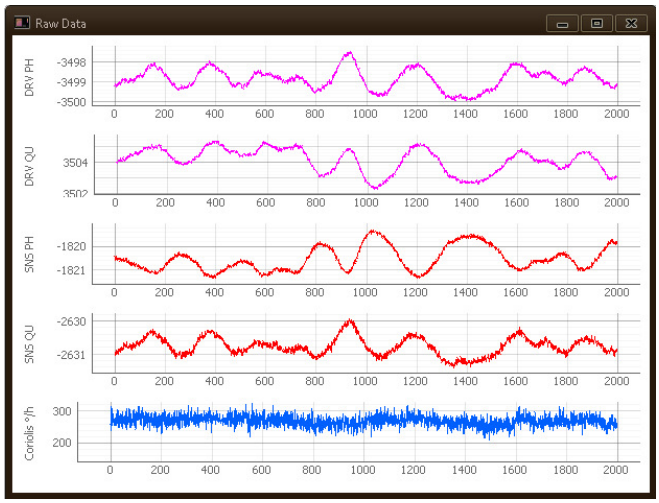

Figure 12 : Drive components (upper), Sense components (middle), and Coriolis output (lower).

D. Results and performance

First, the DPC noise floor is measured, connecting ADC3 to the gyroscope pre-amplifier output, but out of resonance, so that only amplifier noise is captured, and ADC4 to ground. Noise spectral density is plotted on Figure 13. The initial resolution of the A/D converters is 13 bits. Thanks to the very high internal sampling rate (~200 kHz), the averaging at the instrument output sampling rate (~30 Hz) is efficient, and thanks to the demodulation, *1/f* noise, or flicker noise, is much reduced. The noise spectral density is better than 1 µV/√Hz for both ADC3 and ADC4, and the long term resolution, after 100 s averaging, is 0.1 µV, while the LSB is 0.3 mV. This is equivalent to a 23 bits conversion. More reasonably speaking, the resolution is 20 bits at 1second.

The internal sampling rate is actually close to the maximum, because the 3 slots available in the RAS cycle are used to acquire data, leading to a raw sampling rate of 600 kHz on each ADC.

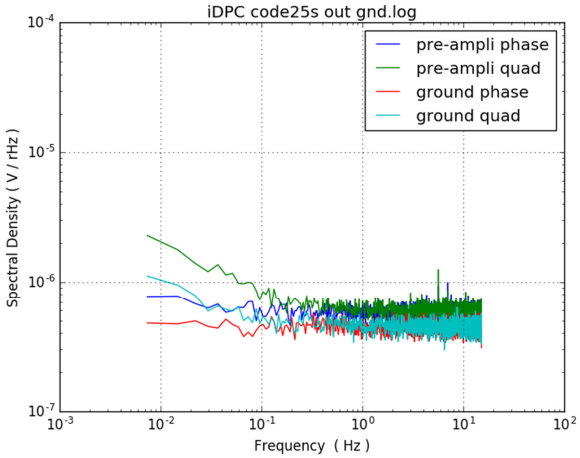

Figure 13 Preliminary characterization of the DPC ADC 3 (pre-amplifier) and ADC4 (ground), for differential voltage measurement.

The performance of a gyroscope is mainly characterized by its Angular Random Walk (ARW). It means the standard deviation of the angle output, integrated from the angular rate, generally after one hour. ARW is extrapolated on the angular rate Allan variance, taking the left asymptote at one hour.

On Figure 14, the black line comes from the previous grounded input, processed with scale factor as if it were the gyroscope signal. It provides DPC noise contribution in this application. The equivalent ARW is 0.01°/√h. Then the blue line is recorded with the pre-amplifier and vibrating cell connected, but away from resonance, so that it is representative of electronics. The equivalent ARW is slightly degraded, 0.03 °/√h, but still satisfactory in the gyroscope application. Finally the system is operated at resonance in the true conditions of the instrument. The ARW is further degraded (red line, up to 0.07 °/√h), yet acceptable; the main disappointment comes from the Allan variance minimum, which is around 15 °/h, and translates to the $1/\sqrt{f}$ slope in the spectral density.

Investigations performed into this degradation revealed that a feature of the DPC may be the cause of the problem. When writing to the DAC, the value is not directly effective on the converter, but is re-sampled by a 3.75 MHz sub-clock of the 120 MHz core clock. While RAS cycle occurrence and sampling times in the ADC are controlled with a resolution of one core clock period (8 ns), the DAC registers are also updated with that precision, but the conversion will be effective after a delay between 1 and 32 clock periods. This causes a small jitter with negligible impact on the out-of-resonance measurement, but with annoying impact at resonance, due to the large amplitudes measured.

When the RAS period is a multiple of 32 core clock periods, then the time of DAC refresh always occurs synchronously with the re-sample sub clock. Now when the RAS period differs from that multiple, DAC refresh time will drift and the resulting excitation signal for the resonator will be modulated.

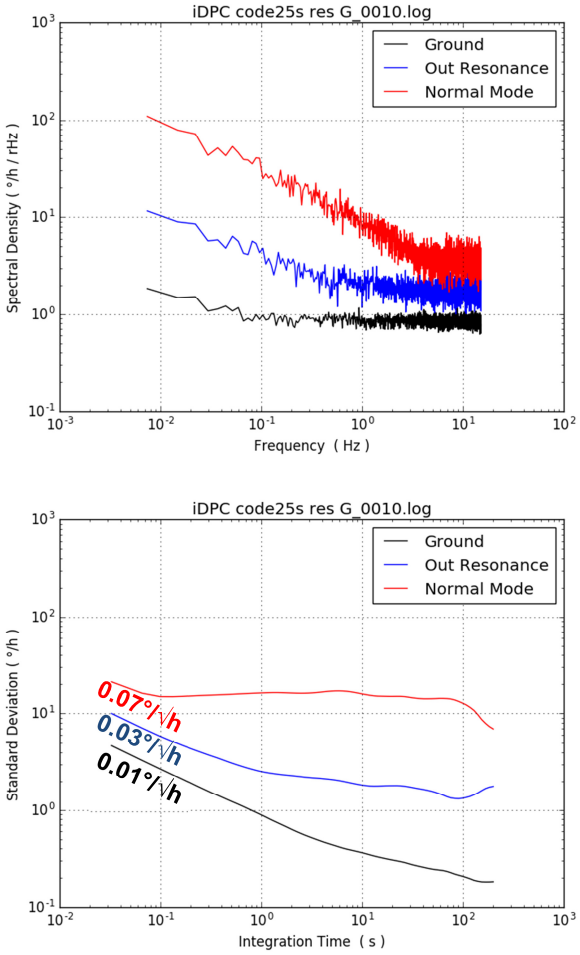

Figure 14 : Gyroscope DM noise performance. The same data are processed for noise spectral density and Allan variance.

This effect is shown on Figure 15. The signal fluctuation can be increased by a factor 10.

Ongoing work is focused on the coherency of RAS cycle period and DAC resample. Workaround can be found, at the expense of synthesizer resolution, but the 7 µHz obtained above can be relaxed thanks to the complex division algorithm.

Besides, the DAC sampling scheme should be revised in version 2 of the DPC ASIC, the best option in our case being a synchronized latch of the DAC with the ADC sequencer.

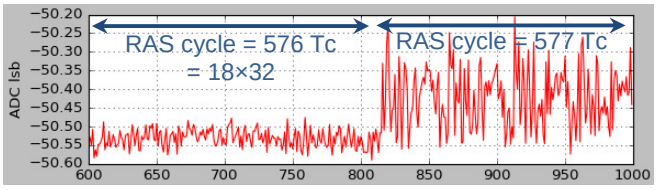

Figure 15 : Effect of DAC re-sampling on one demodulated output.

VIII. CONCLUSION

A gyroscope Demonstrator Model has been built with a DPC as main electronic device connected to the quartz Coriolis Vibrating Gyroscope developed by ONERA, all other components being operational amplifiers. This simplified architecture allows defining a low cost MEMS sensor, targeting applications in the range of assistance to star tracker. It could be included in the star tracker, or integrated in the OBC motherboard.

The DRK allows live power measurement in the DPC. As expected, the current driven is 500 mA on 1.8 V for the digital circuits. Some unused peripherals like 1553 interface and PWM have been disabled. Analog circuits of the DPC require 50 mA on the 3.3 V supply, and external amplifiers require 30 mA. The total power for one gyroscope sensor is 1 W.

The software functions developed for the sensor match the intentional asymmetric core design of the DPC, and all three cores are in use in the application. The program memory is tiny for each core (4K, 8K, 16K), but keeping an eye on assembler generated by the compiler allows the programmer to write clean yet efficient code.

At this time about 30 % of the available program memory is used in the DM, leaving margin for further development (Figure 16).

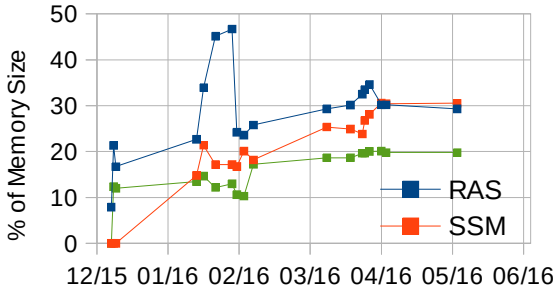

Figure 16 Percentage of program memory used in each core during development.

Generally speaking, high over-sampling and efficient synchronous demodulation implemented here bring the ADC resolution up to 20 bits, which makes the device interesting for numerous metrology applications, where carriers can be preferred to DC polarisation of sensor heads. The 20 bits performance is obtained in the following conditions:

- Differential pairs to reject common mode parasitic signals;
- Sinusoidal signals and synchronous demodulation to reject bias and flicker noise in amplifiers;
- Renormalisation by division of two parallel channels, to reject reference voltage fluctuations;
- Contiguous decimation synchronised with signal period to preserve averaging efficiency

IX. PERSPECTIVES

The first performance demonstration of the ONERA gyroscope cell in a space architecture design is encouraging, considering the following opportunities of improvement :

- The excitation level of the quartz cell is currently ±1.25V, limited by the DAC range (no cascaded amplifier). It can be increased by a factor 2 or more without damage to the quartz cell, increasing the signal to noise ratio;
- The quadrature term was very important in the generation of quartz cell of the demonstrator. It implies external re-injection of drive into sense to compensate for the $\sin\theta$ term, at least to de-saturate the pre-amplifiers. The next generation cells will have reduced quadrature terms;
- The size of the cell can be increased for free, as long as it remains smaller than the DPC device. An x times larger cell delivers x^2 times more piezoelectric charges.

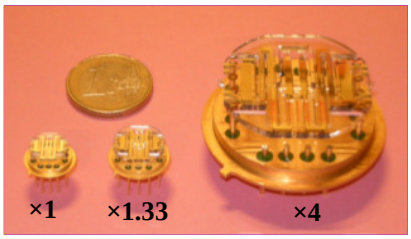

Figure 17 : scaled gyroscope cell for stronger signal. The DM cell is the 1.33 scale.

After this demonstration, ONERA is ready to return the DRK and build an Engineering Model, in an integrated design, so as to perform environment characterisations.

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