Serial I/O ADCs/DACs : The Next Giant Leap in Mixed-Signal for Space

R. Bedi

Spacechips Ltd, Harpenden, U.K.

rajan@spacechips.co.uk

Abstract

Today, the cost and effort to develop satellite payloads, platforms and space instruments have to be repeated for each new mission, introducing unnecessary re-design, re-test, performance, re-qualification, schedule and budget risks to key programs.

Operators are constantly complaining to OEMs that the cost to develop satellites is prohibitively expensive, delivery takes too long and never right-first-time, while satellite manufacturers are handicapped by the reusability limitations of current mixed-signal electronics.

Today, 3 billion people around the world do not have internet access and new, Silicon-Valley entrepreneurs intend to build thousands of low-cost, satellites to address this market. The traditional approach to developing space electronics is simply too bespoke, too expensive, too inflexible and too power consuming to deliver tomorrow's, space-enabled world for everyone.

Serial-I/O ADCs/DACs offer manufacturers of satellite sub-systems the potential to deliver spacecraft operators bespoke levels of performance without having to continually re-engineer the avionics. Individual customer needs can be accommodated by simply swapping pin-to-pin compatible ADCs/DACs each with different resolutions (SNRs), because for the first time, the digital interfaces will remain the same. This novel advance means that only mission-specific, on-board processing algorithms will have to be re-coded, completely eliminating non-recurring, hardware design effort and cost. Recurrent test and manufacturing costs will also be reduced, allowing future satellites to be delivered right-first-time, within budget and to schedule.

Introduction

The digital payloads used on the Sentinel-1 and NovaSAR, Earth-observation satellites performed very similar functions but each had its own architecture, hardware design, fabrication, assembly, test and qualification. Effort and cost had to be duplicated and in terms of performance, the only difference between both was one effective bit.

Similarly, the digital payloads used on Alphasat and that being developed for the Inmarsat 6 telecommunication satellite perform very similar channelizing functions, but each has its own architecture, hardware design, fabrication, assembly, test and qualification. Effort and cost was duplicated and in terms of performance, the only difference between both payloads was 2 dB and extra information bandwidth.

The traditional approach to developing mixed-signal, payload electronics is simply too bespoke, too expensive and too inflexible.

The JESD204 Standard

Parallel-I/O devices have reached their limits in terms of pin count, package size, parasitics and managing skew between digital signals and their clocks. High-speed serial links embed clocking information within the bitstream which is extracted by the receiving device.

Initially semiconductor vendors developed their own proprietary serial-I/O ADCs/DACs with little or no interoperability between these or companion logic devices. To standardise devices, JEDEC formed a working group and published the first industry-wide standard for serial-I/O ADCs/DACs in 2006. This defined a high-speed serial link for a single lane with a maximum data rate of 3.125 Gbps as illustrated below:

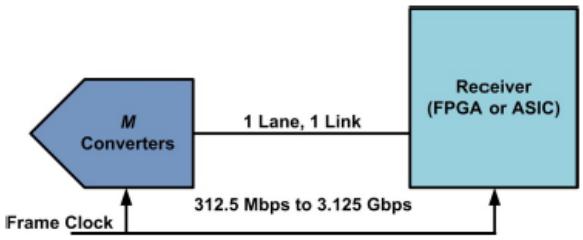

Figure 1: Serial ADC connected to a FPGA

In 2008, JEDEC formally released revision A of the standard which supported multiple-aligned serial lanes with data rates up to 3.125 Gbps as shown below:

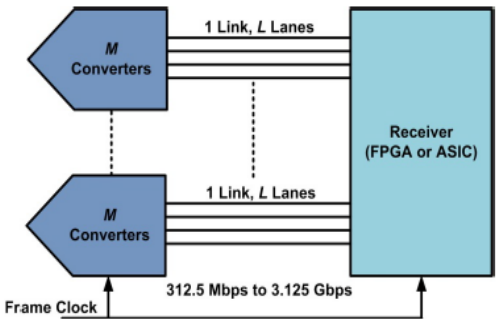

Figure 2: Serial ADCs connected to a FPGA

To accommodate the increasing performance needs of cellular base-stations, JEDEC released revision B of the standard in 2012 which added deterministic latency and supports data rates up to 12.5 Gbps as illustrated below:

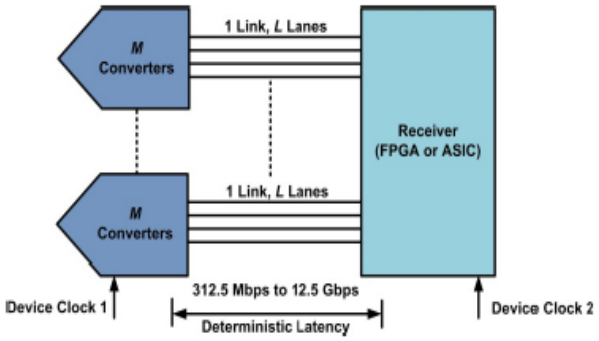

Figure 3: Serial ADCs connected to a FPGA

A serial-output ADC connected to an FPGA is shown below. The ADC is physically small, 10 x 10 mm, occupying significantly less footprint than an equivalent, parallel-output ADC. Only two pins are required for each high-speed serial link, easing PCB layout and routing effort, resulting in simpler and less expensive PCBs as shown below:

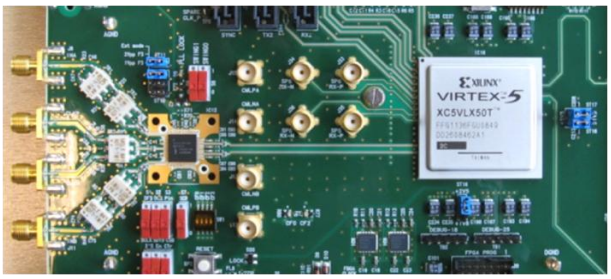

Figure 4: ADC connected to FPGA using high-speed serial links

Due to limits in the number of available I/O, up to four broadband, parallel-I/O ADCs/DACs can be reliably connected to one V5QV FPGA. Achieving timing closure of several hundred high-speed I/O can be very challenging. Conceptually, many more serial-I/O ADCs/DACs can be connected to one FPGA as illustrated below:

Figure 5: Serial ADCs/DACs connected to a space-grade FPGA

Hardware verification of digital interfaces will change from traditional IBIS simulation to IBIS-AMI modelling. This too has been standardised by silicon vendors and the EDA industry to allow interoperability between devices. The analogue and mixed-signal extension to the IBIS specification was developed to simulate a BERT, allow interoperability between models from different semiconductor vendors using commercially available EDA tools, with the ability to simulate ten million bits in minutes.

Compared to traditional IBIS, protected, proprietary, behavioural DSP algorithms have been added in the form of compiled executables to support SERDES emphasis and equalisation functions.

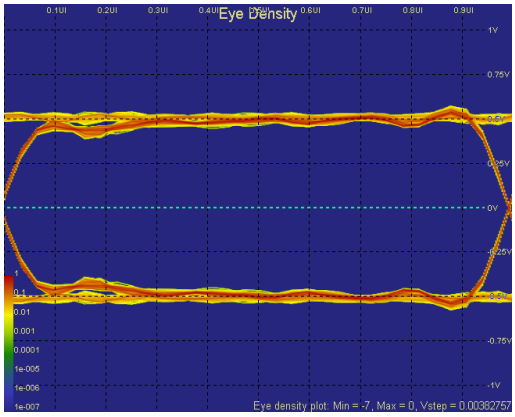

Figure 6 : Serial ADC connected to an FPGA

Serial-I/O ADCs/DACs also offer the potential of locating mixed-signal convertors at the RF receive/transmit antenna, exploiting high-speed serial links connections to the digital payload processor.

Conclusion

JESD204 is a mature and proven standard adopted by the global electronics industry and supported by the major mixed-signal providers.

JESD204B offers deterministic latency capability to support digital beamforming applications and can offer the space industry the same benefits it delivered cellular telecommunications.