

# Single Event Simulation and Error Rate Prediction for Space Electronics in Advanced Semiconductor Technologies

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**Abstract:** The effect of a single event in today's advanced semiconductor technology is no longer restricted to a single circuit node, and can depend strongly on layout details, on the angle of the ion, and on the response of the circuit during the charge collection. In order to catch weak spots in circuits and layouts, and to get reliable predictions for space error rates, it is important to have a possibility to model the circuit designs with a full (and correct) description of the layout, of direction of the ion, and of the time profile of the charge collection.

This paper discusses simulation techniques which makes this possible, while still being fast enough to be used to generate full cross-section maps and error rate predictions for different radiation environments. Application examples from advanced FinFET technologies (logic) and bulk technologies will be presented, along with comparisons to measured single event data. The application of the simulation techniques to remove or reduce the single event error rate will be discussed.

**Index Terms**— Soft error, single event effect, radiation hardening, SET, SEU, layout optimization, LEAP, RHBD

## I. INTRODUCTION

In today's most advanced semiconductor manufacturing technologies the effect of a radiation generated single event extends over many individual devices in a circuit. This leads to new effects and requires more advanced analysis methods and new techniques for hardening against radiation. It also increases the rate of multiple errors, multi bit upsets (MBUs), in the circuits. The MBU increase, along with the sheer increase of size and complexity, cause the overall rates of radiation generated errors of chips and systems to go up, and increase the importance of estimating and controlling radiation effects, not only for space applications, but also for critical terrestrial applications.

The fact that a single event affects several devices, i.e., several nodes in a circuit, means that the relative placement of the devices and their contacts can have a very strong impact on the radiation sensitivity. To reliably capture these effects in simulation and prediction of single event effects it is essential to use methods with an a priori dependence on the layout.

Both the analysis and mitigation of single event errors also have to adhere to the stricter design rules and design hierarchy of modern chip design, which leaves little, or no, room, for customization. Qualified radiation hard building blocks (standard cells and other IP) which seamlessly can be inserted in the design flow alongside other (not hardened) circuitry, is required to enable cost and time effective radiation hardening.

## II. PREDICTION TECHNIQUES: SIMULATION

In order for a simulation technique to capture the effects of the layout on a single event in a predictive manner, it is preferable to use a model which remains valid regardless of the particular layout used, i.e., a model based on the underlying physics of charge generation and transport, such as

the semiconductor transport physics models used in traditional TCAD device simulation. Traditional device simulation, however, is too computationally intensive to generate sufficient information about the single event behavior of a circuit (cross-section, error rates, etc.), which requires a large number of individual single event simulations in a complex 3D structure with many devices. To alleviate this a hybrid device simulation method has been developed [1][2], which still includes a full representation of the 3D structure, of the simulation of the charge generation and transport therein, and of the contacts and the layout, but permits the simulation of the electrical device characteristics to be run using the circuit compact models (Figure 1).

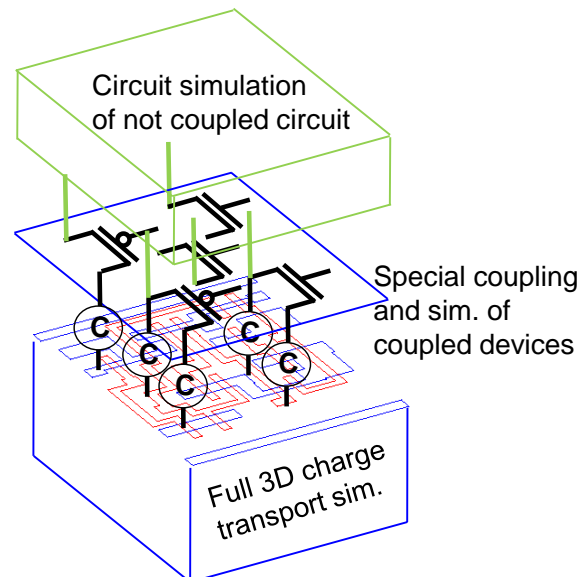


Fig. 1. Illustration of the specialized (hybrid-) single event devices simulation in the tool Accuro [2].

This single event device simulation method is capable of simulating a single event between 10-100X faster than regular

traditional device simulation, while maintaining the accuracy and predictive capability of full device simulation. This still makes it considerably slower than pure circuit simulation, but one simulation of a single event in a small to medium circuit can be done in minutes, and it can also handle much larger circuits (as much as several hundred devices can be included in the 3D structure). The method makes it possible to run the large number of individual simulations (1000-100,000) required to generate full cross-section and cross-section maps.

Since the simulation contains a full description of all doping regions, it fully captures latch-up and other bipolar effects as well.

Figure 2 shows an example of a simulation structure, used in this type of simulation, of a redundant flip-flop (FF) in an advanced FinFET technology. It captures the device placement, layout, and doping of the FF and its' surrounding. But, through the use of special models at the contacts, makes it possible to simplify the details of the individual devices and used the circuit compact models to model the electrical device behavior.

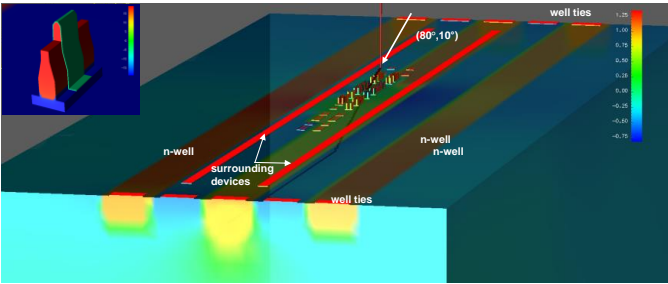


Fig. 2 Snap-shot from the modeling of a LEAPDICE flip-flop in 14nm FinFET technology. The figure shows the potential distribution (partially transparent) during the early phase of a single event at an incident angle of  $(80^\circ, 10^\circ)$ .

### III. PREDICTION TECHNIQUES: ERROR RATE ESTIMATION

The simulation technique described in section II is capable providing the cross-section function,  $\sigma(\theta, \phi, LET, S)$ , of a small to medium circuit as a function of the LET and the angles of incidence,  $\theta$  and  $\phi$ , (and of the circuit state  $S$ ), and the simulation results can be verified directly to measured cross-sections at specific LET values and angles of incidence (section IV shows some selected examples).

If the cross-section is known, it can be applied to calculate the expected error-rate under a certain particle flux spectrum,  $f_{flux}(\theta, \phi, LET)$ , measuring the differential flux per unit area and steradian as a function of LET and spherical angles;

$$ErrorRate = \int dLET \int_0^\pi \sin \theta d\theta \int_0^{2\pi} d\phi \{ \sigma(\theta, \phi, LET, S) f_{flux}(\theta, \phi, LET) \} \quad (1)$$

and it can of course be applied to compare the single event error rates of different circuit cells, and different layouts for the same circuit.

However, it also provides a lot of additional information, which is not accessible from measurements, such as the detailed current and voltage waveforms in the circuit during the single event and information about where in the layout the errors were generated. The latter information, the sensitive regions, make up the cross-section map of the circuit,  $\sigma_{map}(\theta, \phi, LET, S)$ .

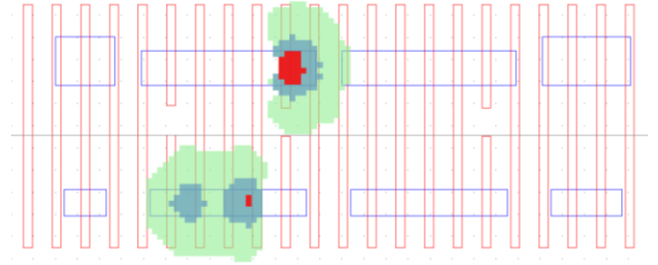


Fig. 3. Example of a cross-section map showing the sensitive regions for normal incidence  $(0^\circ, 0^\circ)$  and LET values 2 (red), 20 (blue), and 100 (green) for a certain circuit state in a flip-flop cell.

#### A. Multi-bit upset prediction

The cross-section maps are helpful in understanding the single event behavior of a particular layout, but are strictly not required for the calculation of error-rates of the individual cell. They can, however, be used very efficiently to predict multibit error-rates. As illustrated in Figure 4, the cross-section for multibit upset (as a function of angle and LET), for two, or more cells, placed at certain positions can simply be evaluated by finding the overlap of the cross-section regions of the cells.

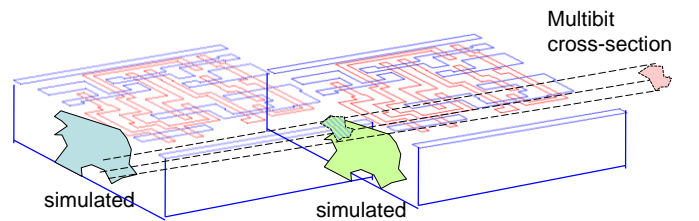


Fig. 4. Illustration of multiple-cell cross-section calculation. For every direction the overlap of the cross-section regions (for the specified criteria for each cell) is calculated to give the overall cross-section of the ensemble of cells (here for the criterion 'cell0 AND cell2').

Since the simulation generation of a cross-section map does require considerable computation resources, it is essential to have a way to interpolate the cross-sections between angles, i.e., not just an interpolation of the cross-section value, but of the actual sensitive regions. The tool Accuro [2] provides such a feature. It utilizes all information from all simulated angles in order to generate the maps (sensitive regions) for all other angles. Figure 5 illustrates this capability showing two

interpolated cross-section maps at  $(60^\circ, 30^\circ)$  and  $(60^\circ, 60^\circ)$  generated from simulated maps at  $(60^\circ, 0^\circ)$  and  $(60^\circ, 90^\circ)$  (shown in the figure) and  $(0^\circ, 0^\circ)$ ,  $(90^\circ, 0^\circ)$ , and  $(90^\circ, 90^\circ)$ .

While this map interpolation is a quite complex process, it is, of course, very much faster than the generation of the simulation results for the original simulated angles. The generation of an interpolated cross-section map takes at most a few seconds per angle, and can easily generate a full cross-section map with a high angle resolution.

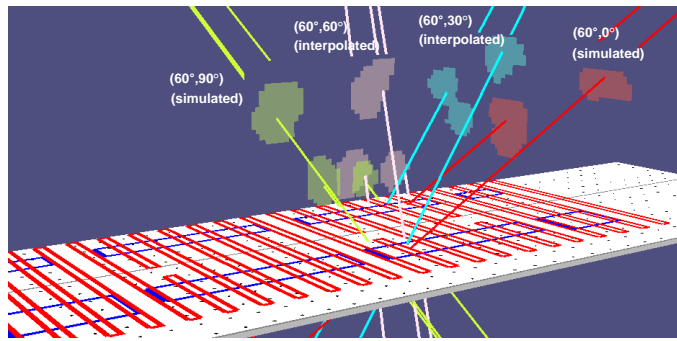


Fig. 5. Illustration of map interpolation including interpolated cross-section maps at  $(60^\circ, 30^\circ)$  (cyan) and  $(60^\circ, 60^\circ)$  (grey).

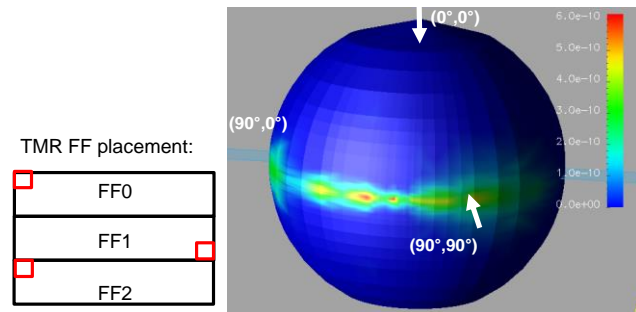


Fig. 6. Example of the cross-section (color-coded as a function of angle) of a TMR FF placement (left) of 3 flip-flops as a function of angle for a certain state (here state1) and LET (here  $20 \text{ MeVcm}^2\text{mg}^{-1}$ ).

An application example of the cross-section interpolation and multibit prediction is shown in Figure 6. Here three flip-flops in a triple modular redundancy (TMR) configuration are placed in different positions relative to each other (one of which is shown in the figure), and the upset is determined by the condition that at least two of the flip-flop are upset (which would upset the TMR). As can be seen in the figures, the cross-section for the TMR configuration is zero (blue color) at normal incidence, and the only contribution comes from radiation with tilt angles close to  $90^\circ$

#### IV. SELECTED COMPARISONS TO MEASUREMENTS

The accuracy of the simulation technique has been verified extensively against single event measurements in bulk technologies from 180-20nm, and SOI technologies from 45-28nm. Figures 7 shows an example from a 28nm bulk

technology and Figure 8 show a comparison for unique measurement data taken at  $91^\circ$  tilt angle in a PDSOI technology.

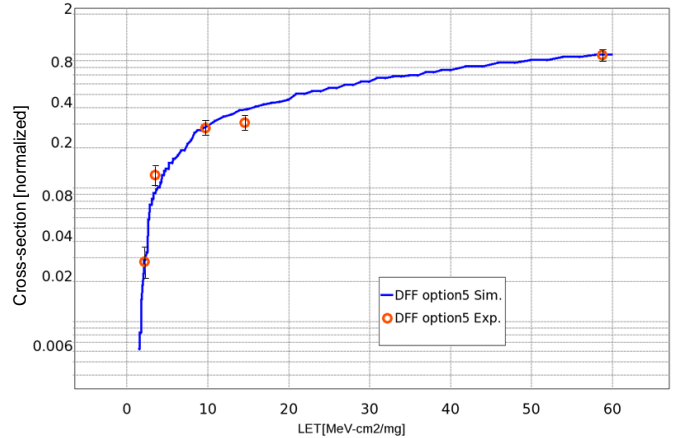


Fig. 7. Normalized experimental data (markers) and simulation (line) for a regular (not redundant) DFF in 28nm bulk technology [1].

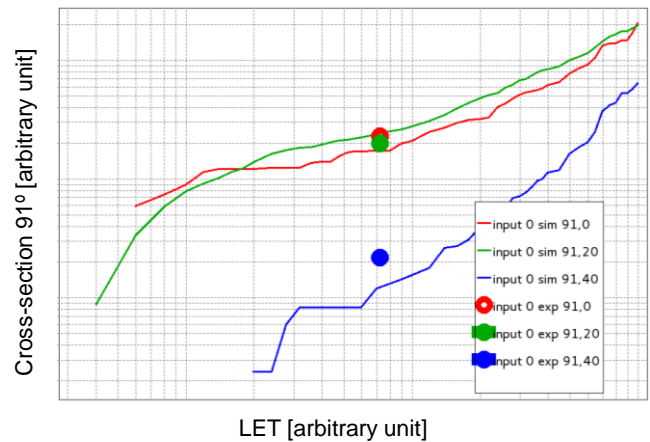


Fig. 8. Comparison of sim. and measured cross-sections for a DICE type flip-flop in 32SOI ( $91^\circ$  tilt,  $0^\circ$   $20^\circ$   $40^\circ$  rotation, nominal supply voltage, blanket pattern 0). Data from [4].

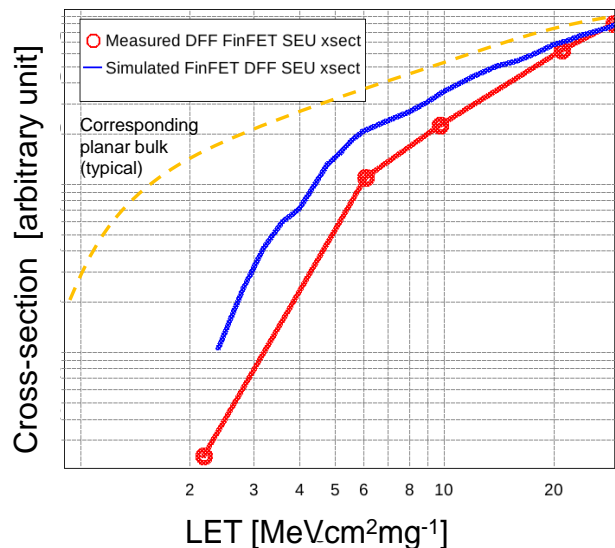


Fig. 9. Comparison of (un-calibrated) simulated and early measured results for the cross-section of a DFF in 16nm bulk FinFET technology [5].

At the 16nm and 14nm FinFET technology nodes comparisons to early measurement data indicate that the basic (un-calibrated) simulation model gives a decent agreement, but that there are deviations at low LET values (Figure 9).

## V. RHBD TECHNIQUES: LEAP

Perhaps an even more important aspect than the error rate prediction is the support the advanced single event simulation provides for the design and optimization of efficient radiation hardened cells, and other basic building blocks. In the development and optimization of ultra-hard logic cells using the Layout design through Error Aware Positioning (LEAP) technique [1][6][7], discussed in this section, the advanced simulation has provided critical information and insight.

The fact that a single event, in an advanced technology, affects many devices and circuit nodes does not only create problems; it can actually be utilized as a hardening technique which can provide extraordinary error rate reductions. The LEAP method takes advantage of the charge sharing by rearranging the layout and the placement of the devices.

LEAP is applicable to sequential logic, combinational logic, as well as other applications (e.g., analog). The penalties in area, speed, or power can be kept very small. The technique is particularly effective for circuits and layouts that use redundancy where consistent error rate reductions of 100X or more (vs. a traditional layout implementation for the same redundant circuit), has been obtained in bulk, SOI, and FinFET technologies from 180nm to 16nm (resulting in three to four orders of magnitude error rate reductions vs. regular (not-hardened) logic).

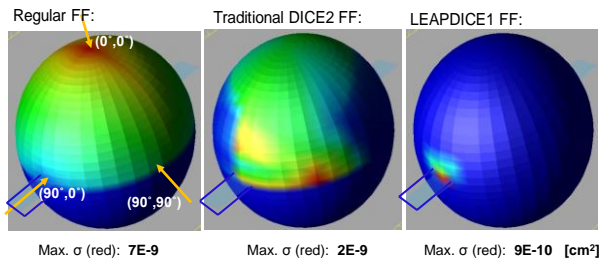


Fig. 10. Spherical plot of the cross-section as a function of incoming angle at an LET of  $16 \text{ MeVcm}^2\text{mg}^{-1}$  in 28nm technology.

Figure 10 illustrates how LEAP can reduce both the solid angle of incidence where the circuit is sensitive to radiation, and the value of the cross-section at the most sensitive direction. The left-most figure shows the cross-sections for the (non-redundant) DFF. This flip-flop can be upset at any angle of incidence, with a maximum cross-section at normal incidence and the smallest cross-section at a grazing angle along the long side of the layout ( $\theta=90^\circ$ ,  $\varphi=0^\circ/180^\circ$ ). The center figure shows the cross-sections for the traditional DICE flip-flop. At  $\text{LET}=16 \text{ MeVcm}^2\text{mg}^{-1}$  the maximum cross-section for this FF is at  $\theta=90^\circ$ ,  $\varphi=325^\circ$ , but it has non-zero

cross-section at normal incidence. The right figure shows the LEAPDICE, where the LEAP technique has reduced the non-zero cross-section to a small angle cone around  $\theta=90^\circ$ ,  $\varphi=0^\circ/180^\circ$  for all LET values.

### A. LEAP at low supply voltage conditions

Figure 11 shows recent SEU measurement results for redundant flip-flops implemented with and without the LEAP technique. These early measurement results have a very poor statistics (and further measurements are under way), but they indicate (along with initial results in other technologies) that the LEAP technique maintains its' efficiency down to very low supply voltages and makes it a good candidate for the generation of logic for Near Threshold Computing (NTC) applications.

Cross-section normal incidence, blanket 0, at  $V_{DD}=0.8\text{-}0.55V$

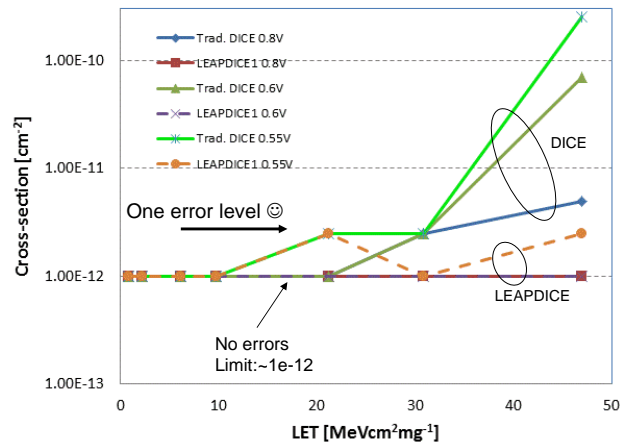


Fig. 11. Early measured SEU cross-section of a regular-layout, and LEAP-layout, DICE flip-flops at different supply voltages in an advanced FinFET technology [5].

### B. LEAP flip-flops and logic

Custom LEAP flip-flops, and certain other logic, have been generated and applied in many different semiconductor technologies (and tested – confirming the extraordinary error rate reductions). Table I provides an overview.

Table 1. Overview of LEAP based logic cells.

Technology	Implemented / Exp. Verified Type	SER reduction	Status / Availability
180nm bulk	LEAP FFs	10000X	Test chip & custom impl.
28nm bulk	LEAP FFs	5000X	Test chip & custom impl.
20nm bulk	LEAP FFs	5000X	Test chip verif.
32nm PDSOI	LEAP FFs, LOGIC	4000X	9T std. cells <sup>1)</sup>
28nm FDSOI	LEAP FFs, LOGIC		Test chip verif.
16nm FinFET	LEAP FFs	5000X	Test chip verif.
14nm FinFET	LEAP FFs, LOGIC	5000X <sup>2)</sup>	9T std. cells <sup>3)</sup>
<sup>1)</sup> FFs (Scan, P, C), clk-tree buffers			
<sup>3)</sup> FFs (Scan, P, C), buffers - testing and test chips in progress 2016			



For an efficient application in today's most advanced technologies, where, as discussed in the introduction, there is little room for customization, LEAP hardening is preferably introduced in form of basic pre-qualified building blocks (standard cells and certain other IP) which seamlessly can be inserted in the design flow alongside other (not hardened) circuitry. Such IP is now available in some advanced technologies (and in the process of being qualified).

## VI. APPLICATION TO COMBINATORIAL LOGIC

The advanced simulation technique can be applied effectively to the analysis of single event transients (SET) in combinatorial logic. By changing the "event" criterion to monitor the SET pulse and recoding the pulse widths during the simulation, cross-sections and error (pulse-) rates which are functions of the SET pulse width are generated in the same manner as the SEU cross-sections and error rates.

Under most circumstances the combinatorial logic gives a much lower contribution to the overall single event error rates (than memory and sequential logic) and is not the primary target for hardening. However, the efficiency of the LEAP RHBD technique for the hardening of combinatorial logic has been experimentally verified for a number of different combinatorial logic circuits [8][9][10].

## VII. APPLICATION TO ANALOG AND OSCILLATORY CIRCUITS

The advanced simulation technique is directly applicable to analog and oscillatory circuits as well (with an appropriate modification of the "event" criterion, e.g., to monitor SET pulses or frequency and phase distortions). However, if the circuit response is complex, requires long simulation times, and introduces additional variables (e.g., the event time-point for oscillatory circuits), the generation of a complete cross-section function and map may become to time consuming.

## CONCLUSION

Advanced simulation techniques can capture the complexity of a single event response in today's most advanced

semiconductor technologies, and provide accurate predictions for single event cross-sections and error rates. The simulation provides critical support for design of hardened electronics in these technologies. The single event behavior in these technologies requires new or modified approaches to radiation hardening. The LEAP RHBD technique is an example of such a technique and its' extraordinary efficiency has been verified experimentally down to the 16nm FinFET technology node.

## ACKNOWLEDGMENT

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