

Development of a Satellite TV receiver for fibre optic distribution system

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Abstract

In this paper we highlight the design work performed by Riverbeck Ltd on the Romeo and Juliet chipset paid for by Global Invacom and the European Space Agency.

Romeo and Juliet are application specific integrated circuits developed as the receiver element of a satellite TV, terrestrial TV and FM radio fibre distribution system. Fibre distribution of media signals is particularly attractive to multi-dwelling units where any TV or radio channel can be demanded by any dwelling. This requires the entire signal bandwidth be provided to all dwellings. A fibre system reduces the infrastructure cabling, is immune to electrical interference, suffers from less signal loss and can be passive split without detriment to reception.

The fibre distribution transmitter (not within scope of this paper) frequency shift and modulates terrestrial radio, TV, and satellite signal using a 1310 nm semiconductor laser.

Romeo and Juliet amplify the received photodiode signal, filter and frequency shift the 5GHz bandwidth to provide a set top box with the same data were it directly connected to a LNB. Romeo is a dual gain, low noise amplifier with differential outputs. Juliet provides broadband programmable RF gain, wideband continuous time filters to clean up the output spectrum, RF power detectors, 75Ω and 50Ω line driver outputs, phase locked loops to frequency shift the received spectrum, monitoring circuits and digital interfaces.

I. INTRODUCTION

European satellite television is broadcast in Ku band between 10.7 - 12.75GHz using two polarisations providing 4.1GHz bandwidth [1]. The bands are named vertical low (VL), vertical high (VH), horizontal low (HL) and horizontal high (HH). Within each band TV channels are broadcast as phase modulated transponders where each transponder is ~30MHz.

Historically the distribution of TV channels has been realized by F type coax, but the cable bandwidth is less than the signal bandwidth. To allow arbitrary channel choice multiple parallel cables are installed. A historic installation is shown in figure 2.

To reduce the coax cabling in single occupancy but multi tuner homes manufacturers now offer digital channel stacking (DCS) technology [2]. DCS reduces the coax cabling requirements but limits the number of TV channels concurrently available. By comparison fibre optic distribution of TV provides all channels to all users concurrently and removes the electrical limitations of coax cabling.

The proposed architecture shown in Figure 1 radically changes the satellite IF architecture. The conventional satellite TV LNB is replaced with an optical LNB that frequency stacks all satellite bands 950MHz – 5.45GHz onto a fibre optic cable (In additional terrestrial TV and radio can be stacked onto the fibre optic at <800MHz). At the receiver the satellite bands are moved to their original frequency locations so the frequency stacking is transparent to the set top box (STB).

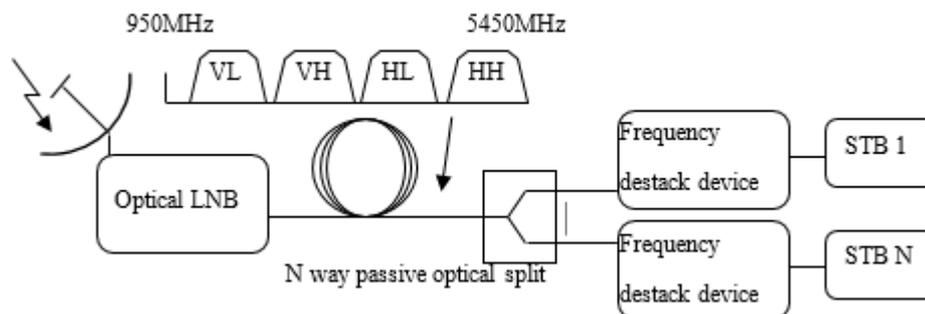


Figure 1: Proposed Satellite television distribution system

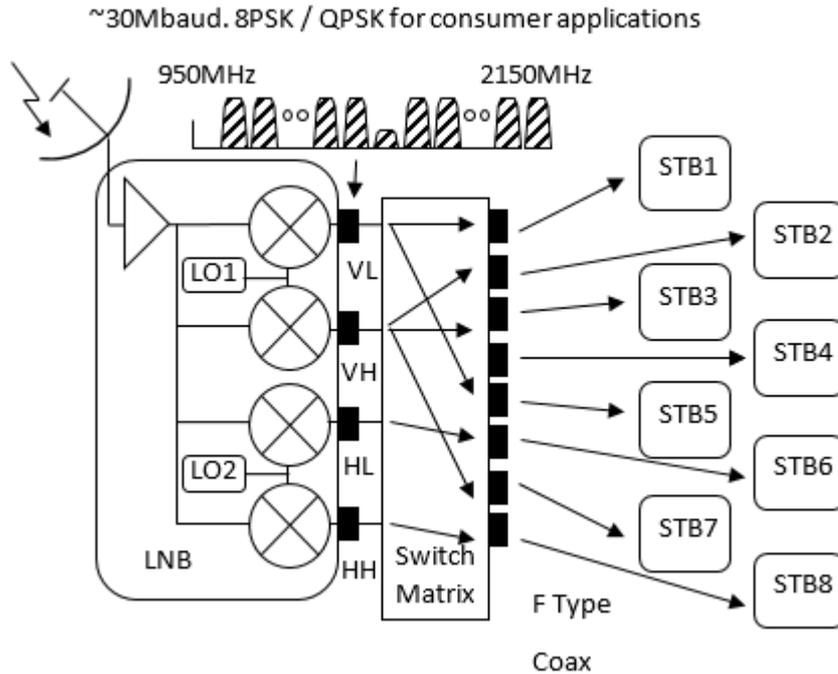


Figure 2: Legacy Satellite television distribution system

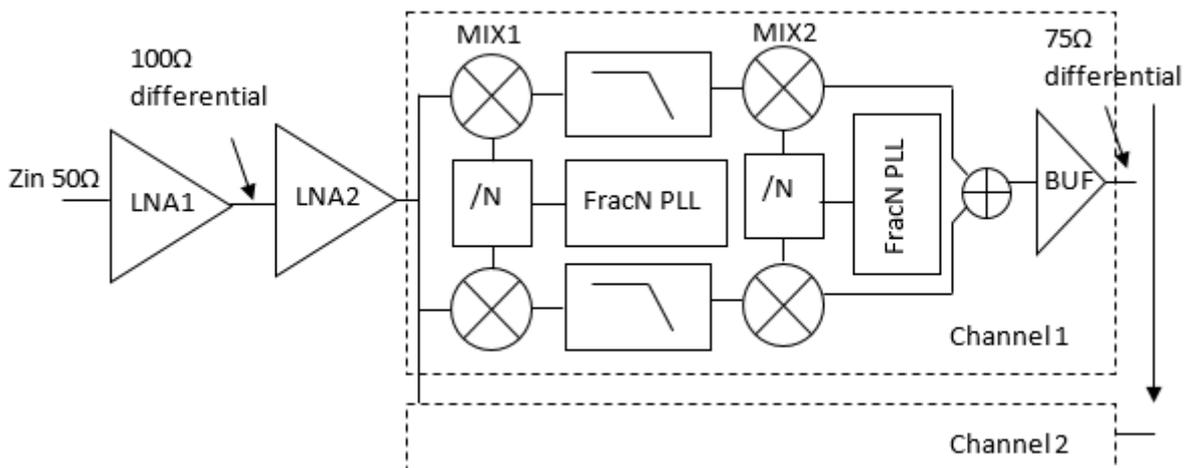


Figure 3: Block Diagram of Frequency destack device

Figure 3 shows a block diagram of the chipset architecture. It is a two integrated circuit solution implemented in 180nm BiCMOS. Whilst both integrated circuit were implemented in the same technology LNA1 is a separate device to improve electrical isolation. Between the devices is a pair of 100 Ω differential microstrip lines. The overall gain is programmable from 15 dB – 45 dB, see Figure 5.

On the main integrated circuit is a homodyne receiver with 1GHz complex IF bandwidth, programmable gain stages and continuous time channel filters followed by a homodyne transmitter. By mixing down the signal to baseband and up converting to the output frequency the lowest order channel filter to meet the attenuation requirements can be implemented. The architecture also allows the frequency shift to be defined by the difference in mixer local oscillator (LO) frequencies.

Integrated low phase noise, but wide frequency tuning fractional N, LC PLLs provide the LO requirements.

The output buffer provides -18dBm at 4dBm OIP3 into 75 Ω via a 1:1 balun to drive a STB. An output balun improves electrical isolation and removes common mode mixer energy from the output spectrum.

Figure 3 shows the main integrated circuit is a two channel device. Either output can output any band (VL, VH, HL or HH) to the STB.

II. LNA

The low noise amplifier (LNA) is a dual gain amplifier. The amplifier is constructed from two parallel input stages with different gains and a common output stage. Depending on the

gain selection, the appropriate amplifier is enabled. The inactive amplifier has high input impedance when off and does not affect the active amplifier.

A simplified schematic of the high gain amplifier is shown in Figure 4. The input transistor and main amplifying transistor is Q0. A cascaded device Q1 reduces the voltage gain of Q0 to reduce miller effect of Q0 cbc. R0 is the load resistor. Q2, and Rfb form a negative feedback loop that define the input impedance $Z_{in}=R_{fb}/(1+A)$. The LNA return loss is better than 10dB from 50MHz – 5.45GHz.

The low gain LNA is a similar design except Q0 has series feedback to reduce gain and provide higher linearity but has higher noise figure.

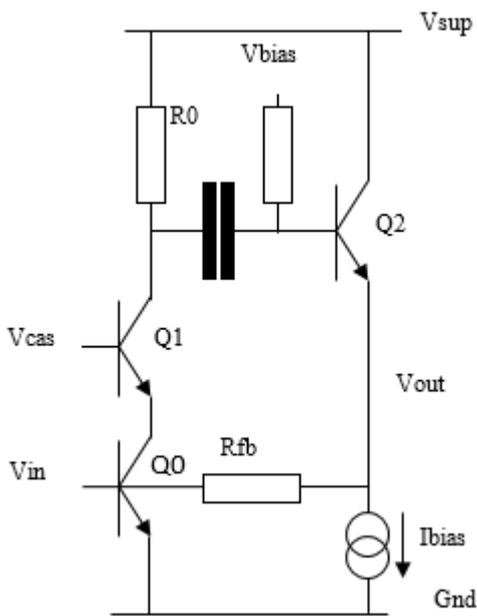


Figure 4: LNA Schematic

III. PGA AND GAIN CONTROL

On chip RF log power detectors measure the total input power and power in bands VL VH, HL and HH. The power detector measurements are digitised and drive a single loop digital gain control loop.

The overall gain is the sum of gain blocks LNA1, LNA2, MIX1, MIX2 and BUF in Figure 3. These cells provide high resolution gain control that maximises system signal to noise ratio over process, voltage and temperature variations Rain fade affects received power level but can be tracked as the effect is a slow time constant.

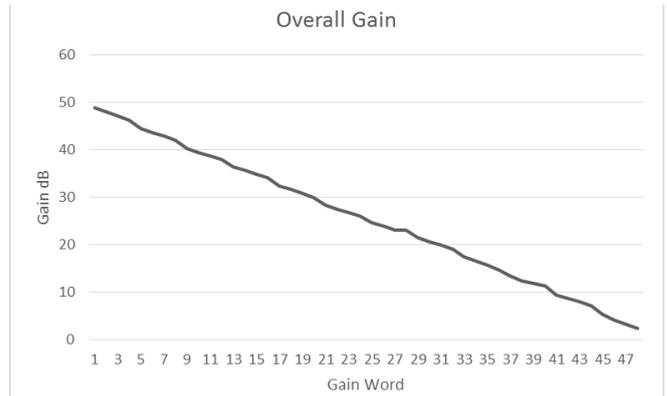


Figure 5: Overall Gain versus Gain Word

IV. LC VCO, PLL AND FREQUENCY PLAN

Due to the wide frequency spacing of VL, VH, HL and HH bands the MIX1 LO must tune 1.45GHz - 4.925GHz. MIX2 LO must tune 1.45GHz – 1.625GHz.

To reduce the oscillator tuning range (and silicon area) the oscillators were designed to run at 2x and 4x LO frequency. The MIX1 LO tuning frequency range remains too large for a single VCO so the additional tuning range is implemented as an oscillator array with overlapping frequency coverage. A negative resistance NMOS LC oscillator topology was selected for each oscillator as shown in Figure 6. Periodic noise analysis showed significant phase noise contributed by the bias network and to remove this a large external capacitor was added to the design. Phase noise is typically -90 to -95 dBc at 100KHz offset from the LO frequency.

During the PLL lock time, a search algorithm selects the lowest phase noise VCO when multiple oscillators oscillate at the target frequency.

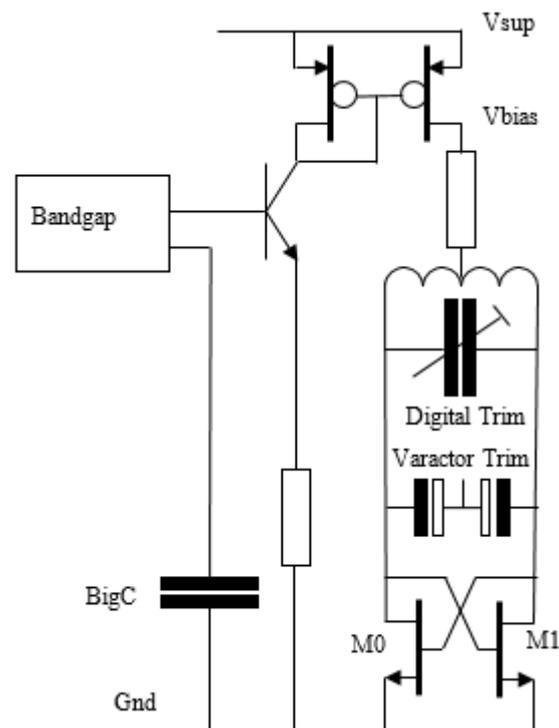


Figure 6: VCO Topology

The digital trim provides coarse frequency VCO tuning whilst the varactor controlled by the charge pump and PLL loop dynamics provides fine frequency tuning.

The high speed PLL dividers are implemented as CML logic and the low speed dividers in CMOS. The overall PLL architecture is a conventional Type II charge pump design.

When both channels are active, four LC VCO PLLs operate concurrently. If two VCO frequencies are within $\sim 10\text{MHz}$ of each other the PLL loop dynamics interact and cause catastrophic in band spurs [3]. In this application we mitigate this issue as the frequency shift is controlled by the difference in LO MIX1 and LO MIX2 and not the absolute frequency of either LO. Software is used to detect potential clashes and move LO frequencies.

V. CHANNEL FILTER

The Channel filter is a 3rd order transconductance capacitance (gmC) filter with cut off frequency tunable from 500MHz – 720MHz. The filter is trimmed by measuring the frequency of a slave oscillator constructed from the same components as the filter. The transfer function is shown in Figure 7.

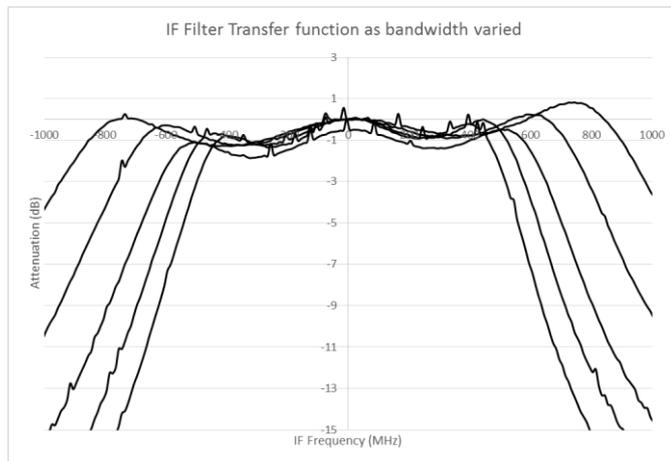


Figure 7: IF Filter Transfer Function

The gmC filter transconductance cell is implemented using resistively degenerated long tail pairs with current source loads. In Figure 8 M0, M1, R3 and R4 provide the current load and common mode feedback. Transistors Q0 and Q1 are degenerated by R1 and R2 respectively.

Many high frequency gmC filters use Nauta's gm cell [4], but in this technology the bipolar ac performance is far superior to the CMOS.

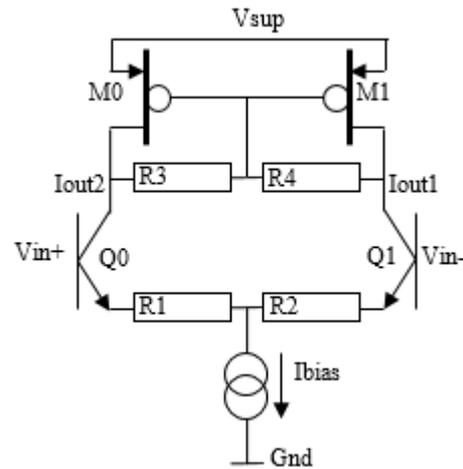


Figure 8: Transconductor Schematic

VI. CONCLUSIONS

In this paper we present a new method to distribute satellite TV signals within multi dwelling buildings. The solution provides the entire signal bandwidth to all users at all times.

As demand for satellite TV bandwidth grows due to introduction of more high definition and ultra high definition content we expect this technology to be widely adopted.

This development is a great example of silicon up integration. Analogue blocks that historically required many discrete components can now be realised as a system on chip.

VII. ACKNOWLEDGEMENTS

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VIII. REFERENCES

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