DiReRa
New Rad-Hard Chip-Set for Radiometers

AMICSA 2016
Outline

- Radiometer Architecture
- Requirements and Frequency Plans
- IC Process Constraints and Requirements
- DiReRa Chip-Set: RF Front-End
- DiReRa Chip-Set: AD-Converter
- Measurement Results
- Radiation Hardening – TID
- Radiation Hardening – Heavy Ions
- Conclusions and Road Map
Full H-V polarimetric radiometer – TRYO Aerospace.

Measures both H and V polarizations at the same time.

DiReRa chip-set is shown in orange. It consists of:

→ L-band RF front-end.
→ Dual-channel 1-bit AD-converter (comparator).
IC – Reduce size and power consumption considerably.
Maintain compatibility with existing LICEF-3 radiometer.
Isolation between channels is critical.
RF bandwidth = 20MHz, flatness = ± 0.1-0.2dB.
Support different frequency plans.

<table>
<thead>
<tr>
<th>No.</th>
<th>RF Frequency</th>
<th>LO Frequency</th>
<th>IF Frequency</th>
<th>Sampling Freq.</th>
<th>Note</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>1200-1600 MHz</td>
<td>1180-1580 MHz</td>
<td>25-35 MHz</td>
<td>130 MHz</td>
<td>ESA SoW.</td>
</tr>
<tr>
<td>2</td>
<td>1413.5 MHz</td>
<td>1396 MHz</td>
<td>17.5 MHz</td>
<td>55.84 MHz</td>
<td>TA – LICEF-3.</td>
</tr>
<tr>
<td>3</td>
<td>1413.5MHz</td>
<td>1384.65MHz</td>
<td>28.85MHZ</td>
<td>115.38MHz</td>
<td>TA – SMOSops.</td>
</tr>
<tr>
<td>4</td>
<td>1200-1600 MHz</td>
<td>1167.5-1567.5 MHz</td>
<td>32.5 MHz</td>
<td>130 MHz</td>
<td>As 1, centered.</td>
</tr>
<tr>
<td>5</td>
<td>1200-1600 MHz</td>
<td>1037.5-1437.5 MHz</td>
<td>162.5 MHz</td>
<td>130 MHz</td>
<td>As 1, higher IF.</td>
</tr>
<tr>
<td>6</td>
<td>1413.6 MHz</td>
<td>1288 MHz</td>
<td>125.6 MHz</td>
<td>55.84 MHz</td>
<td>As 2, higher IF.</td>
</tr>
</tbody>
</table>
IC Constraints and Requirements

**Constraints**

- Single process must fit everything.
- Limited component types and values, large tolerances, but excellent component matching.
- **Coupling** via common substrate and pins.

**Requirements**

- Proper GHz RF performances (dominant requirement).
- Rad-hard – can be radiation hardened.
- Available in small quantities – a few 100 dies yearly.

**AMS S35 – 0.35µm HBT BiCMOS process.**

- Use differential signal paths.
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RF Downconverter ASIC

Architecture

- Single conversion superheterodyne, active mixer.
- Balanced signal path (except LNA), 50Ω RF, 600Ω IF.
- High Z local oscillator port and good mixer isolation:
  → Bridging is possible.
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RF Downconverter ASIC

Layout and Test Fixture

- Size: 1280μm x 1200μm.
- 42 pads, bonded to 40 pins.

- QFN test plastic package.
- JEDEC MO-220, VJJD-5
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AD-Converter ASIC

Architecture

- Dual channel 1-bit AD-converter (dual comparator).
- Latched regenerative architecture (high sens., low power).
- 0-1 imbalance $\leq 0.5\%$: critical.
- Direct and muxed outputs with deglitching circuit (compatible with existing LICEF-3 baseband processor).
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AD-Converter ASIC

Layout and Test Fixture

- Size: 610µm x 880µm.
- 16 pads, bonded to 16 pins.
- QFN test plastic package.
  JEDEC MO-220, VGGC-2
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### Measured Results

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Value</th>
<th>Unit</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DiReRa RF Front-End</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LNA gain</td>
<td>High gain setting</td>
<td>18.3</td>
<td>dB</td>
<td>Noise matched, 50Ω.</td>
</tr>
<tr>
<td></td>
<td>Low gain setting</td>
<td>6.5</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>LNA noise figure</td>
<td>High gain setting</td>
<td>1.7</td>
<td>dB</td>
<td>Noise matched, 50Ω.</td>
</tr>
<tr>
<td></td>
<td>Low gain setting</td>
<td>2.3</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Mixer SSB voltage gain</td>
<td>Balanced input, 50Ω</td>
<td>14.7</td>
<td>dB</td>
<td>Balanced output, no load.</td>
</tr>
<tr>
<td>Mixer SSB noise figure</td>
<td></td>
<td>12.3</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>IF-strip gain range</td>
<td>TIF output</td>
<td>23.5-81.6</td>
<td>dB</td>
<td>PGAs+VCA, balanced, no load.</td>
</tr>
<tr>
<td>IF-strip PGA gain step</td>
<td></td>
<td>1</td>
<td>dB</td>
<td>Balanced I/Os, no load.</td>
</tr>
<tr>
<td>IF-strip VCA gain range</td>
<td>VC=0V to 2V</td>
<td>12</td>
<td>dB</td>
<td>Maximum gain is limited.</td>
</tr>
<tr>
<td>Output 1dB compr. point</td>
<td>PNS output, no load</td>
<td>−4.5</td>
<td>dBu</td>
<td>Referred to 600Ω.</td>
</tr>
<tr>
<td><strong>DADC 1-bit AD-converter</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sampling frequency</td>
<td>Maximum</td>
<td>130</td>
<td>MHz</td>
<td>Operates from ~0Hz to 130MHz.</td>
</tr>
<tr>
<td>DC-offset</td>
<td>Input referred</td>
<td>±3.7</td>
<td>mV</td>
<td>Measured at DC, 2 samples.</td>
</tr>
<tr>
<td>0-1 imbalance</td>
<td>−4dBu, −40 to 125°C</td>
<td>0.5</td>
<td>%</td>
<td>Band-limited AWGN.</td>
</tr>
</tbody>
</table>
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**Radiation Hardening – TID**

- **TOTAL DOSE** – Objective: \( \geq 1 \text{kGy(Si)} [100 \text{krad(Si)}] \).
- **Effects** – MOS: Vt shift, leakages; BJT: \( \beta \) degradation.

- Strongly process dependent, no way to predict ELDRS.
  - But – AMS S35 is already well tested (SY10x7 devices):
  - TD > 1kGy at 0.12Gy/min.

- Some circuit/layout tricks:
  - Differential stages:
    - Vgs shifts will compensate.
  - High current or active bias circuits:
    - Allow for \( \beta \) reduction.
  - Layout techniques.

\[
\begin{align*}
V_{GS} & \quad M1 \quad V_{GS} \\
M2 & \quad \text{D} \quad \text{G} \quad \text{S} \\
\text{Ib} & \quad \text{D} \quad \text{G} \quad \text{S}
\end{align*}
\]
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Radiation Hardening – SEL

- **HEAVY IONS** – Objective: \( \text{LET} \geq 85\text{MeV} \cdot \text{cm}^2/\text{mg} \).

SEL is potentially destructive. Some SEL-tolerant techniques:
- Continuous uninterrupted guard rings.
- Good distributed substrate/well contacts.
- Silicon on Insulator (SOI) – but beware TID effects.

- SEL at \( \text{LET} < 60\text{MeV} \cdot \text{cm}^2/\text{mg} \) requires SEL protection.

![Latch-up circuit](image)

SEL-tolerant layout example
SET/SEU cause noise (analog) or operating errors (digital) but are not destructive. SEE protection *shall not* compromise performance excessively! Some SEE-tolerant techniques are:

- Drive strength hardening (DSH).
- Error correction (ECC, TMR, DICE).
- Glitch suppression, charge storage devices.
- Self-resetting sequential circuits, no dead cycles.
- Fast recovery analog circuits.

- DSH provides *intrinsic protection*, i.e. prevents SEE from occurring, but effectiveness is limited to ~5-15MeV·cm²/mg.
- The other methods *don't prevent* SEE but only correct its effects. LET ≥ 85MeV·cm²/mg can be achieved with ECC or TMR, DICE is ~30-50MeV·cm²/mg (on 0.35μm process).
The DiReRa chip-set has been designed, manufactured and tested with good results, now it should be industrialized:

- Do a preliminary *irradiation test* on current prototypes.
- *Finalize design*, do an engineering run.
- Procure and assemble the *packages*.
- Develop *production screening*.
- Do a *qualification* of the chip-set.
- Prepare all needed *documentation*.

Once these steps are completed the chip-set is ready to be used in a radiometer and will be introduced in Saphyrion's catalogue.
Thank you for your attention