SAPHYRION
communication technologies

DiReRa

New Rad-Hard Chip-Set for Radiometers

AMICSA 2016

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Outline

- Radiometer Architecture
- Requirements and Frequency Plans
- IC Process Constraints and Requirements
- DiReRa Chip-Set: RF Front-End
- DiReRa Chip-Set: AD-Converter
- Measurement Results
- Radiation Hardening – TID
- Radiation Hardening – Heavy Ions
- Conclusions and Road Map

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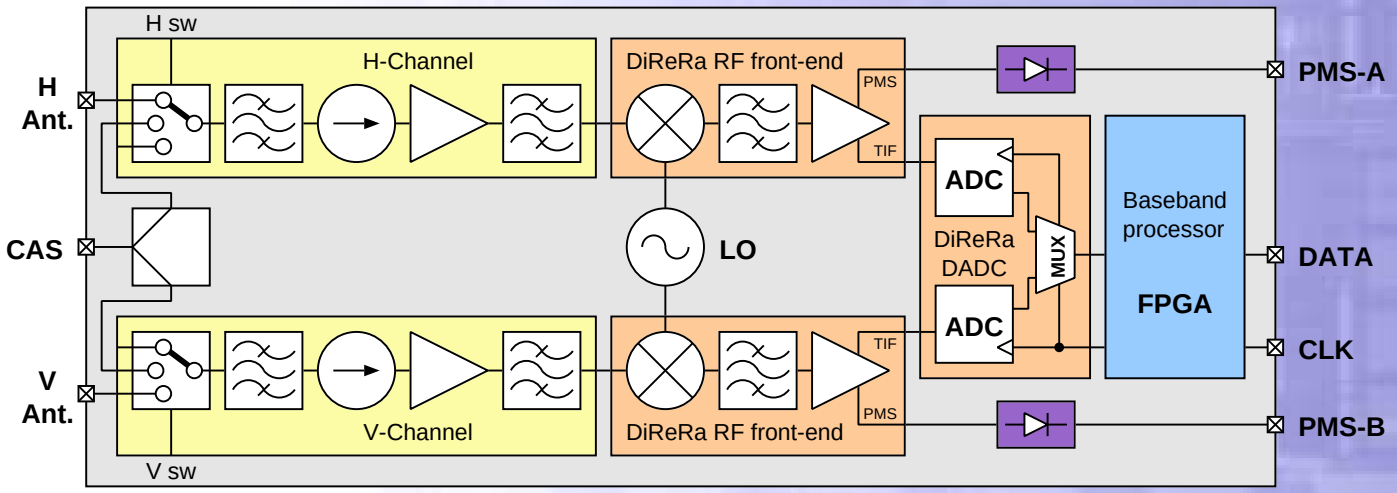
Radiometer Architecture

- Full H-V polarimetric radiometer – TRYO Aerospace.
- Measures both H and V polarizations at the same time.
- **DiReRa chip-set** is shown in orange. It consists of:
  - → L-band RF front-end.
  - → Dual-channel 1-bit AD-converter (comparator).



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Requirements, Frequency Plans

- IC – Reduce size and power consumption considerably.
- Maintain compatibility with existing LICEF-3 radiometer.
- Isolation between channels is critical.
- RF bandwidth = 20MHz, flatness = ± 0.1-0.2dB.
- Support different frequency plans.

No.	RF Frequency	LO Frequency	IF Frequency	Sampling Freq.	Note
1	1200-1600 MHz	1180-1580 MHz	25-35 MHz	130 MHz	ESA SoW.
2	1413.5 MHz	1396 MHz	17.5 MHz	55.84 MHz	TA – LICEF-3.
3	1413.5MHz	1384.65MHz	28.85MHz	115.38MHz	TA – SMOSops.
4	1200-1600 MHz	1167.5-1567.5 MHz	32.5 MHz	130 MHz	As 1, centered.
5	1200-1600 MHz	1037.5-1437.5 MHz	162.5 MHz	130 MHz	As 1, higher IF.
6	1413.6 MHz	1288 MHz	125.6 MHz	55.84 MHz	As 2, higher IF.

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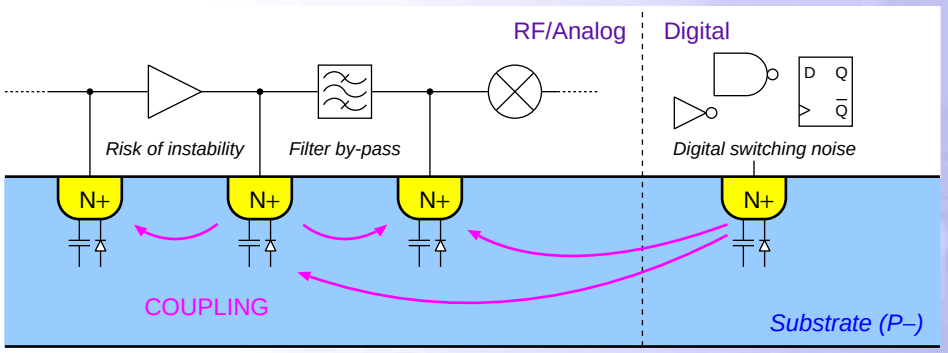
IC Constraints and Requirements

Constraints

- *Single process* must fit everything.
- Limited component types and values, large tolerances, but excellent component matching.
- *Coupling* via common substrate and pins.



► Use *differential* signal paths.

Requirem.

- Proper GHz RF performances (dominant requirement).
- Rad-hard – can be radiation hardened.
- Available in small quantities – a few 100 dies yearly.

► **AMS S35 – 0.35µm HBT BiCMOS process.**

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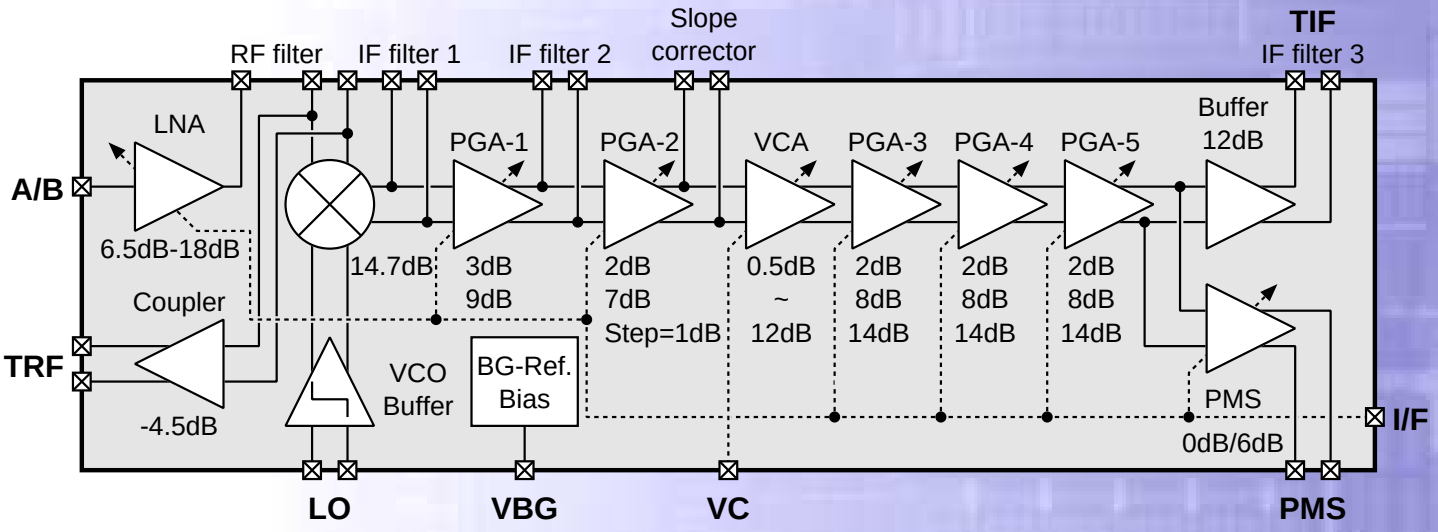
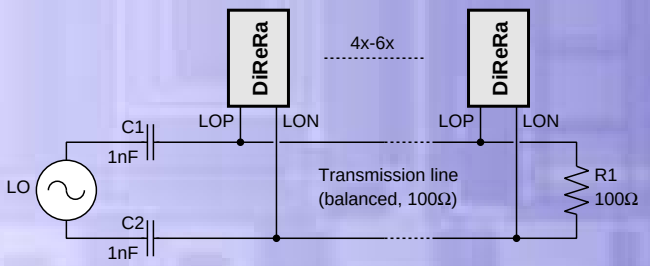
RF Downconverter ASIC

► Architecture



- Single conversion superheterodyne, active mixer.
- Balanced signal path (except LNA), 50Ω RF, 600Ω IF.
- High Z local oscillator port and good mixer isolation:
  → *Bridging* is possible.



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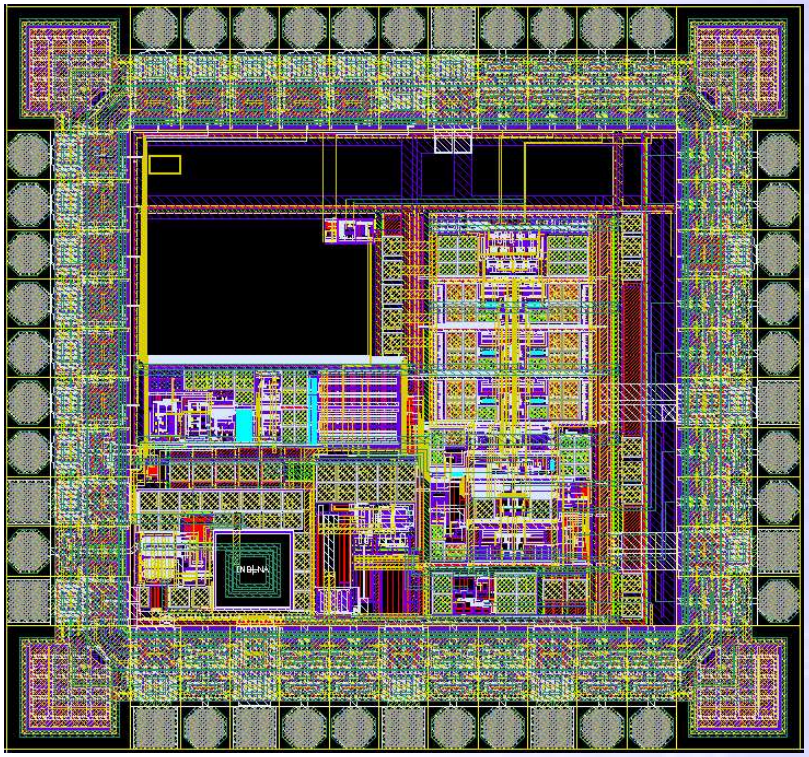
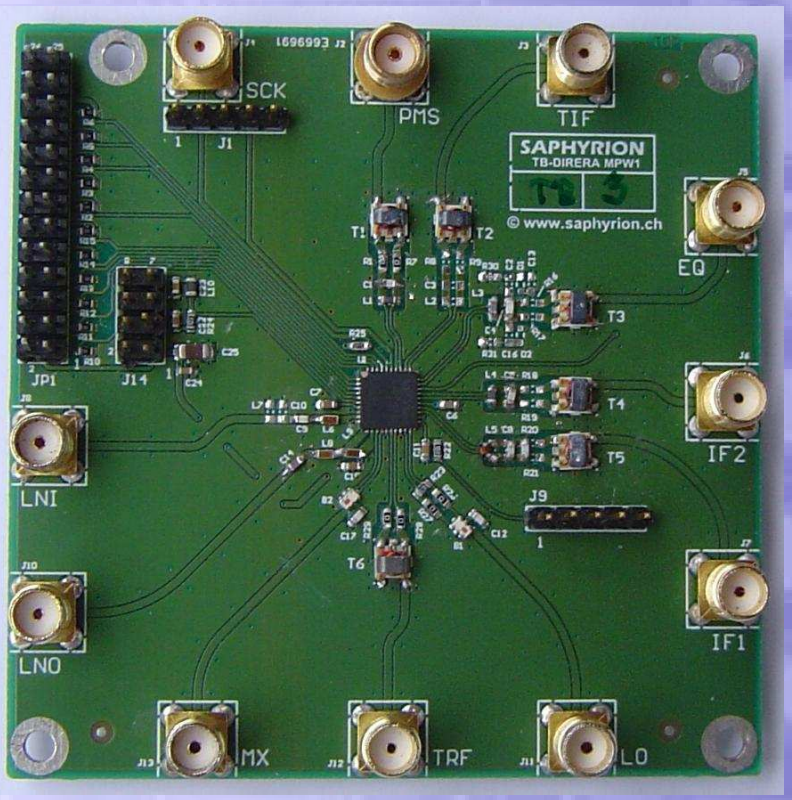
RF Downconverter ASIC

► Layout and Test Fixture





- Size: 1280µm x 1200µm.
- 42 pads, bonded to 40 pins.

- QFN **test** plastic package. JEDEC MO-220, VJJD-5

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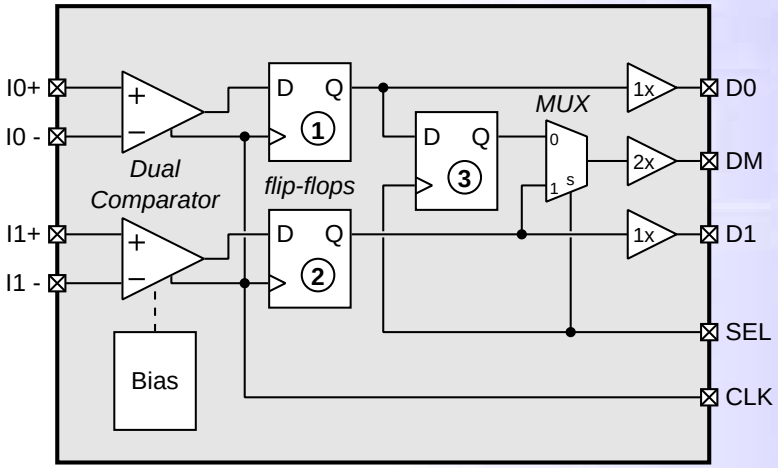
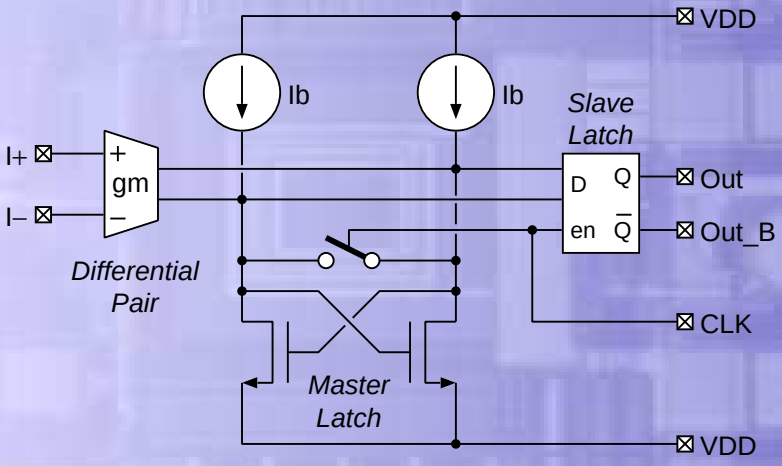
► Architecture





- Dual channel 1-bit AD-converter (dual comparator).
- Latched regenerative architecture (high sens., low power).
- 0-1 imbalance ≤ 0.5%: *critical*.
- Direct and muxed outputs with deglitching circuit (compatible with existing LICEF-3 baseband processor).

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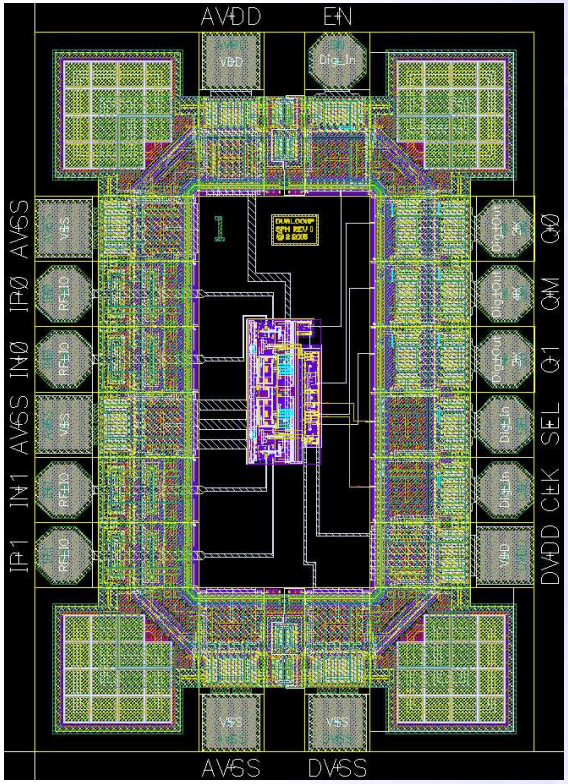
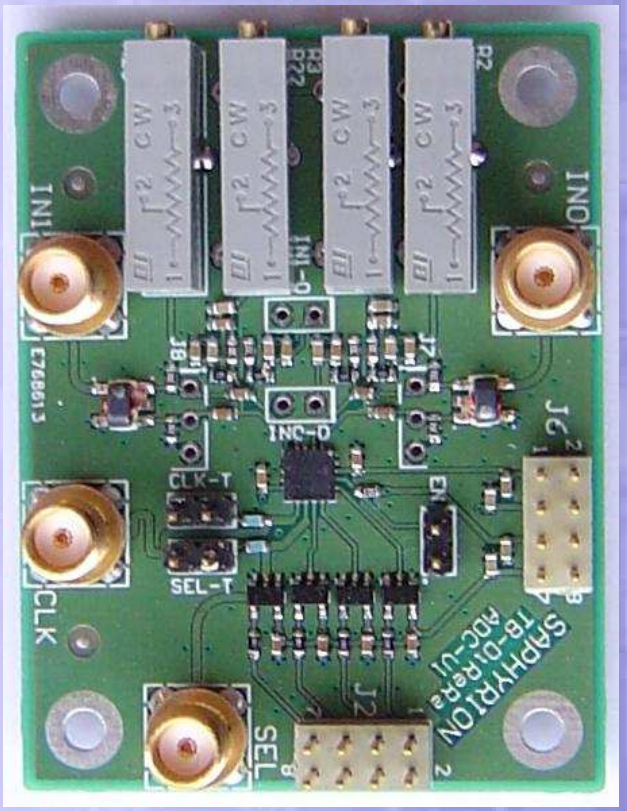
AD-Converter ASIC

► Layout and Test Fixture





- Size: 610µm x 880µm.
- 16 pads, bonded to 16 pins.
- QFN **test** plastic package. JEDEC MO-220, VGGC-2

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Measured Results

Parameter	Conditions	Value	Unit	Notes
DiReRa RF Front-End				
LNA gain	High gain setting	18.3	dB	Noise matched, 50Ω.
	Low gain setting	6.5	dB	
LNA noise figure	High gain setting	1.7	dB	Noise matched, 50Ω.
	Low gain setting	2.3	dB	
Mixer SSB voltage gain	Balanced input, 50Ω	14.7	dB	Balanced output, no load.
Mixer SSB noise figure		12.3	dB	
IF-strip gain range	TIF output	23.5-81.6	dB	PGAs+VCA, balanced, no load.
IF-strip PGA gain step		1	dB	Balanced I/Os, no load.
IF-strip VCA gain range	VC=0V to 2V	12	dB	Maximum gain is limited.
Output 1dB compr. point	PNS output, no load	−4.5	dBu	Referred to 600Ω.
DADC 1-bit AD-converter				
Sampling frequency	Maximum	130	MHz	Operates from ~0Hz to 130MHz.
DC-offset	Input referred	±3.7	mV	Measured at DC, 2 samples.
0-1 imbalance	−4dBu, −40 to 125°C	0.5	%	Band-limited AWGN.

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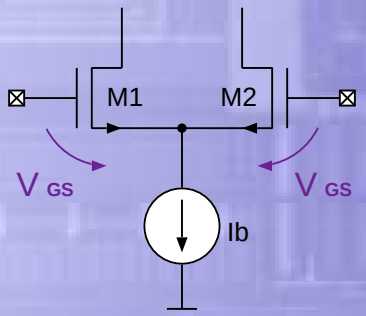
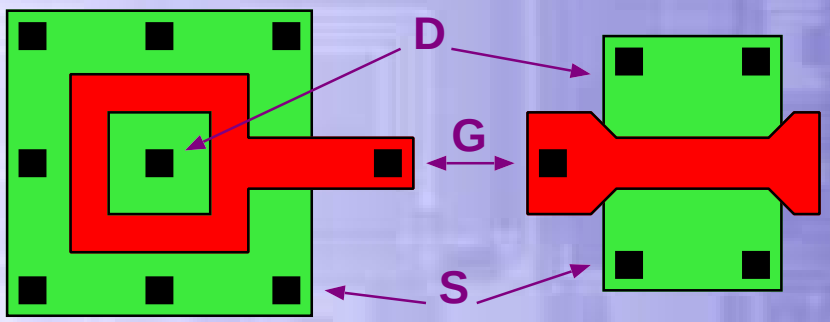
Radiation Hardening – TID

- **TOTAL DOSE** – Objective: ≥ 1kGy(Si) [100krad(Si)].
- Effects – MOS: Vt shift, leakages; BJT: β degradation.

➢ Strongly process dependent, no way to predict ELDRS.
But – AMS S35 is already well tested (SY10x7 devices):
→ TD > 1kGy at 0.12Gy/min.

➢ Some circuit/layout tricks:
→ Differential stages:
- Vgs shifts will compensate.
→ High current or active bias circuits:
- Allow for β reduction.
→ Layout techniques.





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Radiation Hardening – SEL

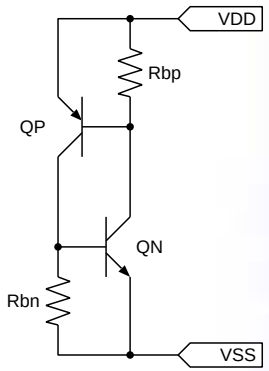
- **HEAVY IONS** – Objective: LET ≥ 85MeV·cm²/mg.

SEL is potentially destructive. Some SEL-tolerant techniques:

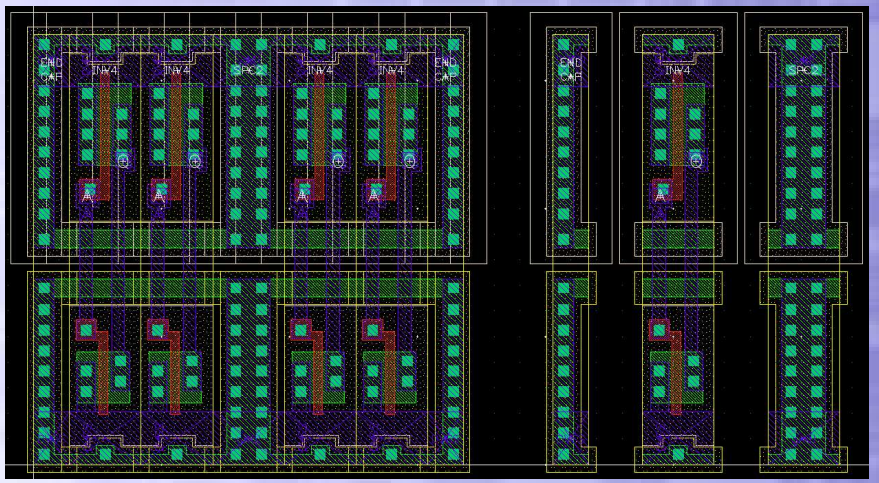
- Continuous uninterrupted guard rings.
- Good distributed substrate/well contacts.
- Silicon on Insulator (SOI) – but beware TID effects.

- SEL at LET < 60MeV·cm²/mg *requires* SEL protection.

Latch-up circuit



SEL-tolerant layout example



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Radiation Hardening – SET/SEU

SET/SEU cause noise (analog) or operating errors (digital) but are not destructive. SEE protection *shall not* compromise perf-ormance excessively! Some SEE-tolerant techniques are:

- Drive strength hardening (DSH).
- Error correction (ECC, TMR, DICE).
- Glitch suppression, charge storage devices.
- Self-resetting sequential circuits, no dead cycles.
- Fast recovery analog circuits.

► DSH provides *intrinsic protection*, i.e. prevents SEE from occurring, but effectiveness is limited to ~5-15MeV·cm²/mg.

► The other methods *don't prevent* SEE but only correct its effects. LET ≥ 85MeV·cm²/mg can be achieved with ECC or TMR, DICE is ~30-50MeV·cm²/mg (on 0.35µm process).

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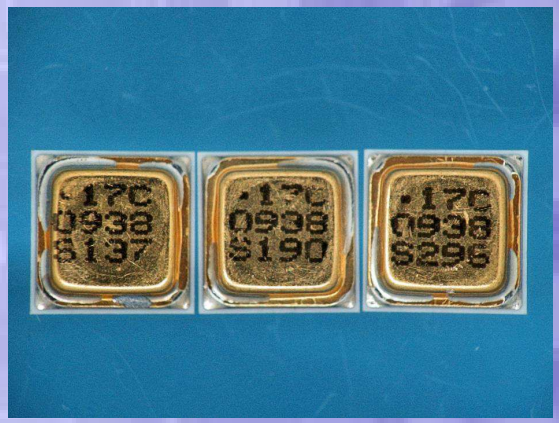
Conclusions, Road Map

The DiReRa chip-set has been designed, manufactured and tested with good results, now it should be industrialized:

- Do a preliminary *irradiation test* on current prototypes.
- *Finalize design*, do an engineering run.
- Procure and assemble the *packages*.
- Develop *production screening*.
- Do a *qualification* of the chip-set.
- Prepare all needed *documentation*.



Once these steps are completed the chip-set is ready to be used in a radiometer and will be introduced in Saphyrion's catalogue.

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Thank you for your attention

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