DESIGN METHODOLOGY FOR MIXED SIGNAL ASIC WITH PREQUALIFIED ANALOG IPS

FOR SPACE APPLICATIONS

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Abstract

Mixed Analog / Digital System on Chip are increasing drastically in space equipment to reduce cost, power and dimensions and to improve performances.

The challenge for mixed SoC is to get a qualified product without heavy SEE or TID testing. As for a digital library, analogue cells and their combinations, High voltage LDMOS, regulators (to allow single supply) and latch-up protections must be "pre-qualified".

The qualification of IOs and digital is done by using a Standard Evaluation Circuit covering at least half of the maximum of transistor of an ASIC.

For the analog part all blocks must be validated. In addition, in order to check the "integrability" of the building blocks towards the elaboration of a complex space-adequate System-on_Chip, a complex function will be realized embedding all individual analog cells and a digital block embedded as an analog cell.

During the realization of this complex function emphasis is given to the observability and testability of the individual building blocks. For each new analog cell the same process must be conducted. The study will continue by determining the observability of the analog nodes and specifically the eventual propagation of Single Event Transient.
This study is conducted with support of ESA and CNES and with European industrial partners.

ATMEL ATMX150RHA offers a wide range of capabilities to enlarge the SoC integration: digital integration up to 20M gates, NVM, analogue, 3Gbit serial interface, N and P deep well, Deep Trench to isolate blocks, handle Wafer contact, 1.8V digital core, 3V, 5V, 15V and high voltage up to 60V. Mixing power, high voltage and high speed on a single chip needs adequate packaging technology, large die and small die must be handled by different packaging solutions: double pad ring, flipchip, Au bonding, Al bonding.

ATMEL can base the qualification for space requirements on standard process used in high volume. It ensures longer process lifetime and stability, as well as lower access cost. Same advantages applies to probe, assembly and final test. A mixed Standard Evaluation Circuit is under definition in order to check the "integrability" and "space testability and observability" of the building blocks.

The flow and the rules for integration of analogue cells coming from multiple suppliers will be clearly defined and qualified.

I. DESIGN FLOWS

I.1. DK description

The ATMX150RHA DK contains a complete set of tools, models, utilities and technology files for Place & Route environment and documentation.
It includes

- Libraries
  - Libraries for Design For Testability
  - Error Detection And Correction source code and testbenches
  - Topological libraries used by Synopsys tools
  - Compiled & Source libraries for Design Compiler Synthesis tool
  - Utilities for ATPG tool
  - Verilog & VHDL/VITAL models for cells, buffers and memories
- Tools
  - Atmel Tool Box & Freeware
  - Package Interface Management
  - Virage RAM / ROM compilers

I.2 PDK description

The ATMX150RHA PDK contains the hardening design rules. Transistors are characterized for the military temperature range (-55°C, +125°C).

It includes

- Analog cells
- Design rules
- Encrypted RHBD IOs netlists

Atmel plans to deliver Encrypted IP's with test files separately, through Atmel Design centers (see §4.2).

I.3. ASIC DEVELOPMENT FLOW

I.3.1. Standard Flow

Standard flow is when customer wants a full digital ASIC or uses Atmel analog IP's, he does not design any analog blocks. In such case, customer has to download the DK, encrypted IP netlist are provided separately. Customer designs its ASIC using ATMX150RHA RHBD library and analog IP blocks, providing Atmel with a synthetized netlist. Atmel is in charge of the Place & Route and verifications. *Figure 1* shows the design flow from DSR to DR with shared responsibilities.
This development phase is concluded by a Design Review (DR) meeting, involving Customer and Atmel. The objective of the Design Review is to validate the entire circuit database and the physical design. The main checked criteria are the simulation results with post-layout, back annotation timings, the layout organization with bonding diagrams and package features and the test program in compliance with Atmel tester rules.

At this step, customer has to provide Atmel with test vectors and burn-in program as well as ASIC marking.

A soon as the DR document is signed off, the manufacturing of the masks set and wafers lot start. 5 validation prototypes and 5 industrialization prototypes (*see appendix 1- prototypes definition*) are delivered to customer for ASIC validation on board.

I.3.2. Analog Flow

Customer wants a full analog ASIC, he designs its own analog blocks and potentially uses Atmel catalog IP's. In such case, customer has to download DK and PDK, encrypted IP netlist are provided separately. The development flow is as described in *figure 2*, Atmel will start from GDSII and run a DRC/ARC/LVS.
This development phase is concluded by a 'light' Design Review (DR) meeting, involving Customer and Atmel. The objective of the Design Review will depend on the Atmel services requested by customer.

- Foundry only: to confirm the DRC/ARC/LVS checks and freeze the schedule for wafer/dice delivery
- If Assembly service option: to freeze the package/pinout
- If Probe/test service option: to provide Atmel with test patterns.

A soon as the DR document is signed off, the manufacturing of the masks set and wafers lot start.

I.3.3. Digital or Analog on top

Customer wants a mixed-signal ASIC and will design its own analog blocks and potentially uses Atmel catalog IP's. In such case, customer has to download DK and PDK, , encrypted IP netlist are provided separately. The development flow will be as described in *figures 3 & 4*. Atmel manages the digital part (P&R, verifications, Cross-talk, IR drop, parasitics extractions…). If analog on top, Digital .LEF is provided to customer for top-layout and if digital on top, Analog .LEF is provided to Atmel for P&R.
This development phase is concluded by a Design Review (DR) meeting, involving Customer and Atmel. The objective of the Design Review is to validate the entire circuit database and the physical design. The main checked criteria are the simulation results with post-layout, back annotation timings, the layout organization with bonding diagrams and package features and the test program in compliance with Atmel tester rules. At this step, customer has to provide Atmel with specification to test analogue blocks and burn-in program as well as ASIC marking.
A soon as the DR document is signed off, the manufacturing of the masks set and wafers lot start. 5 validation prototypes and 5 industrialization prototypes (*see appendix 1- prototypes definition*) are delivered to customer for ASIC validation on board.

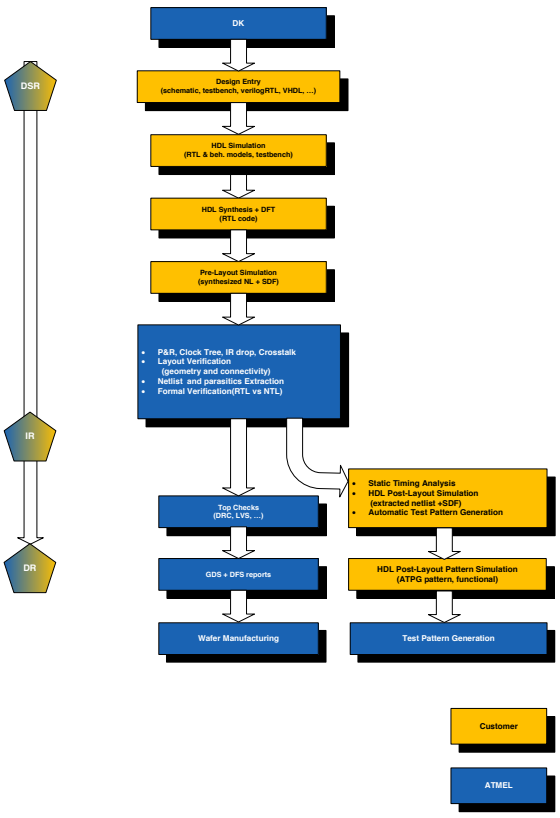

Figure 1: Development flow for digital ASIC or ASIC with Atmel pre-qualified analog IP's

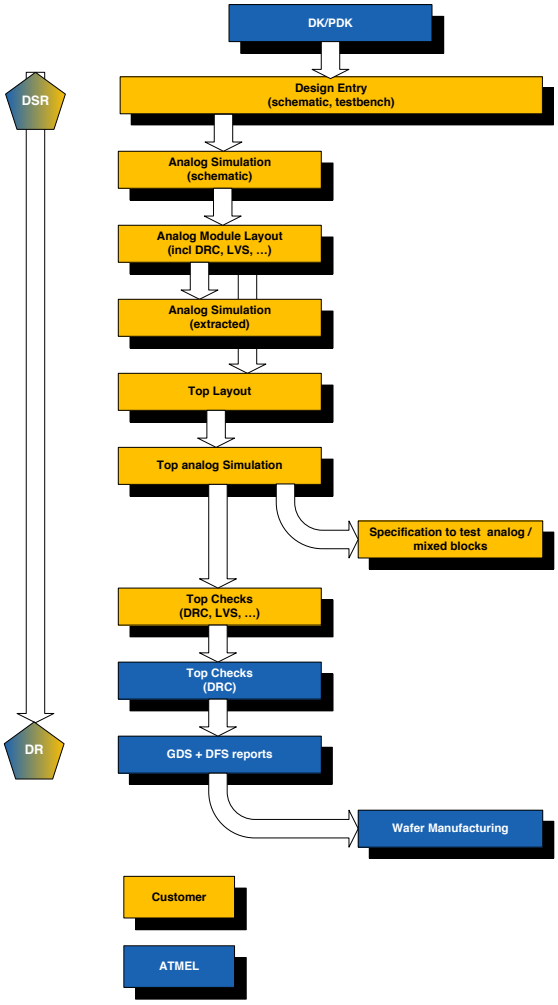

Figure 2: Development flow for analog ASIC

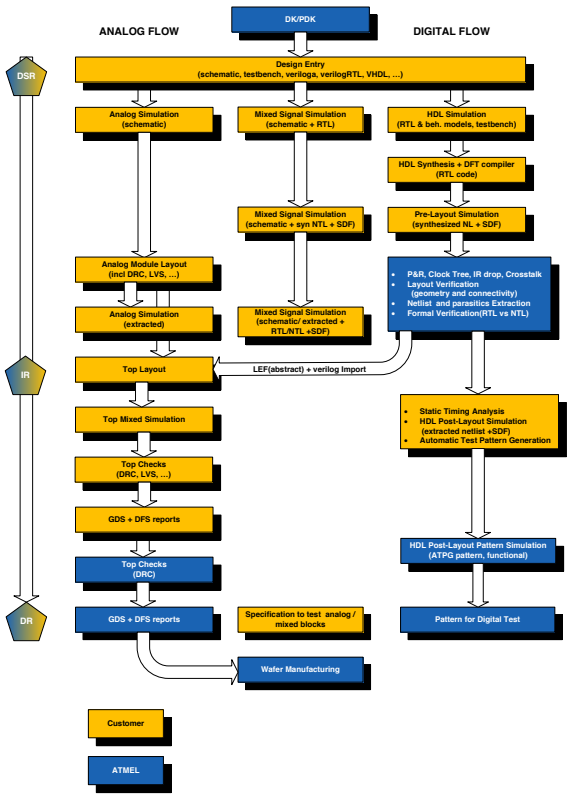

Figure 3: Development flow for analog-on-top ASIC

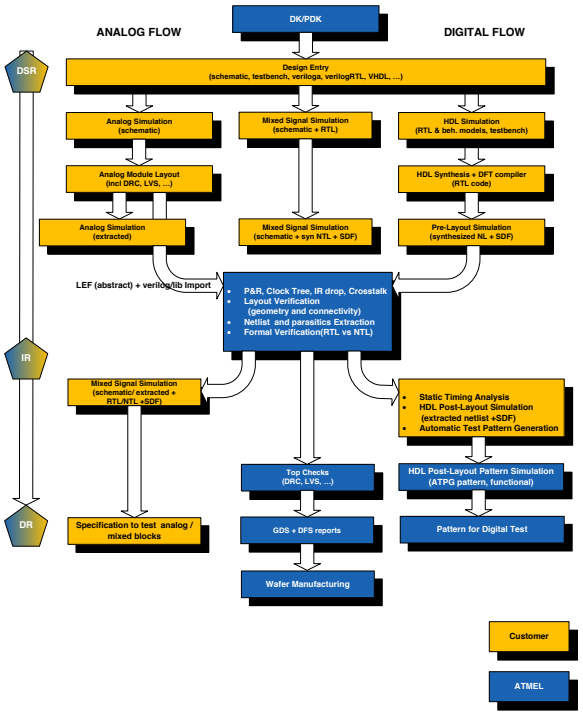

Figure 4: Development flow for digital-on-top ASIC

II. DIGITAL RADIATION STATUS

ATMX150, digital, has been tested against radiation TID, SEL and SEU. Radiation Report is available under NDA signature for users of thee technology. The overall results are on line or better than the previous technology ATC18RHA.

III. ANALOG RADIATION DESIGN

The analogue cells are tested as elementary cells in a test chip allowing individual test of each cell and the test of the combination of the cells. Electrical characterisation will be finished end of 2016. Radiation test results will be available in H2/2017. The analogue cells are listed below:

IP name	Functionality	Main characteristics/interest
	Linear Voltage regulator	Linear 5.5V/2.7V to 1.8V 50mA
	Oscillator	10MHz +/- 10%
	PLL	40-450MHz
	Bandgap	1.25V
IORHA	**IO library (Full digital + analog) up to 5,5 V**	Programmable digital buffer ESD protection enhanced Performance (frequency) enhanced Reduced cell number
MUX8RHA	**Analog Multiplexer**	8 channel 10MHz bandwidth
REG200RHA	**Linear Voltage regulator (including a POR)**	5.5V/2.3V to 1.8V @200mA
OSCRC10RHA	**Clock Generator / Oscillator**	Programmable 4/8/10/12 MHz RC oscillator
PLL400MRHA	**Clock Generator / PLL**	PLL 8/200MHz to 40/450MHz
BG1V2RHA	**Voltage reference / BandGap**	1.25V bandgap voltage reference
HERMES	**Clock Generator**	3GHz clock generator based on injection locked oscillator
	Clock Generator / Oscillator	32kHz xtal oscillator (ascosc138)
	Clock Generator / Oscillator	20MHz xtal oscillator (ascosc136)
	Clock Generator / Oscillator	32kHz RC oscillator (ascrc091)
	I2C filter	Filter for I2C high speed protocol (ascbuffilteterd2)
	Voltage Regulator DC/DC	DCDC 5V to 2.5V 300mA
	PLL	10-200MHz
	ADC	24 bits
	DAC	24 bits
	Voltage Comparator	
	Power On Reset **Low Power Band Gap**	5ms delay

IV. OTHER FEATURES

IV.1. NVM

A 32kBytes NVM is under electrical and radiation qualification.

IV.2. HIGH VOLTAGE LDMOS

The 15V IO is using standard CMOS transistor.

ATMEL has develop 25V, 45V and 65V LDMOS. Transistors. Radiation characterisation is ongoing. It is the plan to develop full IOs with ESD ELT production. Based on

V. ASIC & ASSP PLATFORM

Using this flow an example of the use of this development platform is started for an ASSP as described the below figure. Starting form a validated architecture of a processor core with its bus matrix (dark blue), ATMEL can derives new version adding digital IPs using the libraries (light Blue), custom IPs (middle blue) and NVM or analogue block. The blue to green system control block on the left includes voltage regulators, PLL, oscillators, power management …

VI. CONCLUSION

ATMX150, digital, has been tested against radiation TID, SEL and SEU. Radiation Report is available under NDA signature for users of thee technology. The overall results are on line or better than the previous technology ATC18RHA.

The prequalified analogue IPs give a safer result and so limit the risk of re-spin. The integration of the analogue, NVM and HV with the digital improve drastically the overall cost.

An RF front end will be possible to add in the future.

The 150nm keeps an affordable access to the technology.