High Resolution Radiation Hardened DAC in CMOS-SOI Featuring a Return-to-Zero Matrix

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AMICSA 2016, Gothenburg, Sweden

Outline

- **Design**
  - Description
  - Radiation Hardening
  - Digital Part
  - Analog Part
  - Return-to-Zero feature
  - Results
- **Flow**
  - Analog Flow
  - Digital Flow
  - Top Design Flow
- **Conclusions and next steps**

24-bit Digital-to-Analog Converter
DAC24

Specifications

24-bit sigma-delta current steering DAC

Resolution	24 bit
Specified bandwidth	0.1mHz-50kHz
Effective resolution	>18bit
Dynamic Range	> 108dB
Signal-to-Noise Ratio	> 108 dB
Sampling rate	Up to 310 kSps
Monotonicity	Full code range
Power dissipation	62 mW
LET for SEL immunity	≥ 70 MeV/mg/cm^{-2}
SEU immunity	Protection of critical memory cells
SET immunity	Protection of the digital part
TID tolerance	≥100 krad
Temperature range (functional)	-55 °C < T < 125 °C
Temperature range (full performance)	0 °C < T < 50 °C

Timeline evolution

Cut 1.0

DAC2401A

- First release
- STM H9CMOS 130nm techno

Cut 2.0

DAC2401B

(AMICSA 2012)

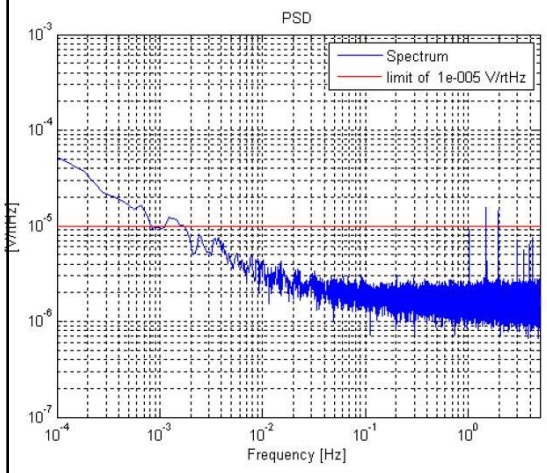
- STM H9CMOS 130nm techno
- Modified input interface

Cut 3.0

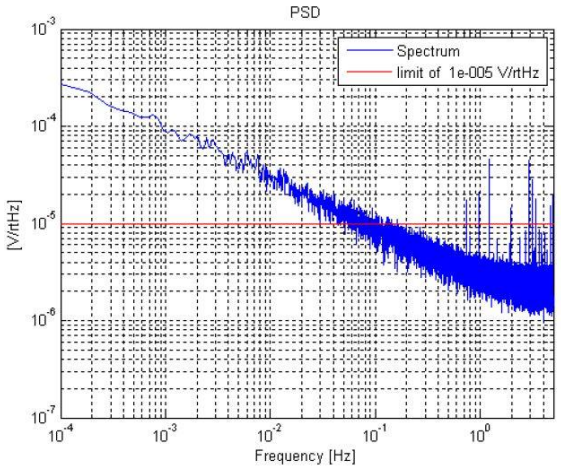
DAC2401C

(AMICSA 2016)

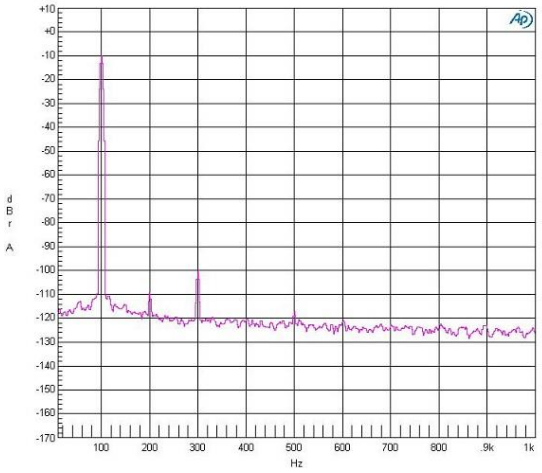
- ATMX150RHA
- Simplified input interface (compatible with ADC2401)
- Single clock architecture
- Configuration through pins
- Embedded IP version
- RTZ analog feature to improve 3rd harmonic distortion



Low freq. noise, 0V input



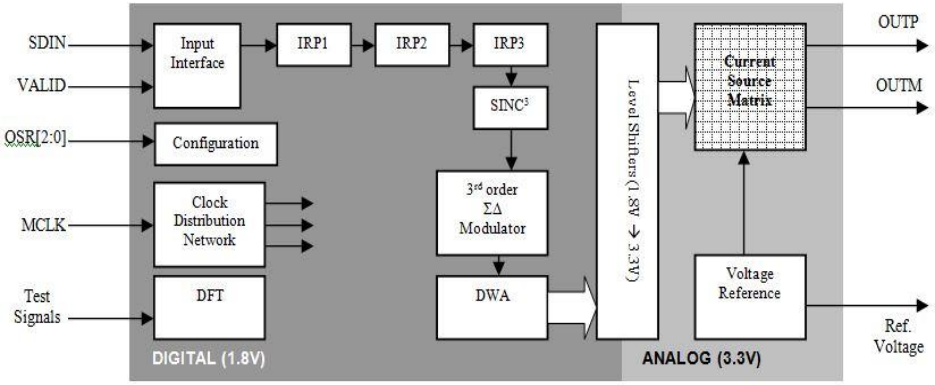
Low freq. noise, DC input



Sine 100Hz -10dBFS FFT

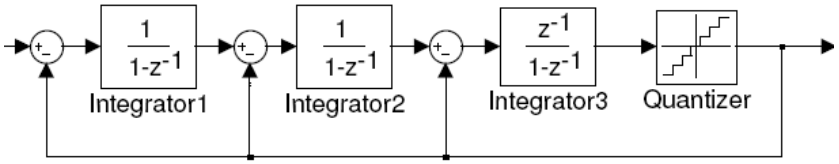
DAC highlights

- **Features**
  - 24-bit resolution
  - multi-bit ΣΔ modulator topology
  - Single clock domain
  - Very low frequency operation
  - Return-to-Zero output stage operation
  - Differential current steering output
  - ΣΔ modulator bypass mode
  - Simple synchronous serial input interface
  - Selectable oversampling ratios allow sampling rates up to 310kSa/s
  - Analog bandwidth from DC to 50kHz
  - 1.8V digital power supply
  - 3.3V analog power supply and I/Os
  - Embedded or external voltage reference
  - Radiation hardened against SEE and TID
- **Applications**
  - High resolution actuator drive
  - High accuracy calibration
  - Servo loop control



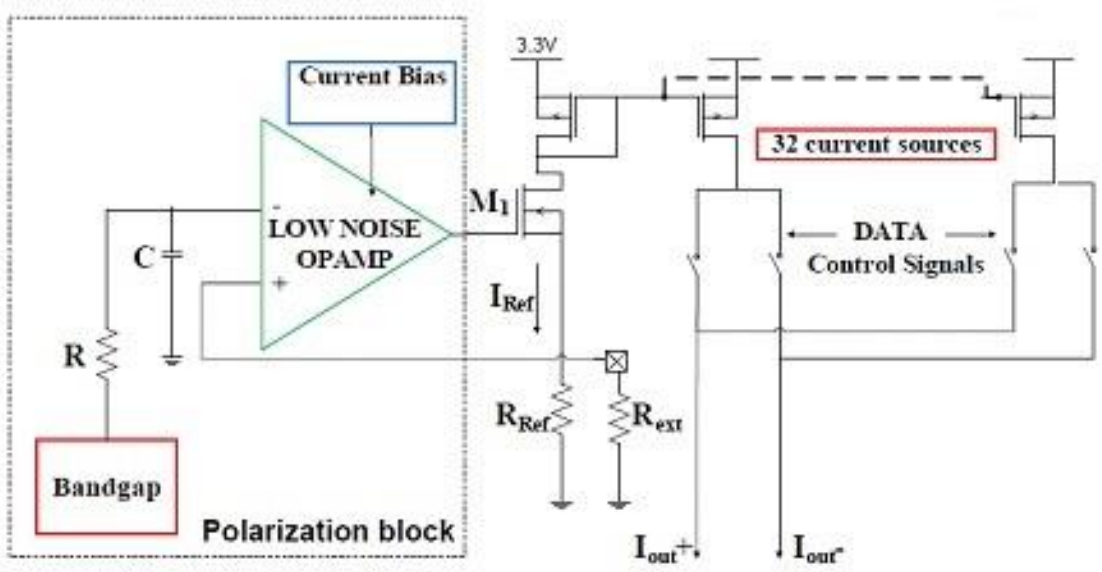
Digital part

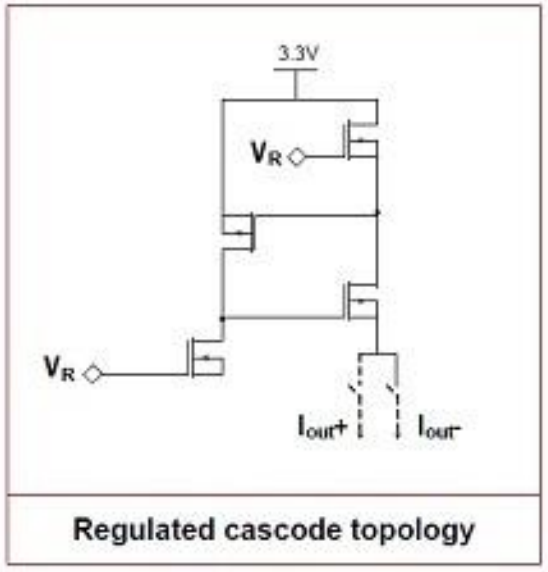
- **Modulator design**
  - 3rd order feed-forward ΣΔ modulator
  - 5-bit quantizer
  - Selectable sampling frequency via control over OSR (x32, x64, x128, x256)
  - Idle Tone avoidance by introduction of dither
- **Dynamic Element Matching (DEM)**
  - The output element mismatch error is minimized by the use of a DEM algorithm.
  - Data Weighted Averaging (DWA) as an efficient DEM algorithm.
  - Algorithm's objective → achieve an equal use of elements in long-term by rotating the output elements (current sources) in a cyclic fashion.
  - DWA uses only one index, which is updated with the addition of the input every clock cycle.



Time	Input	Index	1	2	3	4	5	6	7
1	3	1	■	■	■				
2	2	4				■	■		
3	5	6	■	■	■			■	■
4	6	4	■	■		■	■	■	■
5	2	3			■	■			
6	7	5	■	■	■	■	■	■	■

Analog part

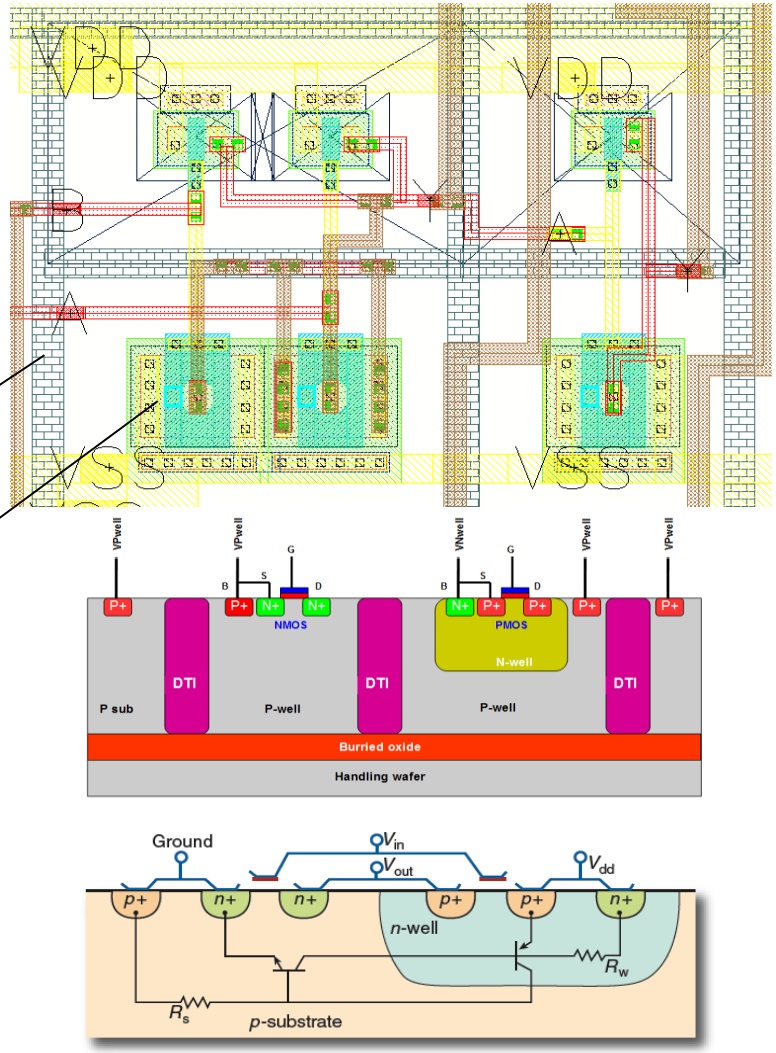


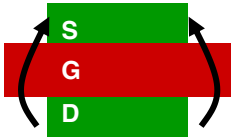


- Bandgap cell provides an accurate reference voltage (1.25V) with a low temperature coefficient.
- First order RC filter reduces any noise from the bandgap block.
- Low noise Op-Amp along with M1 and current setting resistor (Rref or Rext) implements the reference current source for generating the reference current Iref.
- IRef can be set by selecting the internal resistor RRef or connecting an external resistor Rext.
- Differential elementary current sources built around the regulated cascode topology.
- Use of PMOS transistors for lower flicker noise(1/f)

Radiation hardening: analog part

- Deep Trench Isolation (DTI) option cuts away the parasitic structures between PMOS and NMOS that may trigger SEL
- All NMOS transistors are of enclosed layout type (ELT) which greatly improve analog degradation due to TID effects (overconsumption due to severe leakage currents at edge formed parasitic channels)
- Relaxed layout rules
- Decoupling capacitors to eliminate SET in all critical points
- Simulation of SET
- Simulation in 21 corners and MC



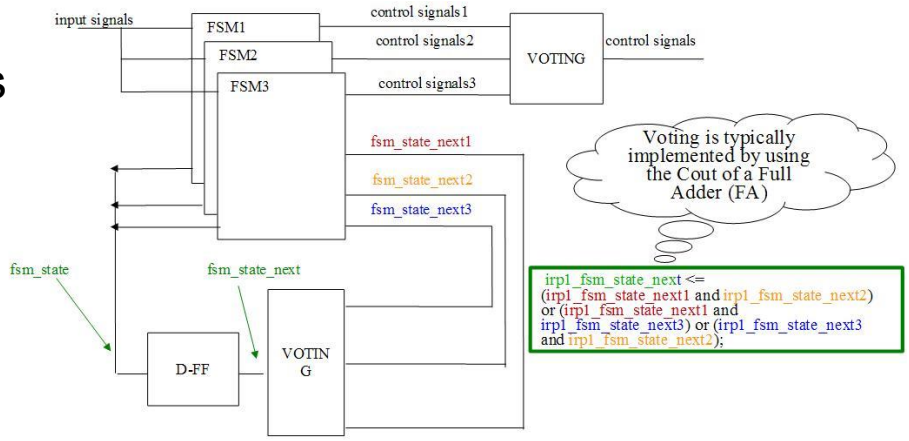


- Radiation induced charges are trapped in the oxides or at Si interface.
- Overconsumption due to severe leakage currents at edge formed parasitic channels may lead to total loss of circuit functionality.

[fig: R. Mauerer, et.all, 2008]

Radiation hardening: digital part

- **Technology level**
  - Atmel AT58K85 0.15 µm is a rad-hard proven technology.
- **Library level**
  - oversized and robust standard cells were used (including latches and flip-flops).
- **Digital design level**
  - Global insertion of TMR logic in FSMs and counters
  - Synchronous reset



RTZ output stage

- **Return-to-Zero functionality to improve linearity**

[3] Adams R., Nguyen Q. K., Sweetland K., A 113-dB SNR Oversampling DAC with Segmented Noise-Shaped Scrambling, *IEEE Journal of Solid-State Circuits, VOL.33, No.12,* December 1998.

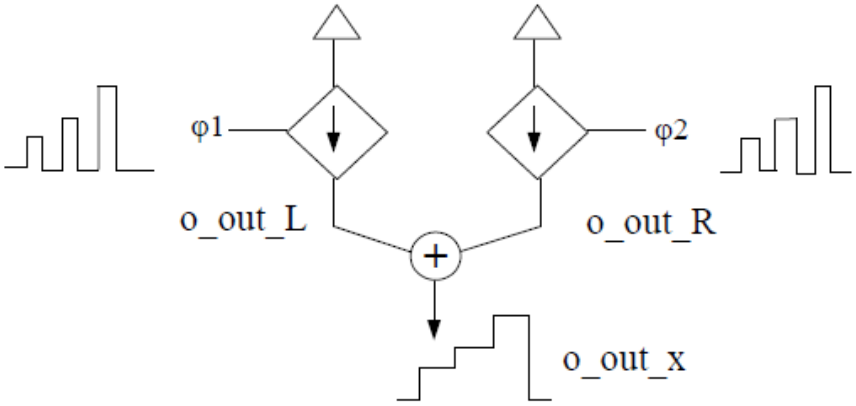
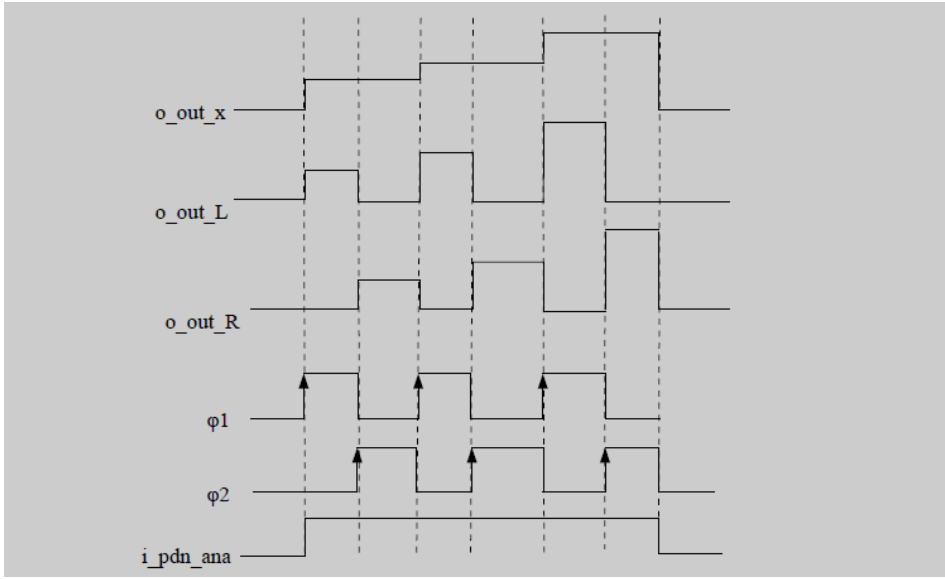
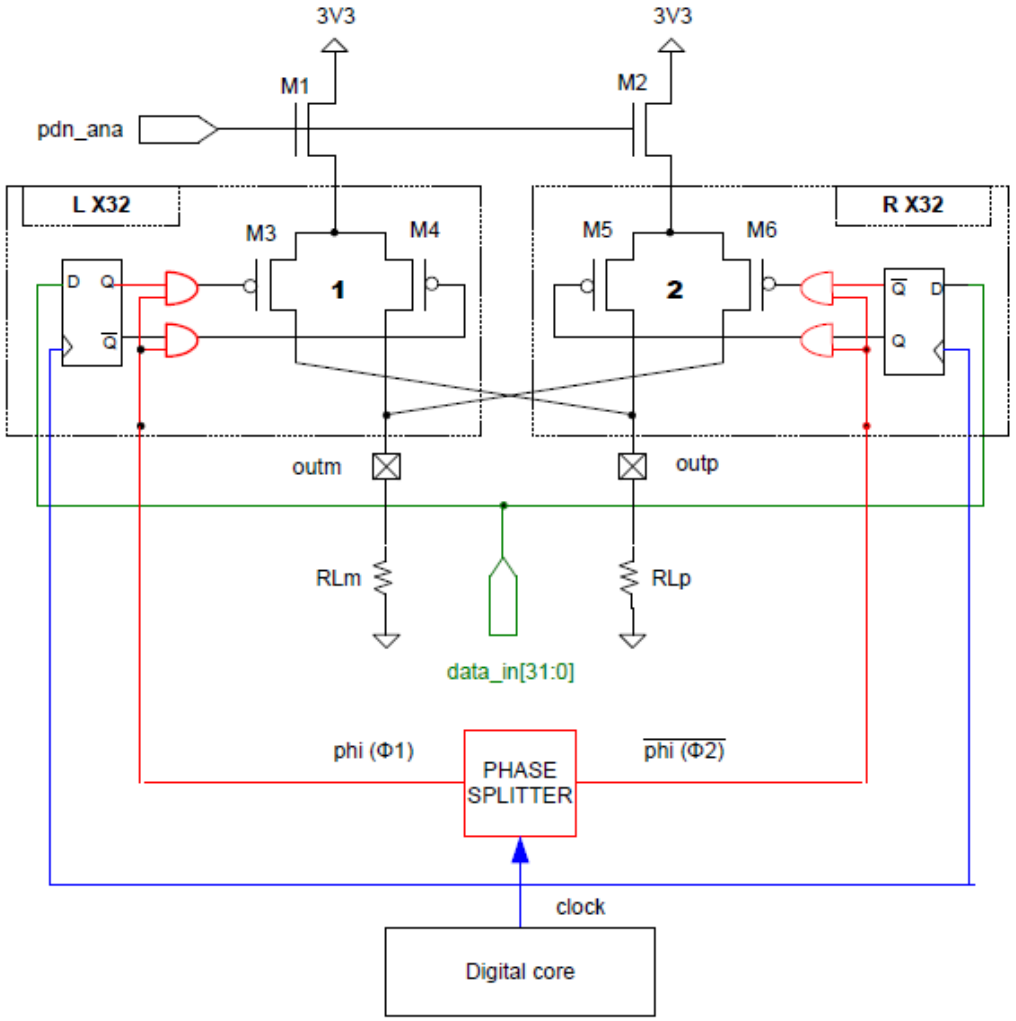


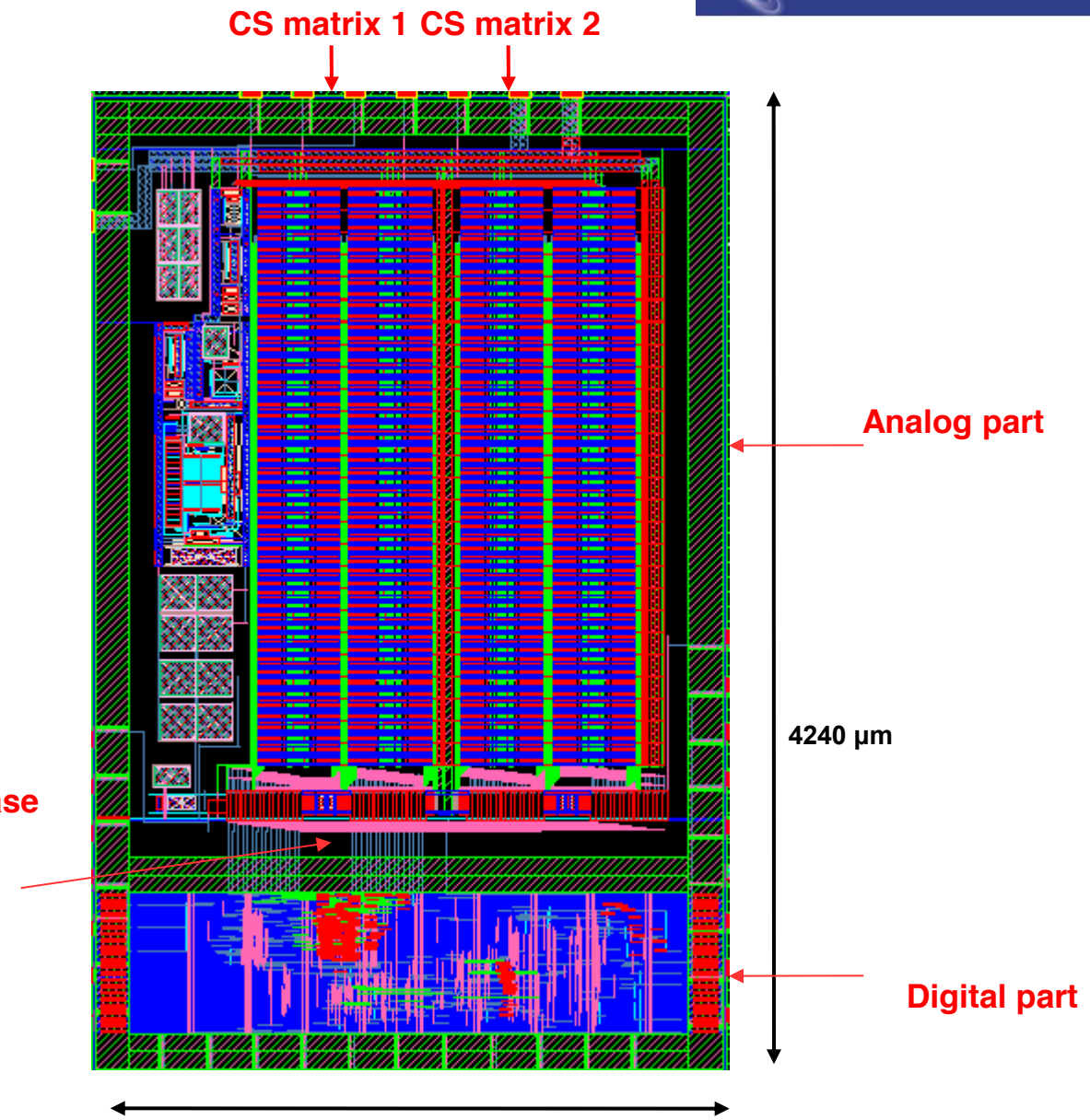
Figure 4.1: RTZ CS architecture



RTZ implementation



Layout

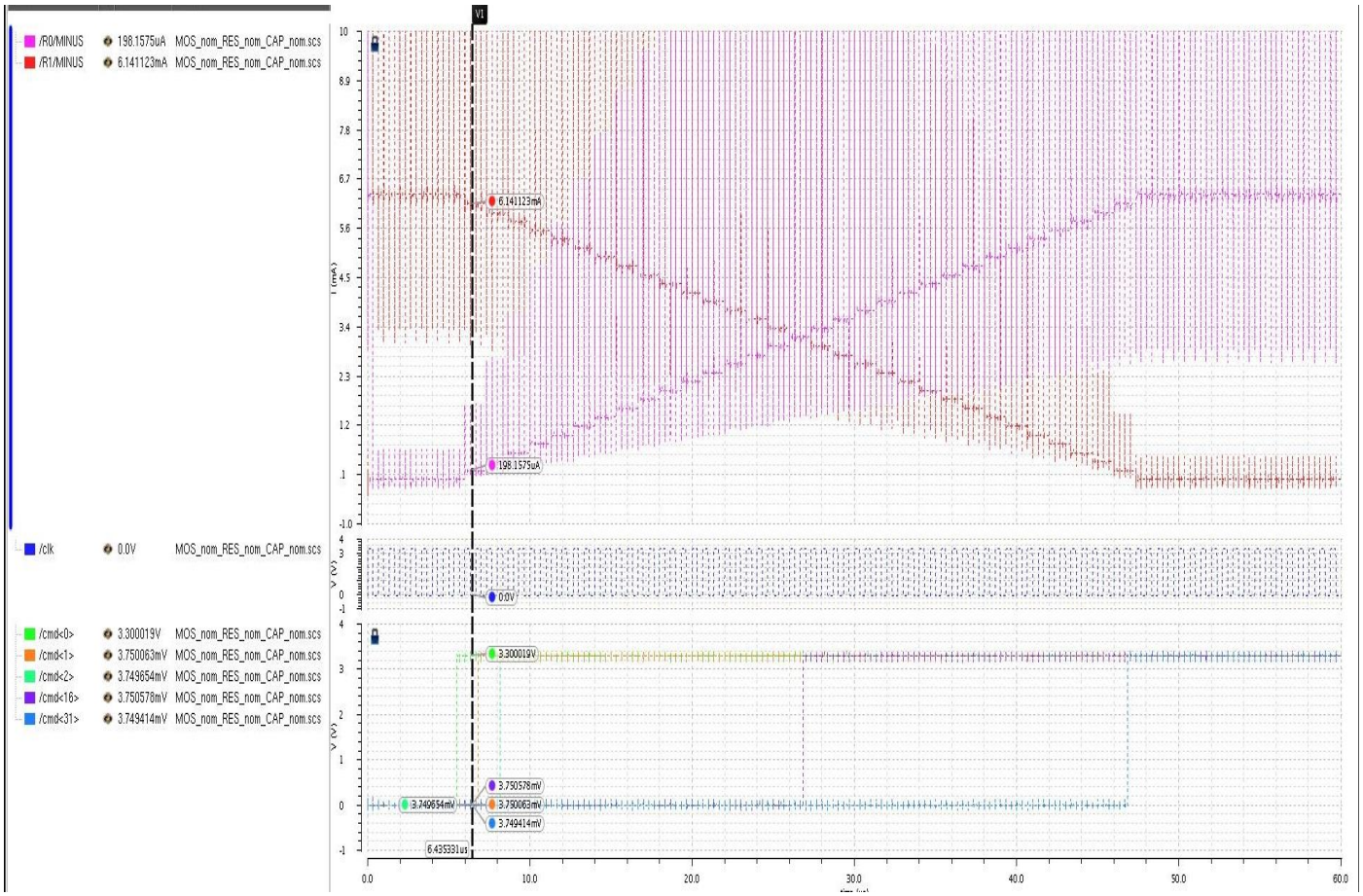

CS matrix 1
CS matrix 2
Analog part
4240 µm
Interface (level translators, phase generator and clock trees)
Digital part

Transient simulation

32 current sources descending (inverting output)

1.5MHz clock

Test data

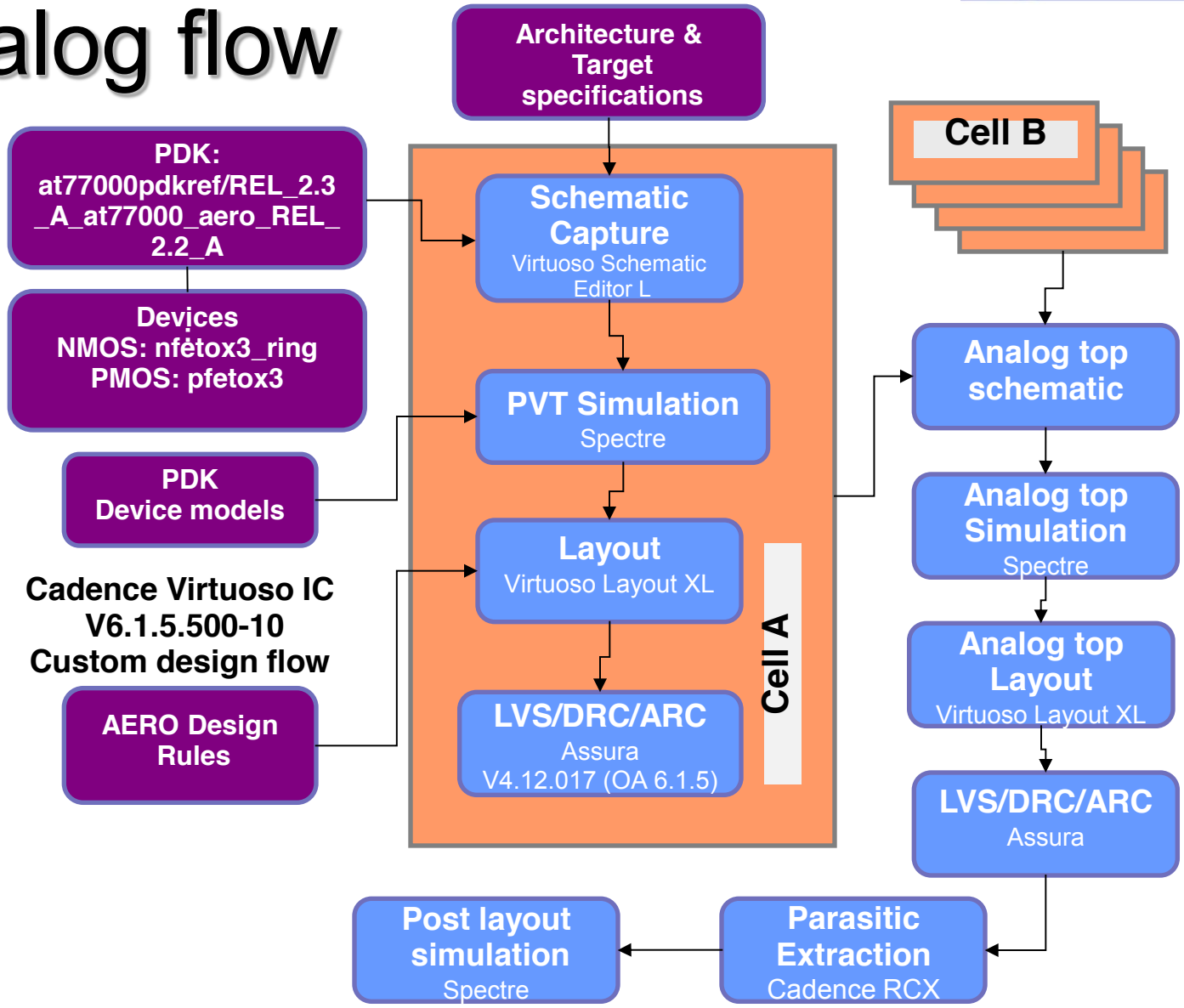


Analog/Digital/Top Design Flow for DAC24

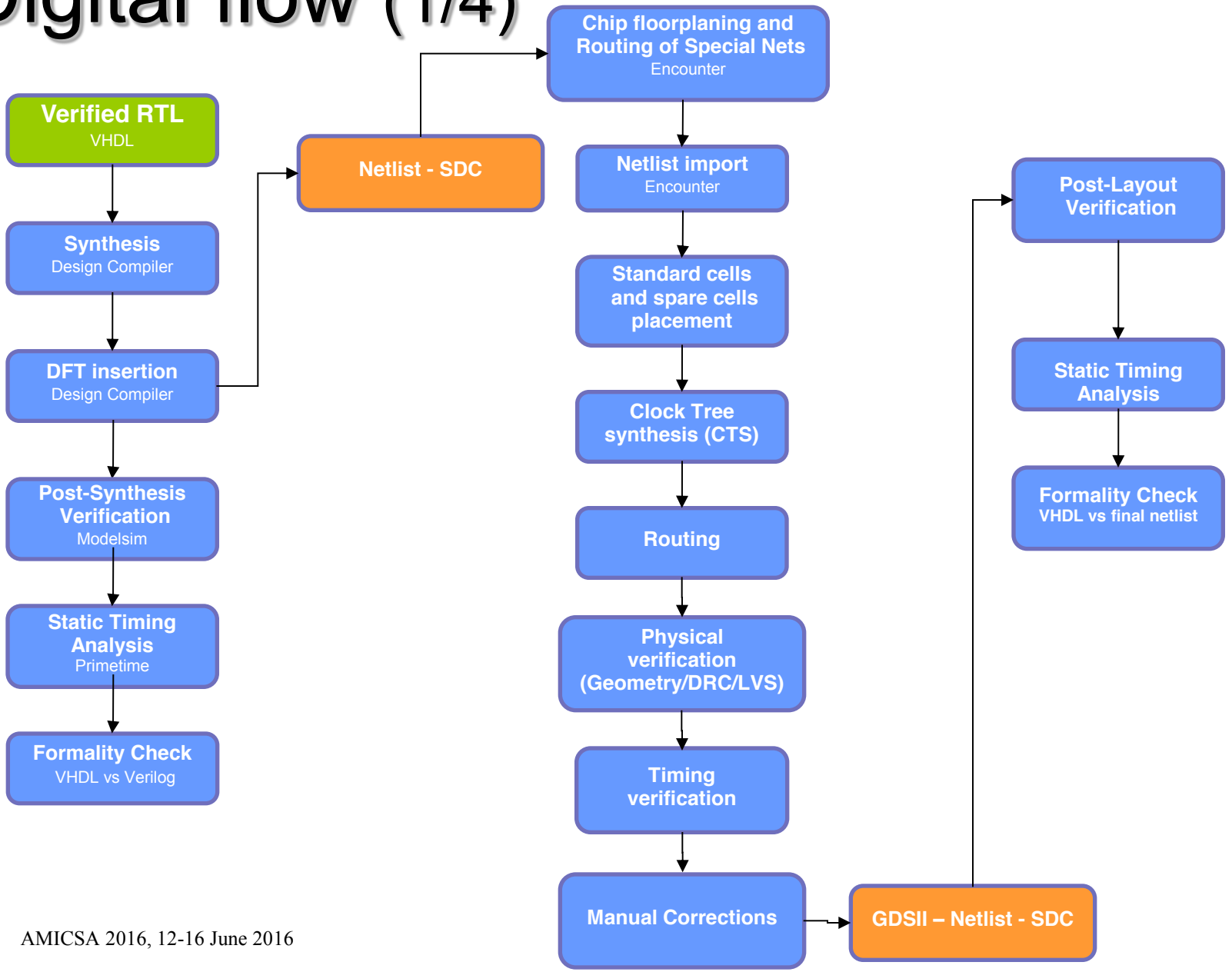
Mixed signal developments

- Radiation tolerant mixed-signal ASIC development for the space industry – AO7794
  - Development of a flow and a library
  - ASIC development via re-use
  - SEC & TCV for production
  - Flow
- Atmel ATMX150RHA technology
  - 150nm CMOS SOI, 5 metal, 1 poly
  - Supplies: 1.8V logic with 3.3V analog and I/Os
  - Extensive device and cell library
  - Rad-hard proven logic
  - Front to back design flow fully supported by the PDK
  - Fully SPICE modeled and characterized devices for analog design included: bipolar transistor, MIM capacitors, 70A oxide FETs,…
  - Low noise performance as demonstrated by circuit simulations
  - Full and direct support by the Atmel team on the PDK and design environment

Analog flow


Architecture & Target specifications
PDK: at77000pdkref/REL_2.3_A_at77000_aero_REL_2.2_A
Devices NMOS: nfetox3_ring PMOS: pfetox3
PDK Device models
Cadence Virtuoso IC V6.1.5.500-10 Custom design flow
AERO Design Rules
Schematic Capture Virtuoso Schematic Editor L
PVT Simulation Spectre
Layout Virtuoso Layout XL
LVS/DRC/ARC Assura V4.12.017 (OA 6.1.5)
Cell A
Cell B
Analog top schematic
Analog top Simulation Spectre
Analog top Layout Virtuoso Layout XL
LVS/DRC/ARC Assura
Parasitic Extraction Cadence RCX
Post layout simulation Spectre

Digital flow (1/4)



Digital flow (2/4)

- Input to the flow
  - Verified RTL in a set of testcases selected to cover different OSR values, dithering, bypass and reset modes.
- Synthesis - translate RTL to gate-level netlist:
  - Design Compiler K-2015.06
  - ATMX150RHA-max+mil+nldm library
  - Master clock: 10MHz, 50% duty cycle
- DFT insertion – scan chain inserted in the design
- Post-Synthesis Verification
  - Same set of tests is run, in order to ensure the correct functionality of the design (netlist/sdc after DFT insertion are used)
- Static Timing Analysis
  - verify the timing parameters of the design using Primetime

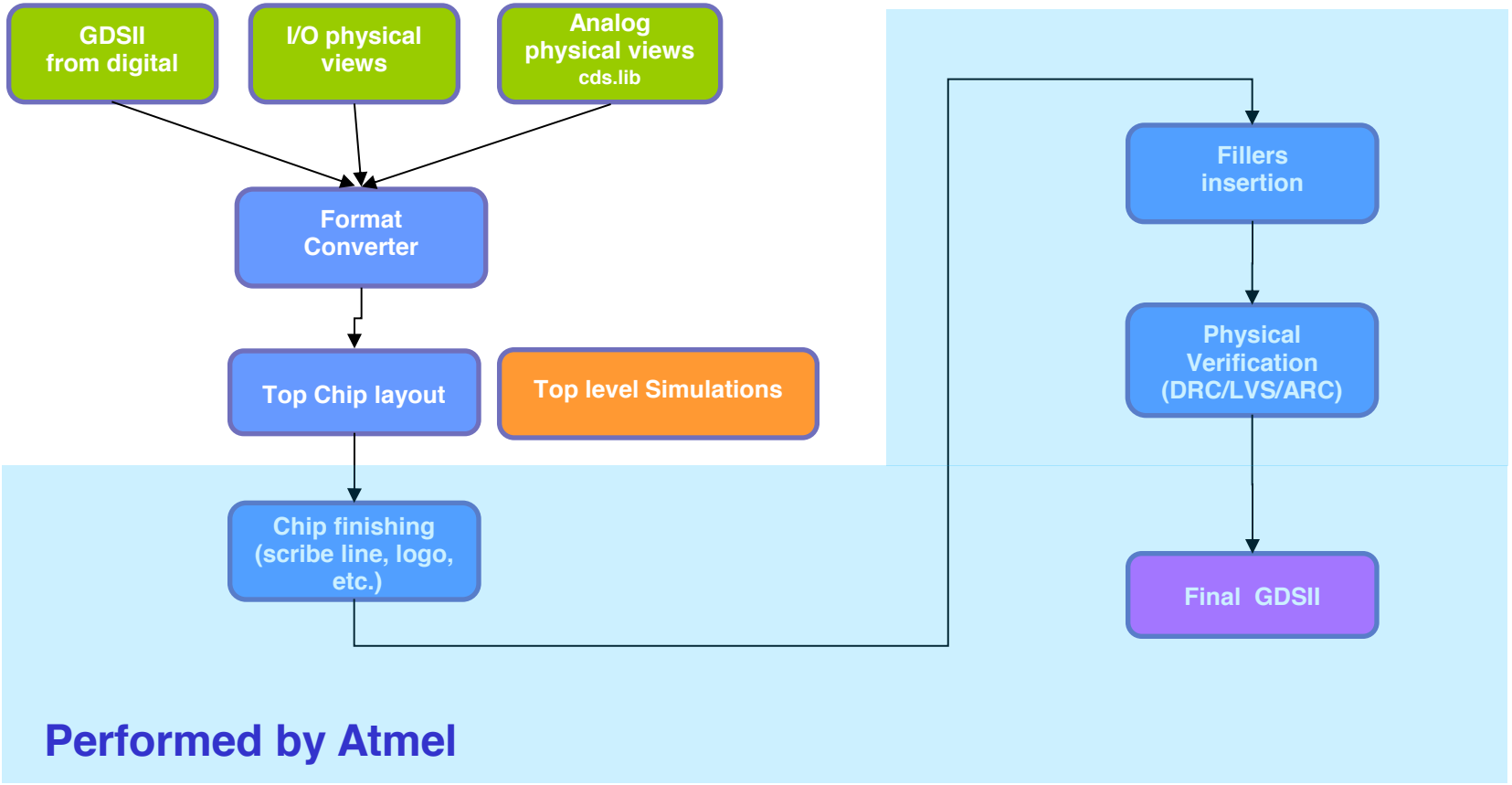
Digital flow (3/4)

- Formality Check
  - Compare VHDL files with the netlist (both before and after DFT inserion) for ensure functional equivalence.
- Physical Implementation
  - Inputs:
    - Verilog netlist after synthesis and DFT insertion
    - LEF files of the digital core standard cells
    - LIB files providing timing and power parameters for the cells
    - SDC file for the timing constraints generated at synthesis step
    - DEF file providing information on the floorplan, IO pins and power lines.
  - Routing of special nets (power supplies)
  - Placement of the cells
  - Placement of spare cells
  - Clock tree synthesis (CTS)
  - Routing of the design

Digital flow (4/4)

- Physical Implementation (continue)
  - Filler insertion
  - Geometry and connectivity verification
  - Timing verification
  - Extraction of GDS/netlist to be imported to Virtuso for chip integration
  - Manual corrections to prevent DRC violations in Virtuoso (same are not appeared as issues in Encounter).
- Post-layout Verification
  - Same set of tests is run, in order to ensure the correct functionality of the final design (netlist/sdc after place&route are used)
- Static Timing Analysis
  - verify the timing parameters of the design using Primetime
- Formality Check
  - Compare VHDL files with the netlist (after place&route) for ensure functional equivalence.

Top Design flow



Conclusions and next steps

- First samples expected end of June 2016
- Preparation for the validation phase based on the validation plan
- Evaluation of the design improvements with respect to the RTZ feature.
- Dissemination about the AO7794 library and flow
- Enrichment of the library (fast ADCs, etc)

Acknowledgments

The authors would like to thank Mr. Michel Porcher (Atmel), Rok Dietrich and Richard Janssen (ESA) for their continuous support.

Thank you for your attention!

Questions?