High Resolution Radiation Hardened DAC in CMOS-SOI Featuring a Return-To-Zero Matrix

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Abstract

We present a current-steering, low-noise, radiation hardened Digital-to-Analogue converter, optimized to operate in the frequency range between DC and 50kHz. The DAC receives 24-bit sampled data in a synchronous serial format and converts it into a differential current analog signal. It uses a third-order multi-bit Sigma-Delta modulator, which provides superior noise and linearity performance. The embedded interpolator follows a multiple-stage architecture and consists of an FIR equiripple low-pass filter followed by two cascaded stages of Half-band equiripple filters. The last stage is a programmable SINC filter, which provides variable interpolation ratios allowing sampling rates as high as 310kHz. The system operates on a single clock domain, which is provided externally. The output current matrix features a Return-to-Zero (RTZ) technique to improve the linearity by ensuring that each elementary current source is zeroed, regardless the data value of the sample sequence. The DAC is implemented in a rad-hard 150nm CMOS-SOI process, exhibits an SNR figure of better than 108dB, and consumes 62mW of power.

I. INTRODUCTION

Digital-to-Analogue (DAC) converters based on ΣΔ modulation are excellent alternatives to conventional current steering architectures, especially for low frequency applications. ΣΔ DACs are based on digital shaping of the quantization noise to the high frequency end of the spectrum, where it is suppressed by means of analog filtering. The work presented here concerns the design of a high resolution, radiation hardened, 24-bit DAC, which continues the work presented in [18]. The device is designed with the ATMX150RHA 0.15 μm CMOS-SOI technology of Atmel® .The presented DAC aims at high-reliability instrumentation and control applications where high accuracy and low noise operation are required.

ΣΔ architecture is an attractive way of realizing high accuracy and low power data converters. Oversampling architectures with noise shaping of quantization error are suitable for low and medium speed applications when there is a trade off between accuracy and speed [10]. A loss in dynamic range occurs if 1-bit quantizer is used in order to guarantee stability of the loop. To overcome this problem a multibit quantizer with a high-order ΣΔ modulator is employed resulting in little loss of dynamic range. As the internal signal swing is reduced with the increase in number of bits, the multibit ΣΔ modulator requires a lower slew rate and thus less power for analog circuits than the 1-bit case. However, the overall resolution of the converter is determined by the internal digital to analog conversion linearity. To improve the accuracy of the internal DAC many techniques have been proposed and analysed [2]-[6].

II. SYSTEM ARCHITECTURE

A. Overview

The architecture includes an interpolation filter with a noise-shaping loop which are digital, while the output stages include an internal DAC and a reconstruction low-pass filter which are analog. The reconstruction filter and the I/V converter are realized externally to aid the design flexibility and device integration according to the target application's requirements. The system block diagram is shown Figure 1.

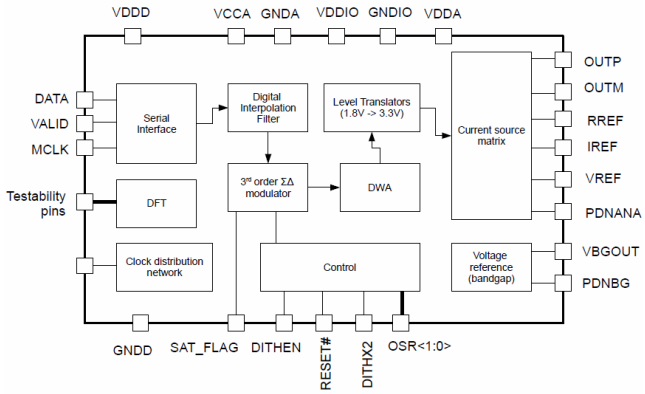

Figure 1: Block diagram of the DAC

B. *Digital Interpolator Filter*

The first block of the DAC is the interpolator. The digital signal interpolation is a fundamental operation to signal processing when a conversion between sampling rates is required. The interpolation stage can be considered as a combination of up-sampling and low pass filtering processes. Thus, the interpolation stage does not only increase the signal frequency by a factor of the Over-Sampling Ratio (OSR), but also has to suppress the image replicas. Many implementations have been reported for the realization of interpolators in the literature [7]-[10]. In this design, the interpolator is implemented efficiently using a multiple stage architecture. This reduces computational complexity, since a one stage implementation would result in a very high order filter. Typically, the order of a low-pass filter is a function of the required ripples δ_p and δ_s in the pass-band and stop-band respectively and inversely proportional to the normalized width of the transition band [11].

Finite Impulse Response (FIR) filters are preferred because they have linear phase response, which results in symmetric coefficients. The partitioning of the interpolation stage is shown in Figure 2.

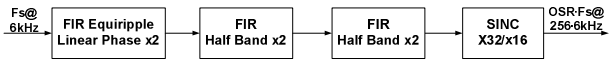

Figure 2: Multistage implementation of interpolator

The first stage is implemented using a 40th order FIR equiripple filter, whereas the second and third stage is implemented by a 30th and 18th order equiripple Half Band (HB) filter respectively. HB filters are FIR structures which allow every second tap weight except the central one to be zero and hence are very efficient in terms of implementation. Moreover, their pass-band and stop-band ripples are the same and their cut-off frequencies are symmetrical around π/2. The last stage is a second order Sinus Cardinal (SINC) filter, which offers variable Oversampling Ratios. The supported OSR values are x32, x64, x128 and x256 selectable through dedicated pins. The specifications of the filters are summarized in Table 1.

Filter Type	**Upsampling factor**	**Fs**	**Pass-band frequency**	**Stop-band frequency**	**Pass-band ripple**	**Stop-band attenuation**	**Order of filter**
Equiripple	x2	12 kHz	1 kHz	3 kHz	0.0001 dB	130 dB	44
HB equiripple	x2	24 kHz	3 kHz	9 kHz	0.00001 dB	130 dB	30
HB equiripple	x2	48 kHz	3 kHz	12 kHz	0.00001 dB	130 dB	18

Table 1: Specifications of interpolation filters

Each of the first three filters perform x2 interpolation and are implemented using a Multiply-Accumulator (MAC) architecture and polyphase decomposition which is described hereinafter. The transfer function H(z) of the filter can be expanded as shown in (1):

$$H(z)=\sum_{n=-\infty}^{\infty}h(n)z^{-n}=\sum_{n=-\infty}^{\infty}h(2n)z^{-2n}+\sum_{n=-\infty}^{\infty}h(2n+1)z^{-2n-1} \quad (1)$$

By defining the polyphase component filters as follows:

$$E_0(z)=\sum_{n=-\infty}^{\infty}h(2n)z^{-n}$$
$$E_0(z)=\sum_{n=-\infty}^{\infty}h(2n+1)z^{-n} \quad (2)$$

where $E_0(z)$ and $E_1(z)$ are the polyphase components of the decomposition, (1) can be re-written as the sum of the odd and even terms:

$$H(z)=E_0(z^2)+z^{-1}\cdot E_1(z^2) \quad (3)$$

Using the Noble identity [13], it is possible to reverse the order of upsampling and filtering as shown in Figure 3.

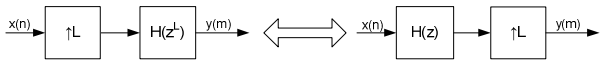

Figure 3: Illustration of Noble identity

Finally, the overall structure can be simplified by using a switch as shown in Figure 4 operating at the high frequency, whereas the polyphase components operate at the low frequency signal resulting in computational and power cost savings.

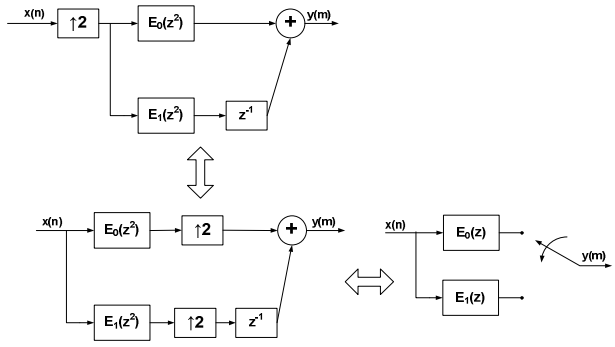

Figure 4: Polyphase implementation

C. *ΣΔ modulator*

The ΣΔ modulator is a fundamental component of the DAC. Several architecture considerations must be taken into account for determining the modulators characteristics, in order to achieve the desired SNR. An important design

decision is the resolution of the quantizer. Single bit modulators have the advantage of inherent linearity, low complexity and low implementation cost. On the other hand, multi-bit modulators exhibit better dynamic performance and overcome some stability problems associated with single bit modulators, provided that the appropriate architecture is chosen. They also introduce a reduced amount of quantization noise. For these reasons Multi-bit modulators are usually preferred [11], [14]. For low orders of modulation, error feedback and error feed-forward structures are preferred while for higher orders, Multi-stAge-noise-SHaping (MASH) architectures are generally used [11],[14]. Equation (4) associates the order (L) of the modulator, the resolution (B) the oversampling ratio (OSR) and the desired Signal-to-Noise Ratio.Equation (4) indicates that in order to achieve the desired Signal-to-Noise Ratio (SNR) the order (L) of the modulator, the resolution (B) of the quantizer and the Oversampling Ratio (OSR) should be increased.

$$SNR_{dB} = 10\log_{10}\left[\frac{3}{2}(2^B-1)^2\frac{(2L+1)OSR^{2L+1}}{\pi^{2L}}\right] \qquad (4)$$

A third order feed-forward ΣΔ modulator with a 5-bit internal quantizer was chosen. The initial sampling frequency is specified at 6 kHz and the OSR at x256, assuming the nominal clock frequency of 1.536 MHz. The input signal can be sampled up to 48 kHz when the OSR is adjusted to x32.

The most important design consideration for realizing a high order ΣΔ modulator is the feedback loop stabilization. For high order loops, stability considerations can reduce the achievable resolution to a lower value than that given by (4). In a third order ΣΔ topology, the Noise Transfer Function (NTF) H(z) is given in (5):

$$H(z) = (1-z^{-1})^3 \qquad (5)$$

Proper modulator operation is assured, if the loop filter remains linear and if the internal quantizer is not severely overloaded. A multibit internal DAC greatly relaxes the stability problem. The first criterion is to ensure that the closed-loop is stable according to the linear systems theory. Since the Signal Transfer Function (STF) is a pure time delay, stability is guaranteed. The second criterion is to ensure that the level of the input signal x(n) does not overload the quantizer. Considering a quantizer with M-step, (M+1) level, the modulator does not experience overload for any input u(n) [14] such that:

$$\max|u(n)| \le M + 2 - \|h\|_1 \qquad (6)$$

where:

$$\|h\|_1 = \sum_{n=0}^{\infty}|h(n)| \qquad (7)$$

and h(n) is the inverse z-transform of H(z) given in (5).

An other aspect of the ΣΔ architecture requiring attention is the generation of idle tones caused from the periodic output patterns at the output of the modulator. The linear noise model of the quantizer is valid only under specific conditions (large and random variations) on the input of the quantizer, which can be satisfied, if the input to the loop meets similar conditions. This means that the modulator under DC excitation or with very low frequency signals may produce periodic patterns, which give rise to idle tones. In practice DC patterns occupy few levels when the input is small. Under these conditions the behavior of multibit ΣΔ architectures is similar to that of a single bit ΣΔ modulator. To break the tones a pseudo-random 19-bit signal produced by a 35-bit Linear Feedback Shift Register (LFSR) is used. Assuming that the random signal to be introduced has a white noise type spectrum, then the most suitable place to add the dithering signal is just before the quantizer. The reason for adding it at this location is that the dithering becomes noise-shaped and thus a large amount of dithering can be added with negligible SNR degradation. The noise power of the dithering signal is similar to the quantization noise power. For assuring stability (8) should be satisfied [14]:

$$\|x\|_\infty \le 1 - \frac{1}{M}\left(1+\frac{\delta}{\Delta}\right)\|h\|_1 \qquad (8)$$

where δ and Δ is the amplitude of the dither and the input signal respectively, $\|x\|_\infty$ is the input maximum peak value, M corresponds to the quantizer steps and $\|h\|_1$ is given in (7). The output of the modulator is normalized to 1 in the previous equation. The time domain and frequency response of the output of the modulator are displayed in Figure 5 and Figure 6 respectively for a sinusoidal input of 750 Hz.

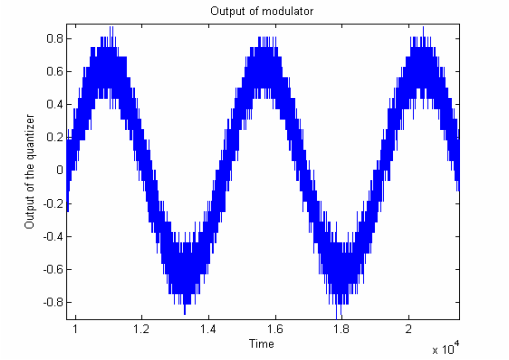

Figure 5: Output of the modulator with dither

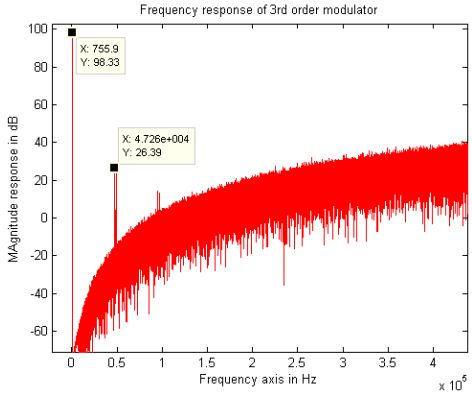

Figure 6. Frequency response of the modulator

D. *Dynamic Element Matching*

The use of a multibit ΣΔ modulator implies the use of an internal multibit DAC. This component, whether it is implemented with resistors or capacitors, exhibits non-linear transfer characteristics with respect to DNL and INL, due to element mismatch. There are two different architectures for the implementation of the DAC: the binary weighted code and the thermometer code. Both architectures offer a trade-off between the DAC's linearity, mismatch error, complexity and area overhead.

Binary weighted topologies have very small complexity, and can be applied to DACs with high resolution. Their disadvantage is the non-linearity of the output caused by unwanted glitches when big transitions happen in the current sources. This affects strongly the DNL performance.

Thermometer code topologies, on the other hand, overcome the differential non linearity problem. The price paid for them is the large area consumed by the sources and the extra decode logic on the digital part of the DAC.

Output linearity is one of the basic DAC features, therefore thermometer code architecture is preferred. In order to avoid element mismatch, which can severely degrade the static performance, different Dynamic Element Matching (DEM) algorithms were studied.

One of the most efficient algorithms to implement DEM is the Data Weighted Averaging (DWA) technique, which is applied in this DAC [1]. Unlike other techniques, which are based in the random element selection, DWA follows a cycled rotation approach. The algorithm's purpose is to achieve in long-term, an equal usage of the elements and, since the mismatch error is a random variable, the mean value is zero. Table 2 displays an example of the DWA algorithm applied to seven elements.

Time	Input	Index	1	2	3	4	5	6	7
1	5	1	•	•	•	•	•		
2	6	6	•	•	•	•		•	•
3	3	5					•	•	•
4	5	1	•	•	•	•	•		
5	2	6						•	•
6	3	1	•	•	•				
7	6	4	•	•		•	•	•	•
8	5	3			•	•	•	•	•
9	5	1	•	•	•	•	•		

Table 2. DWA algorithm example

The advantage of the DWA algorithm is that it uses only one index, which is updated with the addition of the input at every clock cycle

III. ARCHITECTURE OF THE ANALOG PART

A. *Description*

The 32 bit output of the DWA block drives the current sources in the analog section. The output of each analog sub-block of the DAC is the current summation of the 32 elementary current sources in a common node. Figure 7 shows the architecture of the analog part.

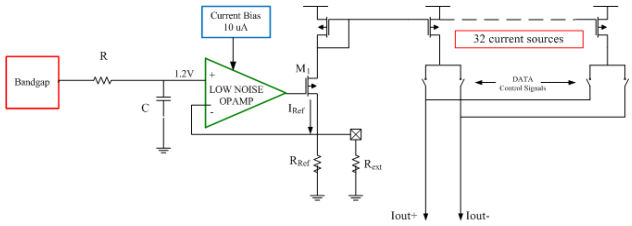

Figure 7. Architecture of the analog part

The components of the analog part of the DAC are a bandgap block, an RC low pass filter, a low-noise operational amplifier (OPAMP) and a current matrix consisting of 32+32 PMOS differential current sources.

The purpose of the bandgap block is to provide an accurate and temperature insensitive voltage output, which is then used as a reference point for generating and maintaining the reference current. The output voltage is 1.25V with a low temperature coefficient. The voltage reference is based on subtracting the voltage of a forward biased base-emitter junction PNP transistor having a negative temperature coefficient, from a voltage that is proportional to absolute temperature, which has a positive temperature coefficient. The noise of the bandgap block is decreased with the addition of a series RC low pass filter.

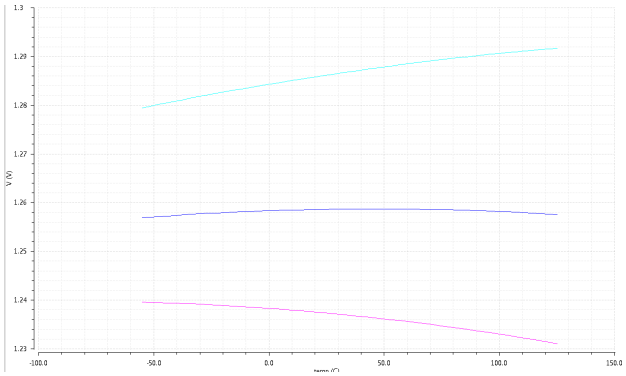

Figure 8: Bandgap output versus temperature at FF -55C 3.6V, SS 125C 3V and TYP 25C 3.3V conditions

The purpose of the operational amplifier is to fix the reference current I_{REF} across transistor M_1. The amplifier senses the voltage drop across the resistor RREF and fixes the I_{REF} by biasing the transistor M_1. RREF is an integrated resistor used to set the reference current value. As an alternative option, this resistor can be bypassed and an external component of different value can be used instead. This approach has the advantage of selecting the maximum value of the sourced current and consequently determining the power drawn from the analog supply. The OPAMP is a two-stage implementation consisting of a first differential stage followed by a push-pull output stage. The amplifier has an open loop gain of 85 dB, a phase margin of 60 degrees, a gain margin of -11.7 dB, and 42 dB Power Supply Rejection Ratio (PSRR). The amplifier is biased by a 10 uA current, generated internally.

The elementary current source cells used in the DAC,

are the basic components of the analog part. Each current source steers 198.1uA of current, resulting in a full-scale output of 6.34mA when all the 32 elements are on. In order to achieve good linearity figures, the elementary current sources should be well matched. In this implementation, we followed a centroid and symmetrical matrix layout by using an arrangement of spare and dummy cells. For the implementation of the current sources, the Regulated Cascode Topology is used as illustrated in Figure 9 [16].In this topology, the M_2 transistor is kept stable in order to have high overall output impedance against channel length modulation. To keep the transistor stable, a feedback loop is used consisting of an amplifier (M_3 and M_4) and M_1 acting as a follower. The use of oversized PMOS transistors, results in lower flicker noise and high linearity [17].

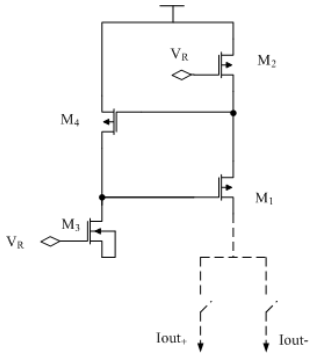

Figure 9. Regulated Cascode Topology

B. *Return-to-Zero Matrix*

The objective of the functionality is the current output to exhibit an RTZ characteristic for each sample. The adapted technique to achieve this is based on splitting the entire CS matrix into two equal and synchronized RTZ CS sub-matrices, with their outputs tight together in a common summing node. The expected advantage of this scheme is the adequate suppression of the harmonic distortion products at the output [20]. Both matrices are driven with the same data; the first one (denoted as LEFT 'o_out_L') contributes to the output during the first half period of the clock cycle while the second one (denoted as RIGHT 'o_out_R') contributes during the second half period. This is graphically represented in Figure 10.

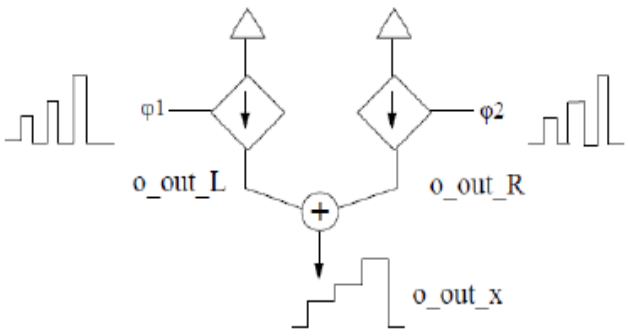

Figure 10: RTZ CS architecture

This functionality implies the utilization of two synchronized anti-phase clocks (φ1, φ2), each one dedicated for each sub-matrix . The two phases can be derived from the main clock input with φ1 to trigger the L matrix, and φ2 to trigger the R matrix. This scheme permits the two matrices to operate in a complementary fashion for each sample.

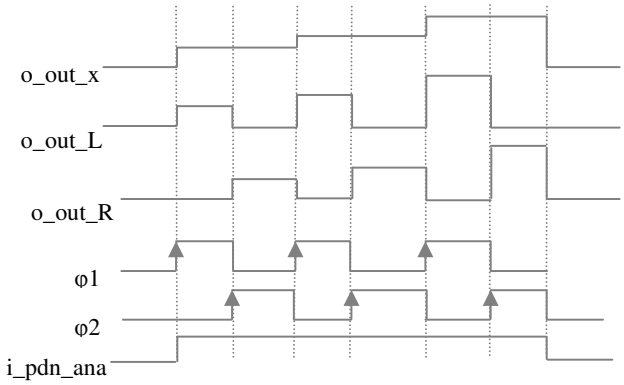

Figure 11 : RTZ Timing Diagram

The entire matrix consists of two thermometer coded sub-matrices, each one composed of 32 equal elementary differential CS cells.

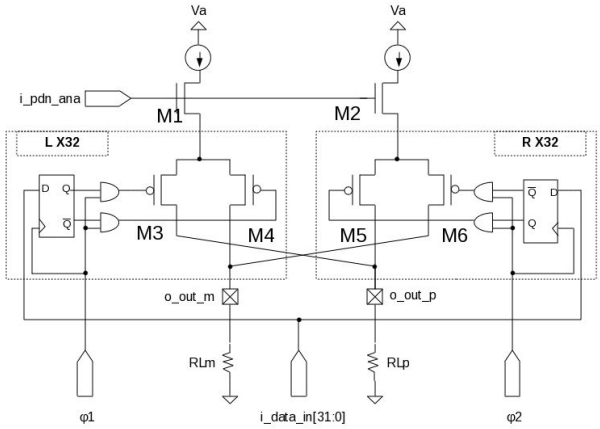

Figure 12: CS matrix simplified schematic

The positive and negative polarities are tied together in the common summing nodes denoted as 'o_out_p' and 'o_out_m' respectively. This yields to a single differential current steering output. The switches of each elementary CS (M3-M4, M5-M6) are driven in a complementary fashion from a common flip-flop and generate the differential polarities. The Left flip-flop (L) is clocked from φ1 while the Right flip-flop (R) is clocked from its complement φ2. The data line is common for both sub-matrices.

Each flip-flop output passes through an AND gate with its corresponding phase clock signal to guarantee, that when L branch is active, R is completely disabled and vice-versa. The 'i_pdn_ana' signal has a global power down effect, as it blocks the current path from the analog power supply rail Va via switches M1, M2.

IV. ON THE PROCESS FLOW

A. *Analog Part*

The analog part of the design has been processed separately, in order to obtain the analog physical views (cds.lib) that were used in the top design flow. For each cell of the analog part, we run the following steps. Firstly, the schematic of the cell is created by using the Virtuoso Schematic Editor XL™ tool. Then, a set of tests, in a wide range of process, voltage and temperature (PVT) corners, is run to ensure the correct functionality of the resulted schematic. Cadence Spectre™ simulation platform is used. In a next step, the layout is generated by using the Virtuoso Layout XL™ tool. The physical design implementation is done according to the predefined rad hard design rules. A set of checks is done that concerns LVS (layout versus schematic), DRC (design rule checking) and ARC (antenna rule checking). This physical verification is done by the Assura™ tool.

As soon as the processing for all the cells has been completed, an equivalent process flow is run for the analog top part. The first step is to generate the analog top schematic and then, a set of tests is run to ensure the correct functionality (Spectre tool). After having generated the analog top layout (Virtuoso Layout XL), a set of checks is done concerning LVS, DRC and ARC. In the next step, the calculation of the parasitic effects in the design (parasitic extraction) is done by using Assura RCX tool. The final step concerns the post-layout simulations by using the Spectre tool.

B. *Digital Part*

The digital part of the design has been processed separately, in order to obtain the GDSII file to be used in the top design flow. Starting from a verified RTL (written in VHDL), the design is synthesized by using the Design Compiler™ tool. The RTL is translated to gates from ATMX150RHA-MAX+MIL+NLDM library. In the same step, the scan chain is inserted in the design (DFT). The results of these steps are a netlist and a corresponding SDC (Synopsys Design Constraints) file. Post-synthesis verification (Modelsim™), static-timing analysis (Primetime™) and functional equivalence (Formality™) are run by using this netlist and SDC, in order to ensure the correctness of the synthesis.

The next step of the process flow concerns the physical implementation. In Encounter™ tool, we have performed: routing of special nets-power supplies, placement of the cells and spare cells, clock tree synthesis, routing of the design, filler insertion, geometry/connectivity/timing verification, extraction of GDS/netlist. One more step is needed for our design concerning some manual corrections in the layout, to anticipate from errors appearing in Virtuoso during top design flow, but not existing as issues in Encounter). The final GDSII is used in the next step of the process flow.

V. RADIATION HARDENING

The DAC is implemented in the single-poly, 5-metal, 0.15μm CMOS on SOI radiation hardened process of Atmel. The digital part is synthesized using the robust cells from the library, including latches and flip-flops with increased area. Triple Modular Redundancy (TMR) is used for every flip-flop and finite state machine along with voting scheme, as a highly effective fault tolerance technique in masking Single Event Effects (SEE). As an added measure, the reset is synchronized with the clock.

The analog part is hardened using relaxed layout rules, guard rings and extensive use of enclosed layout NMOS transistors (ELT). ELT transistors can greatly improve the analog degradation due to TID effects, which can be caused by radiation induced charge trapping in the oxides or at the Si interface [19]. The layout is almost totally immune to Single Event Latch-up (SEL) thanks to the deep trench isolation option (DTI). Each CMOS structure is isolated using a deep trench extending down to the buried oxide of the SOI, as shown in Figure 13. This arrangement cuts away the parasitic SCR devices inherently present in the CMOS structure that may trigger SEL events. The target LET for SEL immunity is greater than 70 MeV/mg/cm^2. The target figure for TID tolerance is 100 krad (Si). Hardening against Single-Event Transient effects (SET) is achieved by placing capacitors of the appropriate size to every sensitive analogue node. The value of each capacitor is optimized for each node through time domain SET simulations.

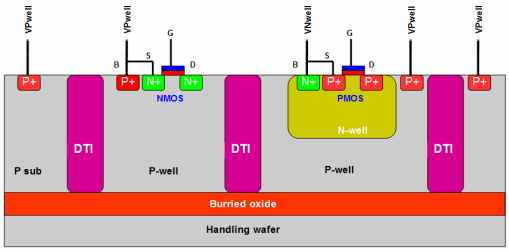

Figure 13: layout cross-section

VI. IMPLEMENTATION & SIMULATION RESULTS

The total area including the core and the I/O pads measures 17.5 mm^2. (x:3.5mm, y:5mm). All the capacitors in the signal path are of MIM type. In Figure 14 the floorplan of the chip is shown.

The dynamic performance of the SDM was evaluated by running post layout transient simulations in Spectre™. Figure 15 shows the output current when the 32 current sources open in sequence. Each current source steers 198.15 μA, which corresponds to a full scale current of 6.34 mA when all 32 sources are open. In the figure, point 1 shows the negative output, while point 2 shows the positive one. Points 3 and 4 corresponds to 32 open sources, while points 5 and 6 to 0 open sources. In the part of point 7, the master clock is shown. Finally, the input thermocode is shown at point 8.

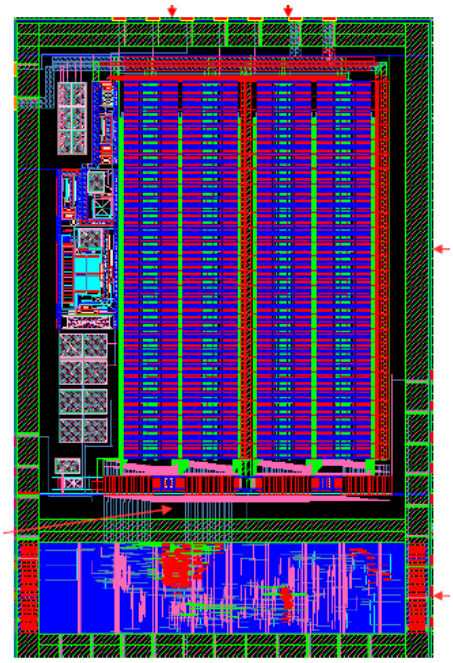

Figure 14: DAC chip floorplan

Table 3 summarizes the characteristics of the DAC obtained after simulation. The radiation tolerance limits are attributed to the target specifications.

Specifications	Value
Dynamic Range	> 108dB
Signal-to-Noise Ratio	> 108 dB
Sampling rate	Up to 310 kSps
Monotonicity	Full code range
Power dissipation	62 mW
LET for SEL immunity	$\geq$ 70 MeV/mg/cm^{-2}
SEU immunity	Protection of critical memory cells
SET immunity	Protection of the digital part
TID tolerance	$\geq$ 100krad
Temperature range (functional)	-55 °C < T < 125 °C
Temperature range (full performance)	0 °C < T < 50 °C

Table 3: DAC Performance summary

VII. CONCLUSION

The design of a high resolution ΣΔ DAC has been presented. The DAC is designed to exhibit more than 108 dB of SNR over its entire analog bandwidth while remaining tolerant to space radiation. The chip validation in silicon will demonstrate how closely the theoretical performance limit could be reached by this DAC, and will evaluate the effectiveness of the RTZ feature in terms of dynamic performance.

VIII. REFERENCES

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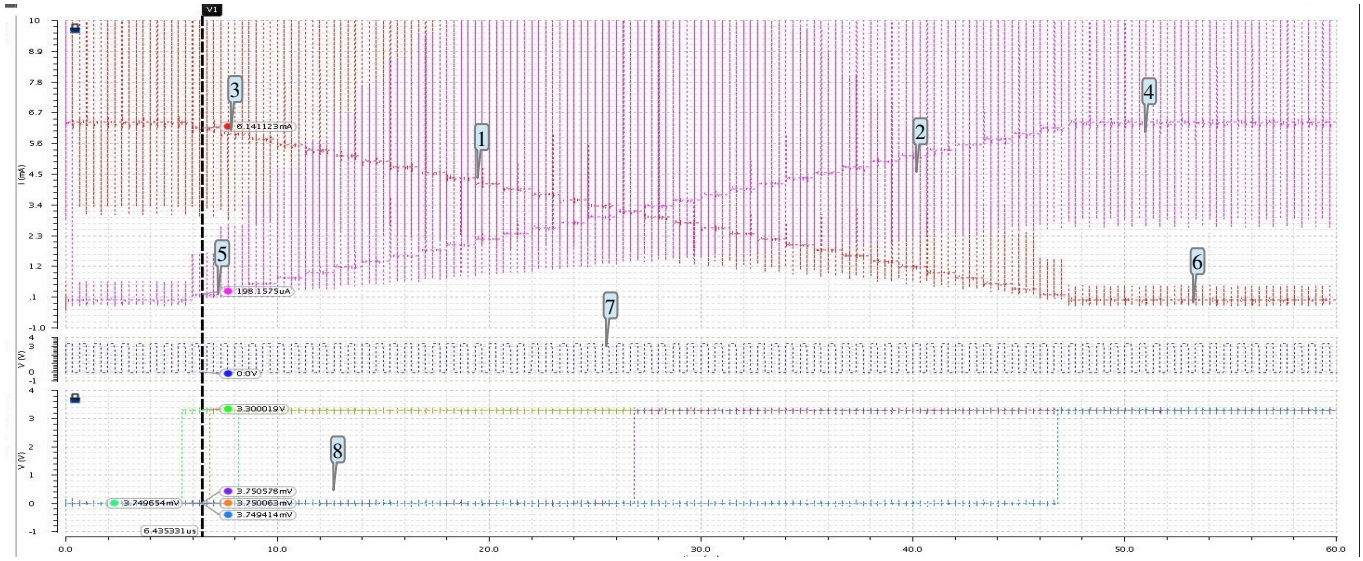

Figure 15: Differential Output Transient Simulation