Scalable Sensor Data Processor
Testing and Validation


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15/06/2016
Outline

- Introduction
- SSDP Prototyping
- Test Bench
- Testing and Validation Activities
- Conclusion
Introduction
Background

The Scalable Sensor Data Processor (SSDP) has been commissioned by ESA on the scope of the CTP programme, aimed at being used by next-generation instruments, payloads and robotic exploration applications, e.g. rovers and landers.

The SSDP is a “One-stop shop” mixed-signal ASIC, offering control and data processing resources together with a rich set of Input/Output interfaces in the same package.

Cost-effective alternative to ASICs and FPGAs upon design of instruments, payloads and even spacecraft control, e.g. ICUs, DPUs, OBCs and robotics applications both at processing and sensors & actuators level.

Builds on previous ESA Contracts: MPPB, DARE180.
Introduction
SSDP Architecture (I)

Process and Control in the same package, with data acquisition capabilities

**Processing Subsystem**
- 2x Recore Xentium DSP
- Network-on-Chip (NoC) interconnect
- On- and off-chip data acquisition

**Control Subsystem**
- 1x CG LEON3FT GPP
- AMBA 2.0 Bus Interconnect
- Local and Networked I/O peripherals
Introduction
SSDP Architecture (II)

Input/Output
- Analogue I/O, with mixed-signal interfaces
- Digital Local and Networked I/O

Processing Resources
- Xentium
- LEON3FT

Internal Functions
- Memory Scrubbing
- Time- and House-Keeping
- DMA transfers
- Subsystem Interconnection
  … etc.
Introduction

Activities to be performed

Testing and Validation Activities driven by questions

Module/Interface Testing
  - Does the module/interface \( N \) provide the required functionality?

Validation
  - Does the system – or a subset of several integrated modules/interfaces – behave as intended?

Benchmarking
  - What is the \{maximum, minimum\} <metric> it can be achieved?
  - How does <metric> in this system compare to system \( X \)?

These questions can be addressed by using appropriate:

- Tests, for Module/Interface testing
- SW and algorithms, for Validation (e.g. operating systems and CCSDS compression)
- Benchmark suites, for Benchmarking (e.g. NGDSP)
An appropriate Test and Validation Architecture is needed, with a Test Bench providing Stimuli and Control inputs

... all this requires some support from several parts

- SSDP Hardware and Software Support
- Test Bench Hardware and Software Support
- Software for tests and benchmarking, both at Test Bench and SSDP level
SSDP is a complex system requiring appropriate prototyping support, for testing and validation.

- PCB with required (physical) resources
  - I/O Interfaces
  - Peripherals
  - Power distribution and miscellaneous

- FPGA device for Processing and Control Subsystems
  - Fabric big enough to accommodate both subsystems
  - Enough I/O pins for required interfaces and peripherals
SSDP Prototyping
Supporting Architecture

Based on a Xilinx Kintex UltraScale FPGA

All I/O interfaces available, analogue interfaces may be emulated

Mezzanine Interfaces for adding additional interfaces and functions
- Off-Chip ADC and DAC
- GPIO
- Logic Analyser connection
- Mixed-Signal Emulation
Revisiting the previously laid Test Bench Architecture

Test Bench will be in charge of testing activities, controlling and providing stimuli to the SSDP, and at the same time capturing the outputs and validating them.

Test Bench Hardware and Software must be flexible enough to cover all the needed activities, and even support further activities, e.g. radiation testing.
Test Bench
Hardware

- National Instruments PXI Platform
- Controller Module, to execute the needed SW
- I/O Interface Modules
  - SpW
  - CAN
  - UART
- Reconfigurable I/O Module
  - Xilinx Kintex-7 FPGA
  - > 100 configurable I/O lines
  - Can be used for SPI, I2C, etc.
Test Bench Software

Test Bench Software is NI LabView, allowing to exploit the full potential of the NI PXI Platform

Modular Visual Test Development

- Enables abstraction by instantiating "boxes" inside "boxes"
- Enables reuse

GUI-Assisted Test execution
Flexible architecture, capable of being used for all types of testing and validation activities

Type of test requires different partitioning of “intelligence” between the Test Bench and the SSDP

Interface testing requires more “intelligence” on Test Bench SW
Testing and Validation Activities
Interface Testing

Current activities are focused in Interface Testing
- Lowest abstraction level (configuration, registers, etc)
- Most of the test activities are in the Test Bench, with the SSDP having software just to support testing activities
- Interface (Control) between Test Bench and SSDP is performed via Tele-Commands, in an Out-of-Band fashion

Tests can be executed in *Manual* or *Automatic* Mode
- Manual, suitable as Debug
  - Individual Parameter Control
  - Interactive Test
  - Low Coverage of functionality tested
- Automatic, suitable as Production
  - Automatic Parameter Control
  - Pre-Defined Test
  - High coverage of functionality tested
TEST PROGRAM INFORMATION

SSDP Front Panel

<table>
<thead>
<tr>
<th>VSA resource name</th>
<th>Done</th>
<th>Read</th>
<th>Error Status</th>
<th>Consumer</th>
<th>StopWhile consumer</th>
<th>Terminal</th>
</tr>
</thead>
<tbody>
<tr>
<td>COM1</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- **Command**
  - `help`

- **Scaler frequency [Hz]**
  - 10000

- **Timer index**
  - TIMER 0

- **Timer frequency [Hz]**
  - 1

- **Timer period [S]**
  - 1

- **Handler to configure**
  - 0
  - ConfigOp
  - ini
  - I
  - SendChar

- **AutoStart**
  - OFF/ON
  - GenerateInt
  - OFF/ON

- **Comando**
  - IRQ handler delegate config

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PROPRIETARY INFORMATION
Concluding Remarks (I)

SSDP is a complex piece of hardware
- Multiple & Heterogeneous Processing Resources
- Analogue I/O
- Digital I/O
- … all in the same package!

The SSDP makes use of a robust Testing and Validation Architecture, with a custom-made prototyping board and a National Instruments PXI Platform and LabView software

This architecture can be reused in EM and FM testing, and even be extended for radiation testing campaigns

Testing and Validation Activities of SSDP must be performed at several abstraction levels, from interface to benchmarking
Concluding Remarks (II)

Currently the Interface Testing activities are in full-speed
  Bulk of software support is on the Test Bench
  SSDP Tests are being designed and carried out in manual and automatic modes

Validation activities have begun, with in-house implementation of algorithms, such as DWT and simple image processing. These can be complemented by (re)using already developed code, e.g. CCSDS 12\{1,2,3\} for compression

Future: Benchmarking, according to the NGDSP suite