A 2.56 Gbps Radiation Hardened LVDS/SLVS Receiver in 65 nm CMOS

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Abstract

A novel radiation hardened by design LVDS/SLVS receiver is designed and simulated in 65 nm CMOS technology. The receiver is capable of receiving a 2.56 Gbps signal with less than 400 fs RMS jitter and 500 μW power consumption drawn from a 1.2 V power supply. A replica receiver with a compensation loop is used to measure and compensate for the total ionizing dose (TID) radiation effects. This loop will ensure an equal propagation delay of the rising and falling output edges, to allow the use in accurate time-domain signalling circuits.

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I. Introduction

Many of today's applications require high precision time-domain signal processing circuits like particle detectors in high-energy physics experiments such as the CMS and ATLAS experiments at the Large Hadron Collider (LHC) in CERN [1] or laser-ranging sensors [2]. The key information of these applications is contained in the timing difference between multiple signals or events. This timing information is usually converted to binary data using time to digital converters (TDC) [3]. In large and/or complex systems however, the distance between the detector/event generator and the TDC can become rather large, calling for a highly time accurate, long distance, transfer of these signals.

Low Voltage Differential Signaling (LVDS) and Scalable Low Voltage Signaling (SLVS) are, because of their robustness to interferences, low power consumption and high speed [4][5], commonly used techniques for data transmission in today's applications. The SLVS standard is comparable to the LVDS standard, with the difference of a 200 mV common mode voltage instead of 1.2 V and a smaller voltage swing. For data transmission applications, the regenerative nature of the receiver allows some tolerance to jitter provided the bit error rate remains sufficiently low. However, in the envisaged sub-nanosecond timing applications, jitter is the major impairment to the performance of the system. When an LVDS/SLVS receiver is used in the signal path between the event generator circuit and the TDC, any time distortion introduced by the latter, will cause a time measurement error and consequently will lower the system resolution. To allow an accurate time measurement between several events, the propagation delay of all the edges, at the output of the LVDS/SLVS receiver, must be the same.

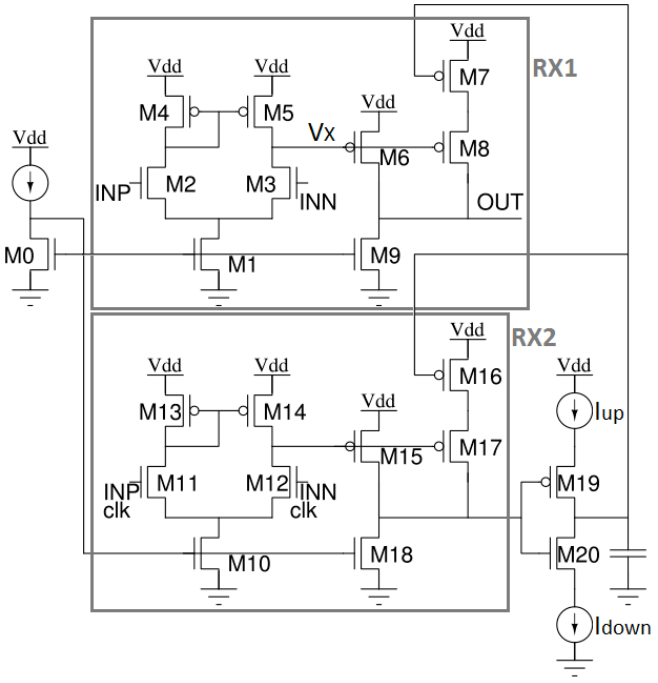

Figure 1: Schematic of the LVDS/SLVS receiver with feedback loop

This paper focuses on the design of a total ionizing dose (TID) radiation hardened by design LVDS/SLVS receiver which can be used in these long distance, high time resolution measurement applications. Radiation effects and/or process corners, will alter the propagation delay of the rising and falling edges at the output. In this design the time difference between these two propagation delays will be measured and compensated by a replica receiver with a charge pump based feedback loop [6].

This paper is organized as follows. Section II shows and discusses the schematic of the LVDS/SLVS receiver. The simulation results of the receiver and feedback loop are shown and discussed in section III.

II. Schematic

The schematic of the receiver is shown in Figure 1. Here RX1 (with input pair M2-M3) receives the accurate timing signal. From a design perspective it is possible to balance the propagation delays of the rising and falling output edges by choosing the ratio between M6 and M9 (ignoring for the time

being M7 and M8). However this cannot be done across all process corners and temperature variations.

Moreover, in radiation environments, the total ionizing dose radiation effects will cause shifts in the threshold voltage and degradation of the charge carrier mobility [7]. These effects will change the gain/propagation delay of the receiver's first stage and consequently will lower the current through M6 and so increases the propagation delay of the rising edge. In this case, transistor M9 can be set far into saturation region, so the threshold voltage shift does not, or minimally, effects the output current. Design for immunity to TID will also increase the circuit's robustness in term of PVT (Process-Voltage-Temperature).

To compensate the receiver's variations in speed and propagation delay, transistor M7 and M8 are added. The current through M7 can now be adjusted to compensate the increase or decrease in the current through M6 due to TID radiation effects and/or process variations. In this design, M8 is used as switch to turn off M7 together with M6 when the output voltage is low.

The mismatch between the propagation delays of the rising and falling output edges will be measured by a replica receiver (RX2 in Figure 1, input pair M11-M12) associated with a charge-pump (M19 and M20 and current sources I_{UP} and I_{DOWN}). When the propagation delays of the rising and falling edges are equal, an ideal clock at the input of this replica receiver will generate a clock signal at the output with a duty cycle of 50 %. In this case, when both charge pump currents are equal, the output voltage will settle to $V_{DD}/2$.

Any deviation from this 50 % duty cycle, caused by the TID effects, process corners or temperature, will cause the charge pump output voltage to shift. This voltage shift is used to compensate the current through M7 and M16 in order to equalize the propagation delays of the output rising and falling edges.

In this design, the clock input for the replica receiver will be generated by a second source. In practice, this can be done by a CDR (Clock Data Recovery) circuit. To save power, the feedback loop can also be implemented on the actual receiver (here RX1). But this requires a Manchester coding (which will halve the bit rate for the same bandwidth), or a scrambled signal with enough bit-flips, depending on bandwidth of the feedback loop and the frequency of the input signal, to ensure a stable voltage at the output of the charge pump.

III. Simulation Results

The proposed receiver is designed and simulated using a commercial 65 nm CMOS technology. This technology has a power supply of 1.2 V which is identical to the common mode voltage of an LVDS signal. In this design, for an optimal use of the receiver, the common mode voltage of the input signals must be between ± 0.5 V - 1 V. This is fine for ad-hoc systems, like the CMS and ALTAS detectors at CERN, which don't need to communicate with off-the-shelve LVDS modules, and so can freely choose the common mode level. Nevertheless, the proposed technique is easily scalable to I/O devices or other technologies with a larger power supply for full LVDS compatibility. Additionally, a PMOS input pair receiver is designed which is able to receive low common mode voltage and SLVS signals. All simulations shown in this section were done using the cadence spectre simulator.

All following simulation results will be executed using a 2.56 Gbps input signal with 200 mV single ended swing and 800 mV common mode voltage. The top receiver (RX1 in Figure 1) has a 2^7-1 sequence pseudo random bit stream input, while a separately generated clock is added at the input of the replica receiver (RX2 in Figure 1). The 800 mV common model level will give the worst case output signal. When the common mode level decreases, current source M1 will go into the linear region, consequently decreasing the current through the receiver and its performance. An increase in common mode voltage will make M1 more able to provide current through the receiver, thus increasing the speed and performance of the receiver.

A. Normal operation

Figure 2 shows the simulated eye diagram of the receiver's input (grey line) and output (black line) signal (output signal of RX1 in Figure 1). In an eye diagram, when the propagation delays of the rising and falling edges are equal, the crossing voltage of both edges should be at V_{DD}, in this case 0.6 V. In this paper, this crossing voltage is given to indicate the error in the propagation delay. Knowing the rise and fall times, and assuming that $t_{RISE} = t_{FALL}$, the error can then be calculated using:

$$Propagation\ delay\ error = \pm \frac{t_{rise}}{V_{DD}} \left(V_x - \frac{V_{DD}}{2} \right) \quad (1)$$

where V_x equals the crossing voltage.

In the eye diagram of Figure 2, the crossing is 580 mV, so indicating a small error between both propagation delays. This error is due to mismatch in the charge pump currents. The loop will, in this case, generate a 580 mV output voltage instead of 600 mV. The output signal has a rise and fall time of 100 ps and so a -1.5 ps propagation delay error between both edges. The output signal shown in this figure has a 400 fs RMS output jitter and consumes 500 μW drawn from a 1.2 V power supply.

The output signal of the charge pump during start up is shown in Figure 3. The feedback loop has a start up time of approximate 60 ns. This start up time can, depending on the application, be changed by changing the charge pump's current and/or capacitor. In regime, the output signal of the charge pump has a 10 mV variation.

B. Corners/Temperature/Voltage

This subsection give an overview of the variations of the crossing voltage and propagation delay error in terms of PVT.

These simulations were executed using the same input variables as in section III-A.

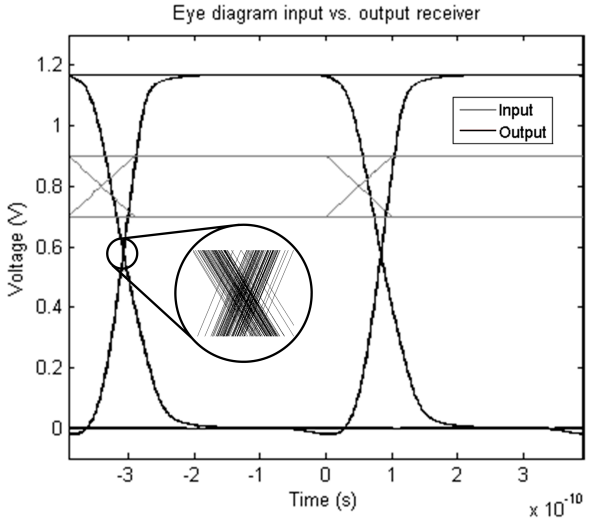

Figure 2: Eye diagram output LVDS/SLVS receiver with 200 mV amplitude, 800 mV common mode level and 2.56 Gbps, 2^7-1 sequence pseudo random bit stream input

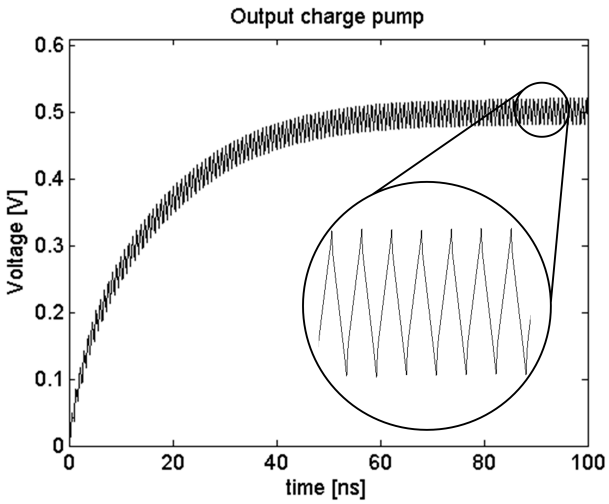

Figure 3: Output charge pump with 200 mV amplitude, 800 mV common mode level and Gbps, 2^7-1 sequence pseudo random bit stream input

The variations due to process corners are shown in Table 1. In all corners, the crossing voltage varies from 500 mV (SS corner) until 640 mV (SF corner) which is a total variation of 140 mV. The output signal has a rise and fall time of a 100 ps and so the crossing point variations will, using Eq. (1), introduce a total propagation delay variation of 10 ps, from 3 ps (SF corner) and -7 ps (SS corner).

Table 2 shows the variations of the crossing voltage and propagation delay due to changes in the operating temperature. Here, the crossing voltage varies from 550 mV (-25°C) until 640 mV (125°C) which is a total variation of 90 mV. The rise and fall times remain 100 ps, and so the crossing voltage variation can be related to a total propagation delay of 6.6 ps, going from -3.6 ps (-25°C) up to 3 ps (125°C).

Finally, the effects of 20 % power supply variations are shown in Table 3. Here, the crossing voltage varies from 460 mV (1.08 V) until 730 mV (1.32 V) which is a total variation of 270 mV. These variations relate, with a 100 ps rise and fall time and respecting the change in supply voltage in Eq. (1), to a total propagation delay error variation of 17.7 ps, from -10.3 ps (1.08 V) up to 7.4 ps (1.32 V).

Table 1: Variations crossing voltage and propagation delay error vs. corners

	TT	FF	FS	SF	SS
Crossing voltage [mV]	580	630	520	640	500
Propagation delay error [ps]	-1.5	2.2	-5.9	3	-7

Table 2: Variations crossing voltage and propagation delay error vs. temperature variations

	-25°C	25°C	85°C	125°C
Crossing voltage [mV]	550	580	620	640
Propagation delay error [ps]	-3.6	-1.5	1.5	3

Table 3: Variations crossing voltage and propagation delay error vs. power supply variations

	1.08 V	1.2 V	1.32 V
Crossing voltage [mV]	460	580	730
Propagation delay error [ps]	-10.3	-2.33	7.42

C. Influence of radiation

The TID radiation effects on the proposed circuit are simulated using transistor models with parameters after 500 Mrad radiation. Again, these simulations were executed using the same input variables as in section III-A.

The results of the radiation simulations (grey line) are shown together with the original output signal (black line) in Figure 4a. The simulated output signal after irradiation clearly has a larger propagation delay and a data dependency of the rising edge. These effects can be related to the internal node V_X (Figure 1). Due to the decrease of the transistor's gm, caused by the TID radiation effects, the charge and discharge speed of node V_X decreases, consequently increasing the slew rate of this node and the output propagation delay. Secondly, due to this drop, the internal node V_X can't be fully charged at the 2.56 Gbps speed. Now depending on the previous bit, node VX can be fully or partially charged, which will cause a variation in the propagation delay, resulting in the observed data dependent jitter.

The eye diagram (Fig. 4a) shows an output rise and fall time of 140 ps and a data dependent variation of the crossing voltage of 150 mV, which relates to a 16 ps data dependent jitter. The output signal has an average crossing voltage of 590 mV which gives a -1.2 ps propagation delay variation. This is only a 10 mV increase in crossing voltage and a 0.3 ps variation on the propagation delay error compared to the closed loop simulations without irradiation (section III-A). Figure 4b shows the output signal of the receiver when no feedback loop is implemented. The propagation delay error at

normal operation is equal to the one of the closed loop system. Like in the closed loop output signal, the open loop output signal has a rise and fall time of 140 ps. The crossing

Table 4: Summary table of required styles.

	Data rate [Gbps]	RMS jitter [ps]	Power [mW]	FOM [mW/Gbps]	FOM [ps/mW]	Measurements	Technology
This work	2.56	0.4	0.5	0.19	0.8	No	65 nm
[4]	11.2	58.8	1.602	0.14	36.7	Yes	0.18 μm
[8]	1.5	/	7	4.66	/	No	150 nm
[9]	3	/	2	0.67	/	No	0.18 μm
[10]	6.4	/	4.2	0.65	/	Yes	80 nm DRAM

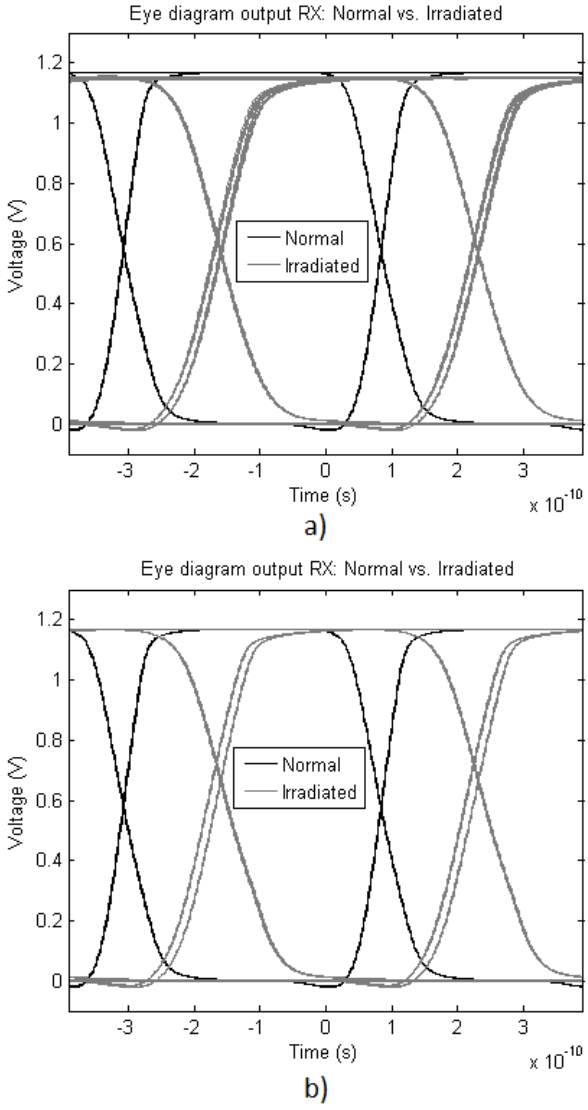

Figure 4: Eye diagram output LVDS/SLVS receiver with 200 mV amplitude, 800 mV common mode level and 2.56 Gbps, 2^7-1 sequence pseudo random bit stream input: a: Normal vs. irradiated output signal with compensation. b: Normal vs. irradiated output signal without

voltage has a data dependent variation of 300 mV, resulting in a 35 ps data dependent output jitter. The average crossing voltage equals 700 mV, which gives a 11.6 ps propagation delay error. This is a 120 mV crossing voltage increase and a 13.1 ps propagation delay variation compared to the open loop simulations without irradiation.

The simulations with irradiated transistor models and without compensation loop indicate a 19 ps decrease in data dependent output jitter and a 11 ps decrease in propagation delay error when the feedback loop is added.

D. Comparison SOTA

Table 4: gives a comparison of the proposed receiver with the current state of the art (SOTA). The data rate, jitter and power consumption are summarized in two figures of merit (FOM). The first FOM gives the power consumption of the receiver, relative to the data rate. The receiver designed in this paper has a FOM of 0.19 mW/Gbps which is slightly more than the 0.14 mW/Gbps of [4] but significantly less compared to the 4.66 mW/Gbps [10] and 0.65 mW/Gbps [9] of the other receivers. The second FOM gives the RMS jitter as a function of the power consumption. For the proposed receiver this is only 0.8 ps/mW, which is substantially lower than the measured 36.7 ps/mW achieved in [4].

IV. CONCLUSION

This paper proposes a novel 2.56 Gbps, radiation hardened by design, LVDS/SLVS receiver. Primary simulation results show a 500 μW power consumption and a 400 fs RMS output jitter. The propagation delay differences, due to radiation effects or PVT of the rising and falling edges at the output is compensated using a replica receiver with compensation loop. In normal operation, the receiver has a -1.5 ps propagation delay error. The process corners, temperature and power supply variations give a total propagation delay error variation of respectively 10 ps, 6.6 ps and 17.7 ps. The radiation effects were simulated using 500 Mrad TID irradiated transistor models. These simulations show a 13.1 ps propagation delay error at the output of the open loop receiver. The receiver with the proposed feedback loop shows only a 0.3 ps propagation delay error, which is an improvement of more than 43 times compared to the open loop system.

The main origin of variations in the propagation delay due to PVT originates in the mismatch between the charge pump currents. Consequently, the robustness to PVT can easily be increased by improving the robustness of the charge pump.

V. ACKNOWLEDGEMENTS

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