25-Gb/s/Channel VCSEL Driver and Transimpedance Amplifier Array ICs in 0.25-µm SiGe:C BiCMOS Technology for Space Applications

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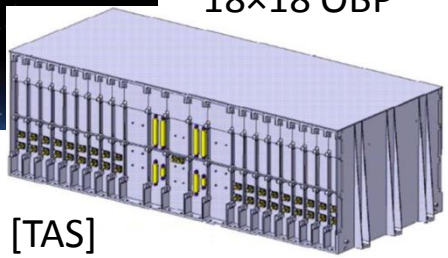
Outline

On-Board Processors in a Satellite

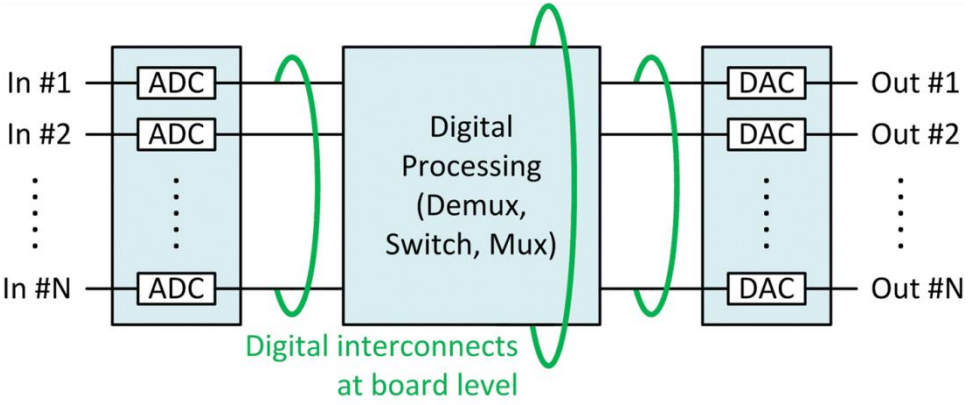
- Next-gen telecom satellites needed to offer very high data rate connections
- Massive digital data transfers between boards, modules, and equipment



Example of 18×18 OBP

[TAS]

Schematic of Digital OBP



850-nm optical interconnects

- VCSEL, PD, multimode fiber, and electronics
- High-speed, low-power, small-size and lightweight connections at a low cost

➔ ***The most attractive solutions for future intra-satellite networks***

MERLIN Project

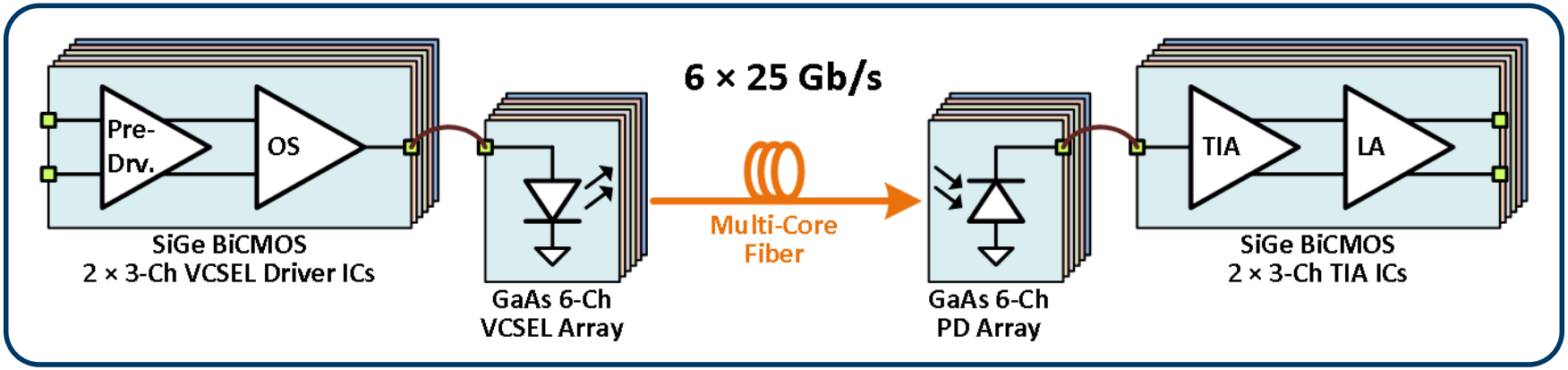
Multi-Gigabit, Scalable & Energy Efficient On-Board Digital Processors Employing Multi-Core, Vertical, Embedded Opto-Electronic Engines

- EU FP7 Space research project grant for 2013–2016 (www.space-merlin.eu)
- **Space-grade optical interconnectivity** for future terabit-scale telecom satellites
  - ***150-Gb/s*** throughput and ***<10-mW/Gb/s*** power consumption
  - Very dense integration by the use of ***multicore fibers***, custom ***VCSEL & PD arrays***, and custom ***multi-channel ASICs***

Project Consortium

G&H · ThalesAlenia Space · U·L·M Photonics · ofs A Furukawa Company · ihp · VTT · Chalmers

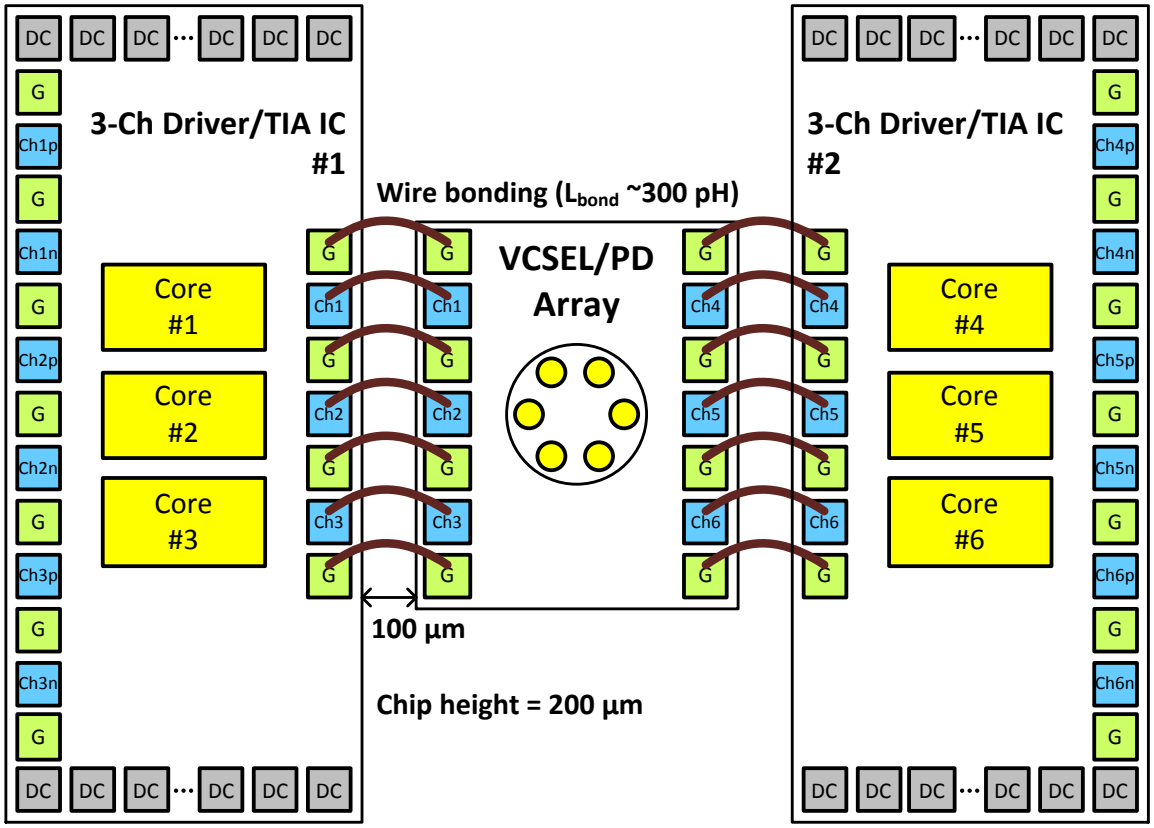
150-Gb/s Optoelectronic Module



Key Requirements for ASICs – VCSEL Driver and Transimpedance Amp. (TIA)

- # Channels: 3
- Data rate: 25 Gb/s per channel
- Power consumption: <10 mW/Gb/s per channel (Tx + Rx)
- Operating temperature: −40 to +85 °C (up to +100 °C)
- Radiation-hardening
- Serial interface for control and monitoring

IC Floorplan



- 2 × 3-ch IC (rotated 180 degrees)
- Differential for electrical signaling / Single-ended for optical devices
- Common-node voltage (VCSEL ground or PD bias) provided from the IC
- Bondwire inductance on the signal path taken into account

IC Development

Two-Generation Development Approach

- Gen1 ICs: focus on verification of high-speed signal path with simple analog control circuits
- Gen2 ICs: include advanced digital control functions with SPI bus

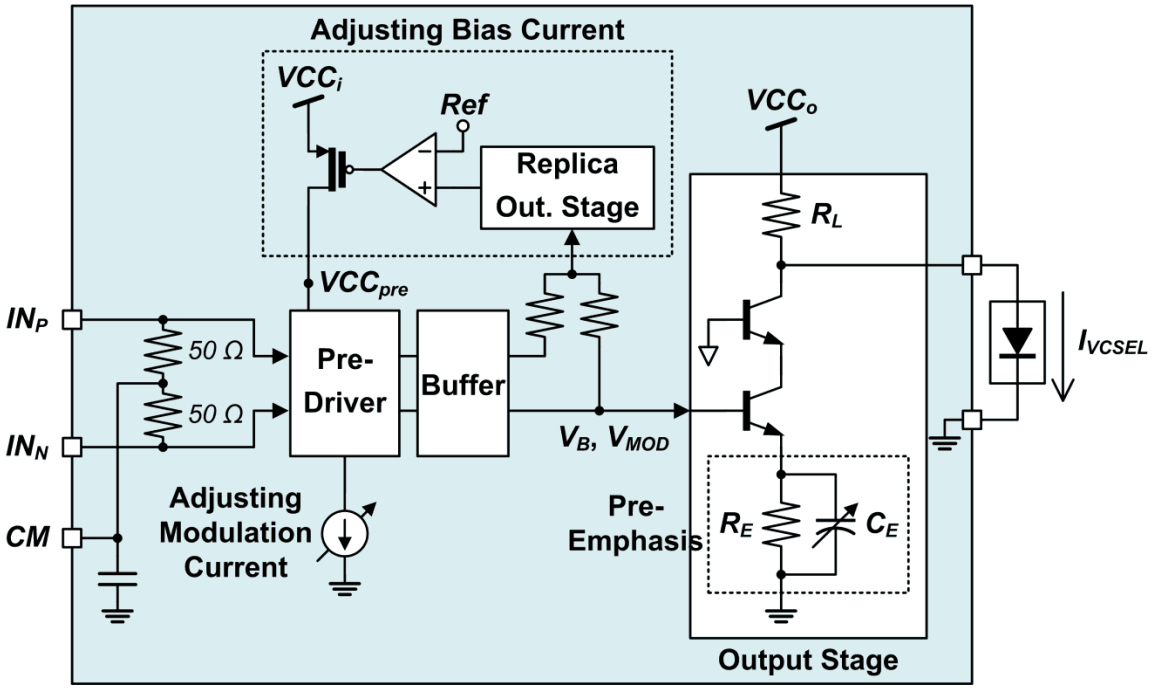
Fabrication Technology

- IHP's 0.25-µm SiGe:C BiCMOS technology: ***SG25H4*** (former SG25H1)
- Same CMOS & BEOL as SGB25RH (IHP's RH technology)

  ➔ ***RH libraries*** available
- Higher-performance npn-HBTs with f_T/f_{max} = 190/220 GHz

  ➔ Suitable for 25 Gb/s or even faster

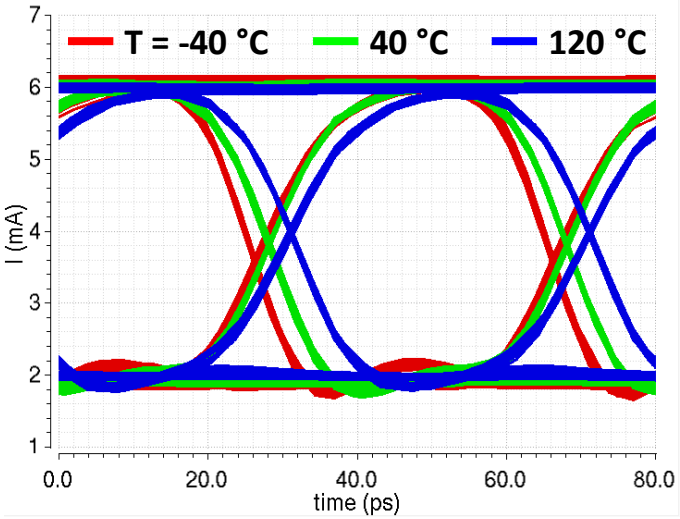
VCSEL Driver – Features



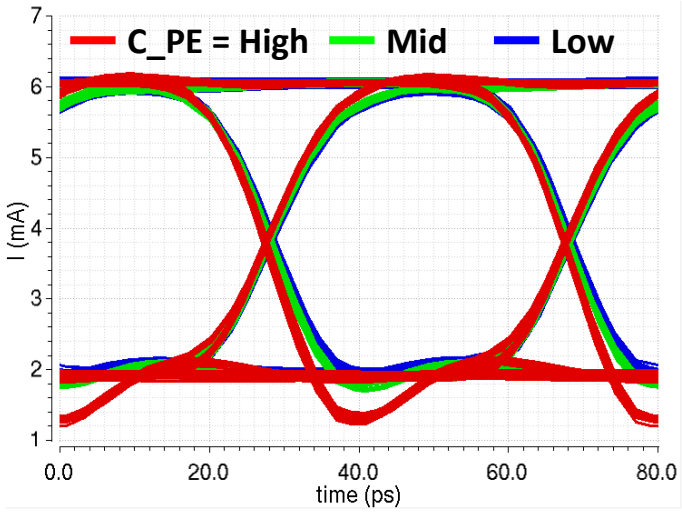
- Low-power design
  - ***Single-ended*** output stage: power reduction up to 50%
- Adjustable, ***temperature-independent*** VCSEL currents
  - Robust ***feedback-loop biasing*** with replica output stage
  - Proportional to absolute temperature (PTAT) current sources
- ***Adjustable pre-emphasis*** bandwidth extension

VCSEL Driver – Simulation Results

< 25G Eye vs. Temperature >



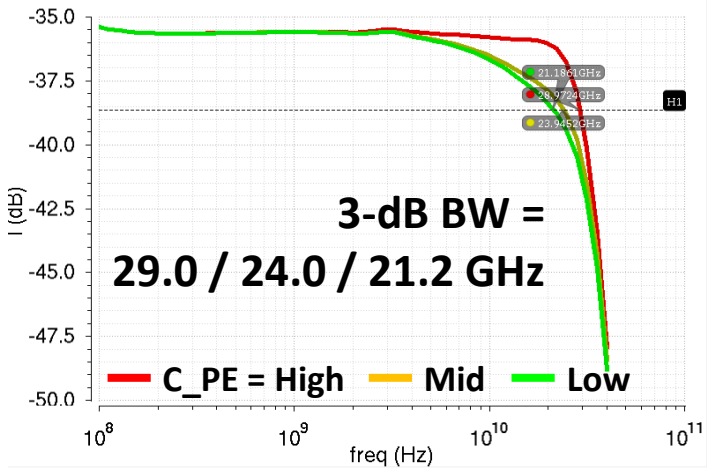
< 25G Eye vs. Pre-Emphasis >



Post-layout simulations with VCSEL ECM

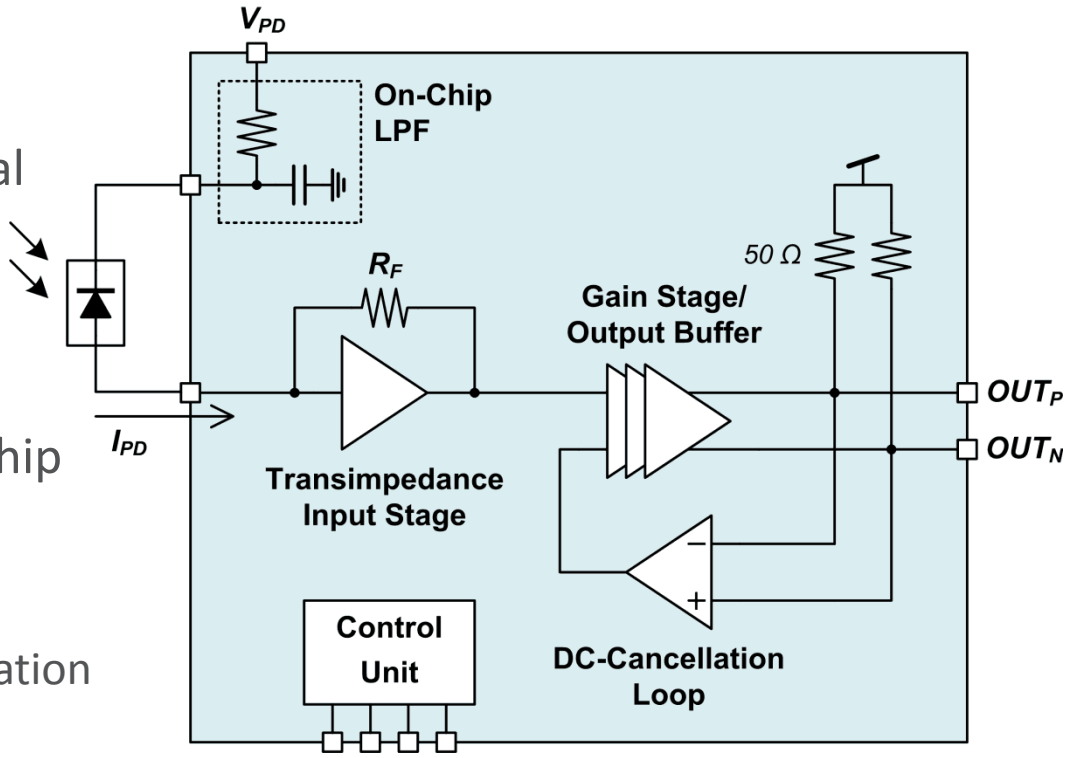
- Constant VCSEL current swing level over the wide temperature range
- Enough speed for ***>25-Gb/s*** operation
- Bandwidth extension by pre-emphasis

< AC Response vs. Pre-Emphasis >

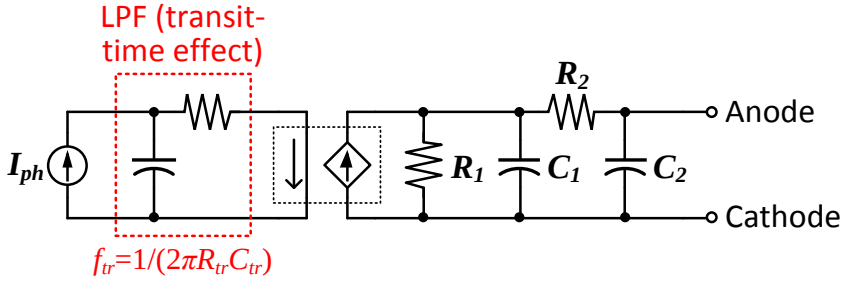


TIA – Features

- Low-noise input stage
- Output buffer for driving external differential 100-Ω load
- ***DC-cancellation loop*** for offset elimination
- External PD bias input with on-chip low-pass filter
- A variety of ***adjustability***
  - gain, output swing, jitter optimization
- Accurate design with PD ECM including ***transit-time effect***

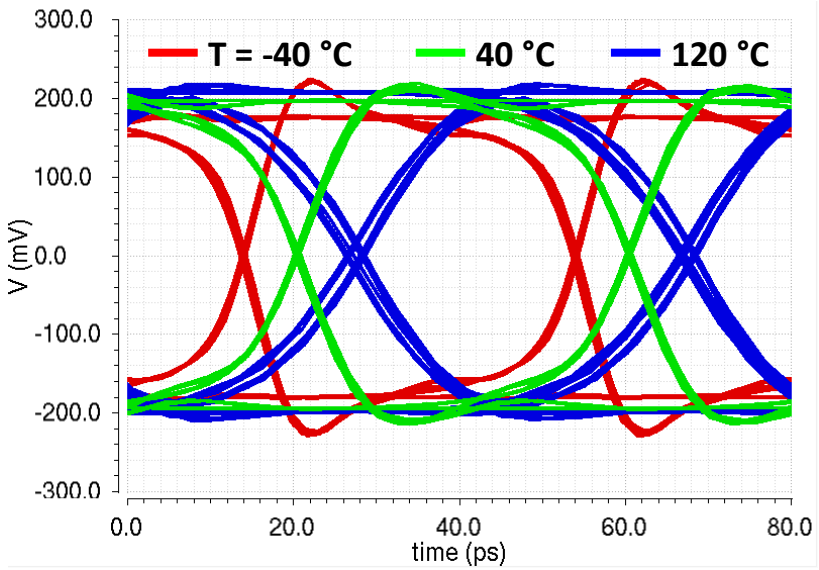


< PD Equivalent Circuit Model >

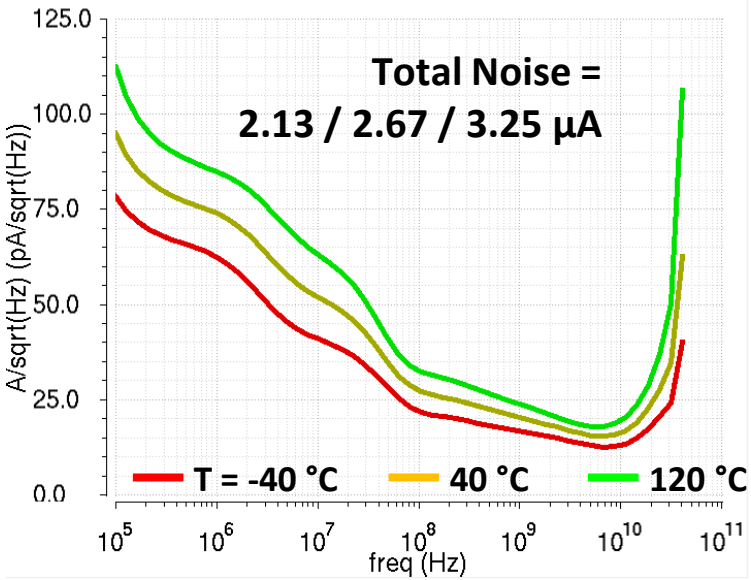


TIA – Simulation Results

< 25G Eye vs. Temperature >



< Input Noise vs. Temperature >



Post-layout simulations with PD ECM

- Endurable performance degradation at the extreme temperature

  → Can be optimized further by gain & jitter control
- Very good noise performance: receiver sensitivity better than ***–6 dBm***

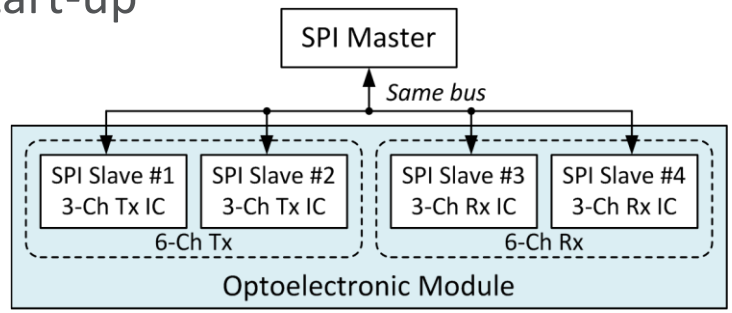
Digital Control

Channel-independent digital control via SPI-standard serial interface

- Power-on-reset (PoR) circuit for autonomous start-up
- Non-zero preset value for each control register

Proven RH design by using ***SGB25RH libraries***

- Digital Standard Cell and IO Libraries
- TMR flip-flop design for SPI core



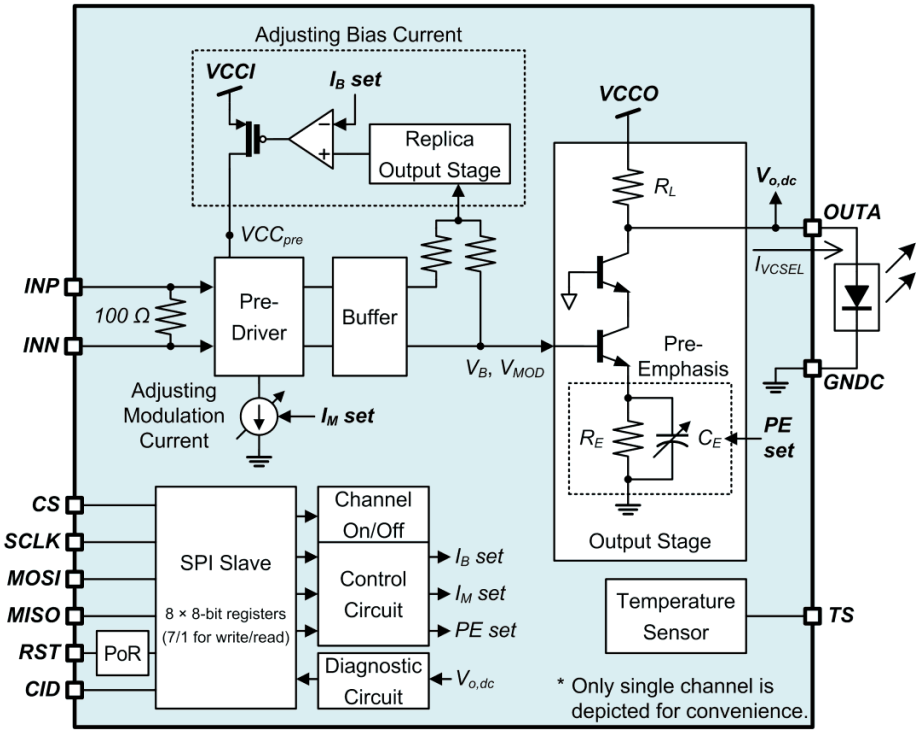
< Control Parameters >

Tx/Rx	Control	# Bit per Channel	Note
Common	Channel ON/OFF	1	
Tx	VCSEL bias current	4 (16 levels)	0 – 5 mA @ R_{VCSEL} = 160 Ω
	VCSEL mod. Current	4 (16 levels)	0 – 5 mA_{pp} @ R_{VCSEL} = 160 Ω
	Pre-emphasis	3 (8 levels)	
Rx	Jitter	4 (16 levels)	
	Gain	4 (16 levels)	4 – 13 kΩ
	Output amplitude	4 (16 levels)	0 – 750 mV_{ppd}

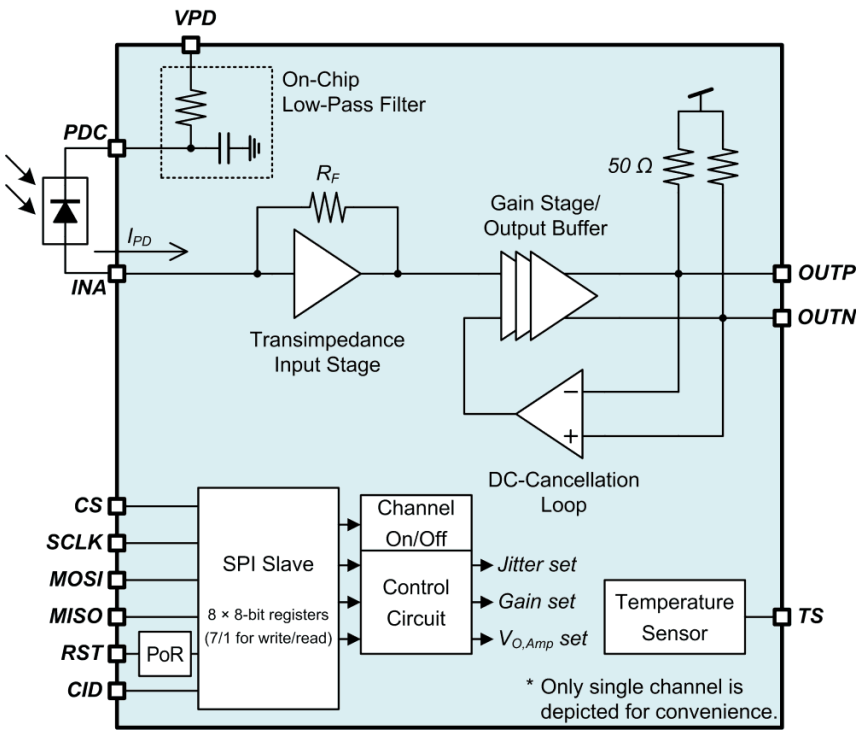
Gen2 IC Design

- Analog cores: updated from the Gen1 cores by using the final VCSEL/PD models
- RH digital circuits: SPI, I/O pads, control/diagnostic circuits
- Very low power consumption
  - Driver: 45 mW/channel & TIA: 65 mW/channel

< Gen2 Driver >



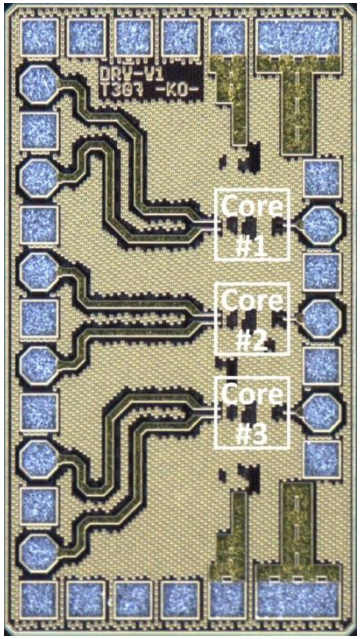
< Gen2 TIA >



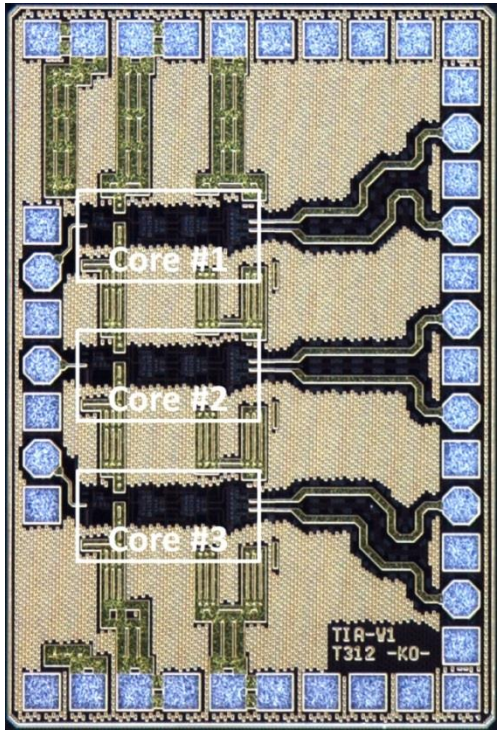
IC Fabrication

- IHP's 0.25-µm SiGe:C BiCMOS SG25H4 technology
- Gen1 ICs: designed, fabricated, tested
- Gen2 ICs: designed, fabricated

< Gen1 Driver >

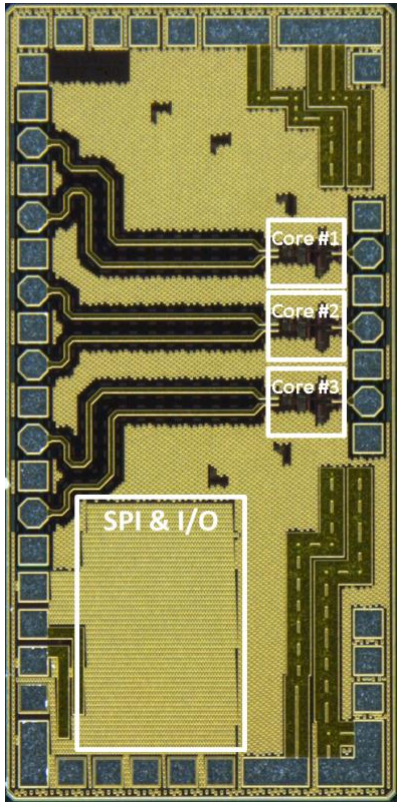


< Gen1 TIA >



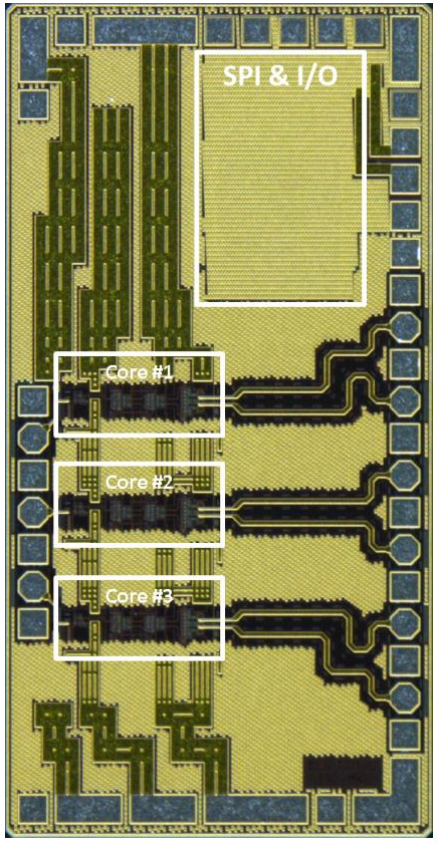
1.14 mm × 2.24 mm

< Gen2 Driver >



1.24 mm × 2.34 mm

< Gen2 TIA >

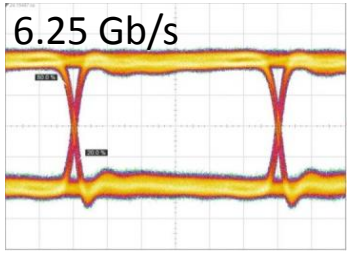


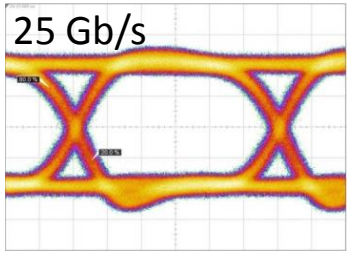
Measurement Results – Gen1 VCSEL Driver

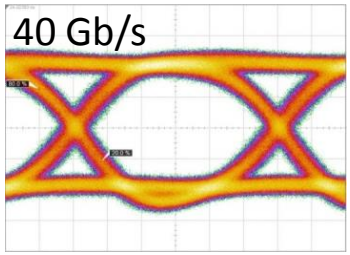
On-Wafer Electrical Measurement With 50-Ω Load

- Clean eye-diagrams up to 40 Gb/s
- Good agreement between simulation (blue lines) and measurement
- Good array uniformity

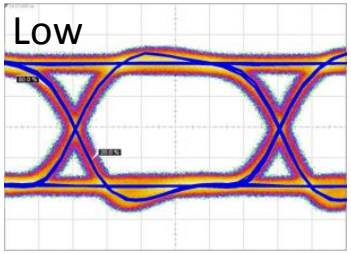
< vs. Data Rate >

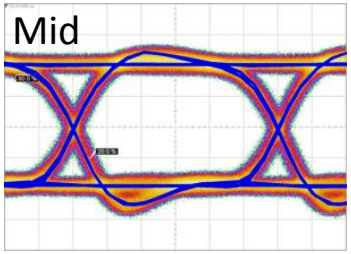


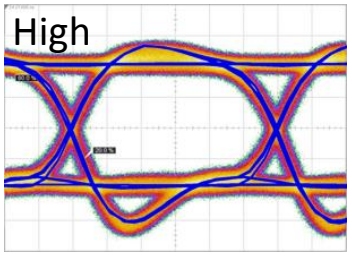




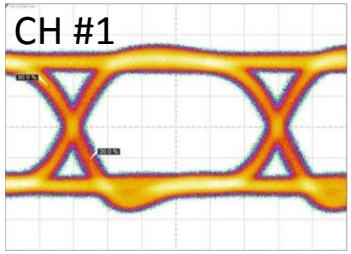
< vs. Pre-Emphasis >

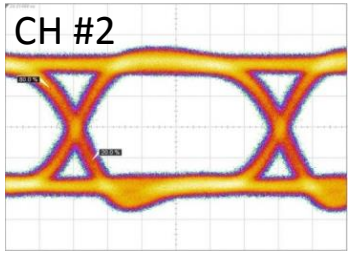


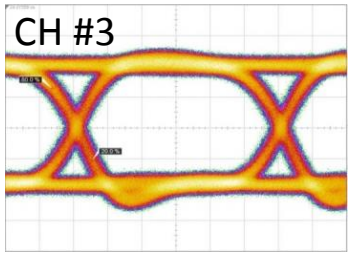




< vs. Channel >





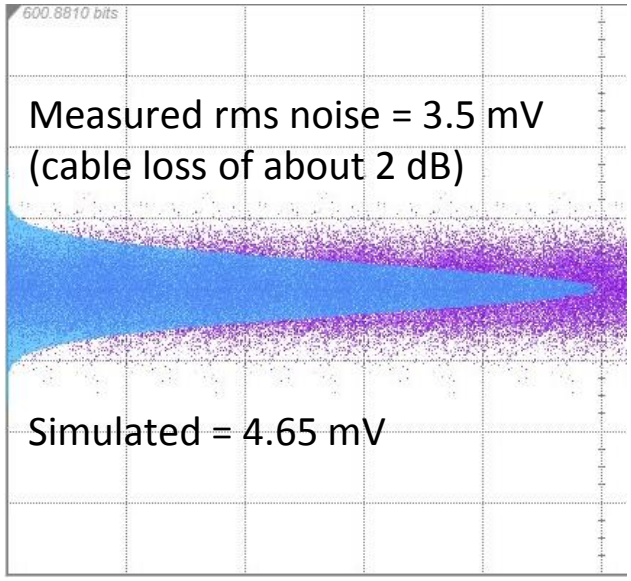


Measurement Results – Gen1 TIA

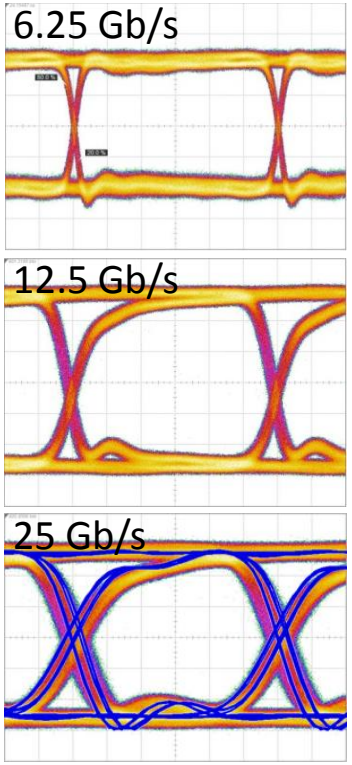
On-Wafer Electrical Measurement With 50-Ω Source

- Measured output noise matched to simulated one
- Clean eye-diagrams up to 25 Gb/s (Performance will be improved with real PD.)
- Good agreement between simulation and measurement
- Good array uniformity

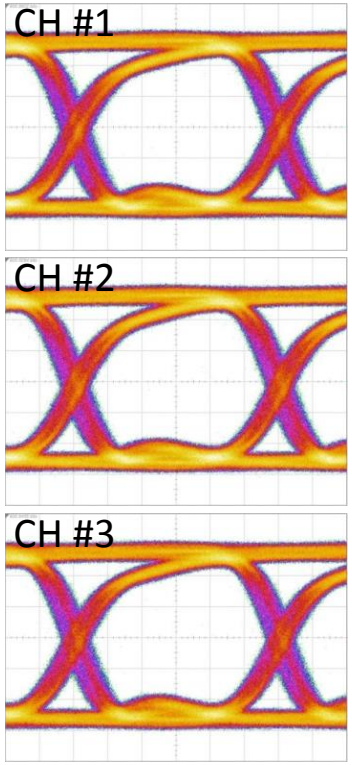
< Output Noise Voltage >



< vs. Data Rate >



< vs. Channel >



Conclusion

- Monolithic SiGe BiCMOS VCSEL driver and TIA ICs for multi-channel optical transceivers for space have been developed.
- The Gen1 ICs have been electrically characterized up to 25 Gb/s for the TIA and even up to 40 Gb/s for the driver.
- The Gen2 ICs with radiation-hardened digital control circuits have been fabricated and will be tested soon.

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Thank you for your attention!

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