25-Gb/s/Channel VCSEL Driver and Transimpedance Amplifier Array ICs in 0.25-µm SiGe:C BiCMOS Technology for Space Applications

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Abstract

We present monolithic VCESL driver and TIA ICs for multi-channel optical transceivers for space. The ICs provide 3 independent channels and are targeted to operate at the highest data rate of 25 Gb/s/channel and the lowest total power consumption of 5 mW/Gb/s. The driver for common-cathode VCSEL arrays consists of pre-driver, buffer, and output stage. The TIA IC consists of transimpedance input stage, gain stage, output buffer, and DC-cancellation loop. Each IC provides a standard SPI serial interface for advanced digital controllability. The radiation hardness is achieved by triple modular redundancy flip-flop design. Two generations of the ICs have been implemented with IHP's 0.25-µm SiGe:C BiCMOS technology. The Gen-1 ICs with simple analog control circuits have been electrically characterized by on-wafer measurements and successfully demonstrated with eye-diagram measurements up to 25 Gb/s for the TIA and even up to 40 Gb/s for the driver. The Gen-2 ICs equipped with full digital control circuits including SPI are under fabrication. They are expected to have very low power consumption of 1.8 and 2.6 mW/Gb/s for the driver and the TIA, respectively.

I. Introduction

As the demand for broadband communication has been explosively increasing, next-generation telecom satellites are needed to offer very high data rate connections, bringing massive digital data transfers between boards, modules, and equipment in a satellite. 850-nm optical interconnects based on vertical cavity surface emitting laser (VCSEL), photodiode (PD), and multimode fiber are the most attractive solutions for future intra-satellite networks as they can provide high-bandwidth, low-power, small-size and lightweight connections at a low cost [1]. In such a system, electronic ICs providing higher bandwidth and lower power consumption per data rate are very critical since at a given aggregated throughput these parameters determine the number of required parallel links and the overall power consumption.

In this work we present monolithic VCESL driver and transimpedance amplifier (TIA) ICs for multi-channel optical transceivers for space. The ICs provide three independent channels and are targeted to operate at the highest data rate of 25 Gb/s/channel and the lowest total power consumption of 5 mW/Gb/s. The ICs are equipped with a standard serial peripheral interface (SPI) for advanced digital controllability.

The paper is organized as follows: in Section II the circuit design methodology is described. Section II-A and II-B present the VCSEL driver and the TIA, respectively. Section II-C presents the digital control part. In Section III, high-speed characterization results of the driver and the TIA are reported. Finally Section IV concludes the paper.

II. Circuit Design

The 3-channel 25-Gb/s VCSEL driver and TIA ICs have been developed with the two-generation approach. The first generation (Gen-1) ICs focus on verification of high-speed signal path so they contain only analog control circuits for simple operation adjustment. And the Gen-2 ICs include advanced control functions with SPI. The ICs are realized with IHP's 0.25-µm SiGe:C BiCMOS technology.

A. VCSEL Driver

The VCSEL driver is designed to directly modulate high-speed common-cathode VCSEL arrays.

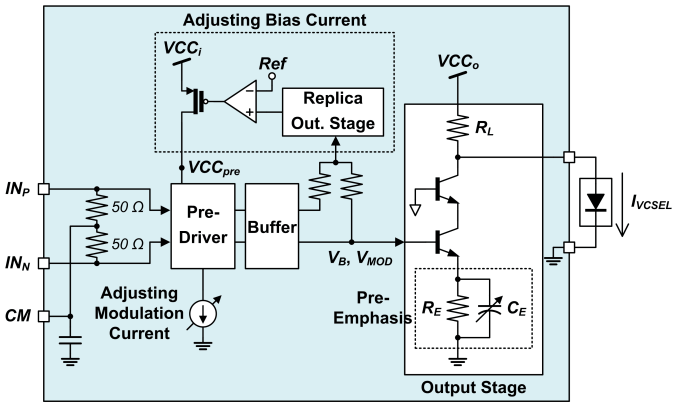

Figure 1: Schematic of VCSEL driver core.

The schematic of the single-channel driver core is shown in Figure 1. It consists of pre-driver, buffer, output stage with RC pre-emphasis, and feedback replica bias and control circuits. Differential input signals from digital modules come into the pre-driver with differential 100-Ω termination for input matching. VCSEL driving currents generated from the output stage are applied into the VCSEL anode. A ground for the VCSEL common cathode is provided from the driver.

The output stage is the most critical building block in low-power design because it consumes most of the total power dissipation in order to drive a large amount of currents to the VCSEL. In our driver a single-ended structure is used for output stage so that it can reduce power dissipation by up to 50% comparing to conventional differential structures.

On the other hand, the single-ended output stage is so sensitive to input voltage level that it's difficult to control the driving currents accurately. This sensitive biasing of the output stage is solved by using replica output stage and feedback loop. The exact amount of currents flowing through the output stage is read from the replica output stage and this information is compared with a reference signal representing the desired current level, and fed back.

A capacitive emitter degeneration technique is used for pre-emphasis. It improves the speed of the driver itself, and

moreover it can compensate speed reduction of the optical link, mainly from VCSELs and PDs. The pre-emphasis level can be optimized by adjusting a variable capacitor (C_E) with its control voltage.

The pre-driver and the buffer are biased with on-chip proportional to absolute temperature (PTAT) current sources and this enables bias and modulation currents to the VCSEL to be temperature-independent. The VCSEL bias current can be adjusted by changing the reference voltage (*Ref*) and the output stage supply voltage (VCC_o). The VCSEL modulation current also can be adjusted by changing the PTAT bias current of the pre-driver. The bias and modulation currents have the typical values of 3 mA and 3 mA_{pp} and can go higher up to 5 mA and 5 mA_{pp}, in order to prepare VCSEL performance degradation with time and temperature.

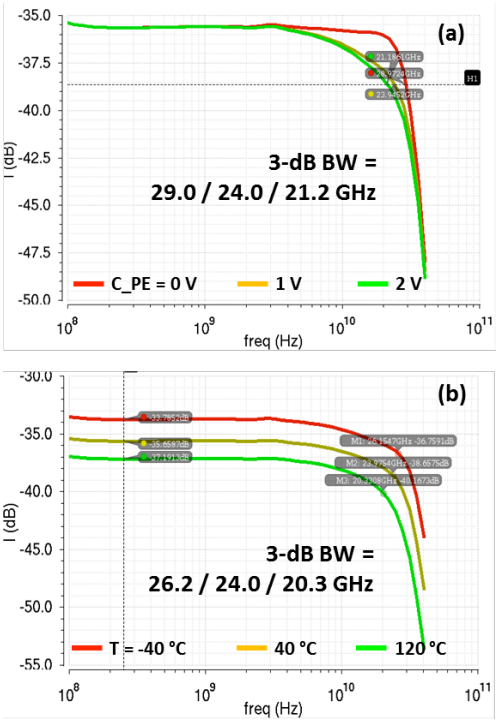

Figure 2: Post-layout simulated frequency responses of VCSEL driver at different (a) pre-emphasis levels and (b) operating temperatures.

Figure 2 and 3 show post-layout simulation results of the designed driver core. Figure 2 shows the frequency responses which are from the differential input voltage to the VCSEL output current (I_{VCSEL}). The responses at different pre-emphasis levels show that the bandwidth can be extended from 21.2 GHz up to 29.0 GHz which is very promising for faster data transmission than 25 Gb/s. Also, as shown in Figure 2 (b), the driver is designed to cover a wide temperature range from –40 °C to +120 °C. . At the nominal temperature of 40 °C, the 3-dB bandwidth is 24.0 GHz. The bandwidth is degraded as the temperature increases, and it goes down to 20.3 GHz at the highest temperature of 120 °C, which is still enough for 25-Gb/s operation.

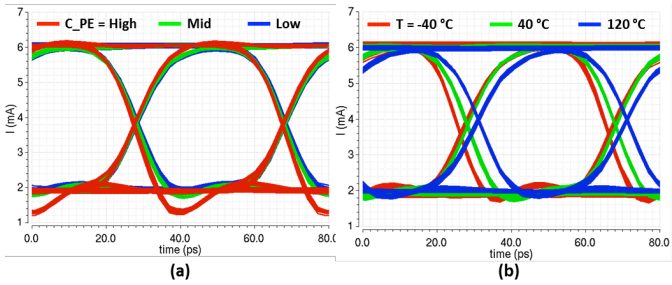

Figure 3: Post-layout simulated eye diagrams of VCSEL driver at different (a) pre-emphasis levels and (b) operating temperatures.

Figure 3 shows post-layout simulated eye diagrams at the data rate of 25 Gb/s and VCSEL bias/modulation currents of 4/4 mA. Figure 3 (a) shows the effect of controlling the pre-emphasis level. At stronger pre-emphasis the rise/fall time is enhanced and the pre-emphasis peak is occurred which can be used for compensating further band-limited optical link characteristics. The diagrams at different temperatures show that the PTAT current sources are well optimized since the DC level (bias current) and the swing (modulation current) do not change within the wide temperature range. Degradation of rise/fall time at high temperature due to the decreased bandwidth can be overcome by optimizing the pre-emphasis level.

B. Transimpedance Amplifier

The TIA converts small input currents from high-speed common-cathode PD arrays into differential voltage output.

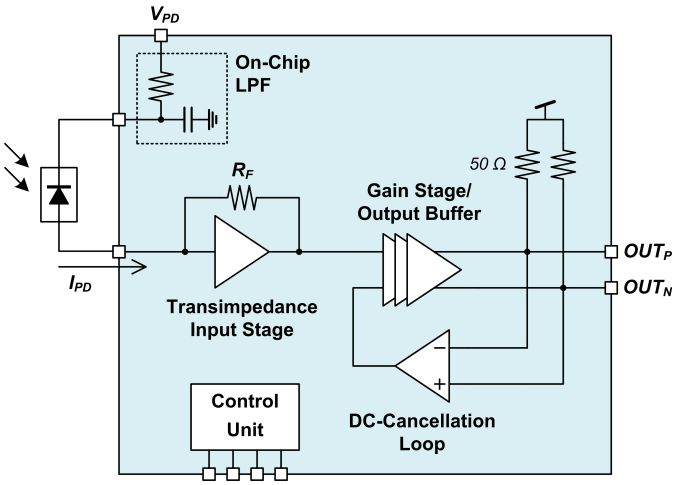

Figure 4: Schematic of TIA core.

Figure 4 shows the schematic of the TIA core [2]. It consists of transimpedance input stage, gain stage including output buffer, DC-cancellation loop, and bias and control circuits. The PD anode is connected to the TIA input pin, and differential output signals from TIA are applied to off-chip devices with differential 100-Ω termination for output matching. The PD cathode bias voltage is not generated by the IC but provided externally (V_{PD}) because it is higher than the circuit supply voltage. It is fed to the PD cathode via on-chip RC low-pass filter which has a cut-off frequency of around 100 MHz. The photo-generated current from the PD is converted to voltage by the input stage, and amplified to a sufficient voltage swing for the next stage. The output buffer enables to drive external differential 100-Ω load. Because the input stage is single-ended, the DC offset can be occurred at differential TIA output. A DC-cancellation feedback loop is

employed to eliminate the offset. In order to give freedom to performance optimization, the IC has a diversity of adjustability, which are gain, output swing, jitter, and zero crossing point controls.

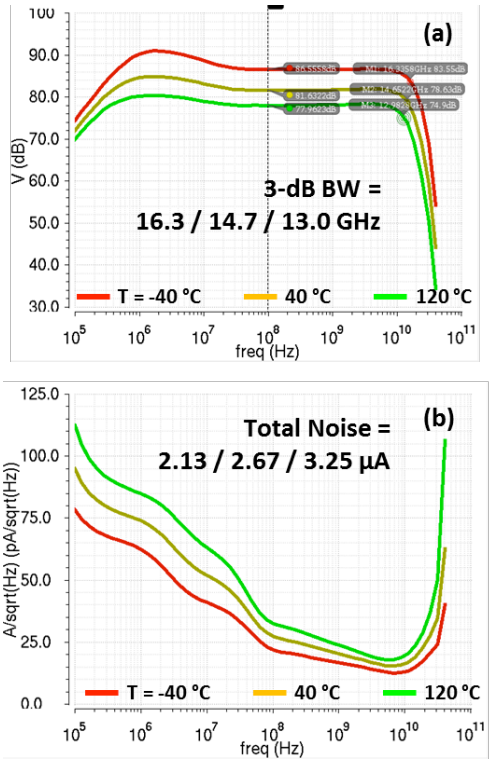

Figure 5: Post-layout simulated (a) transimpedance gain and (b) input-referred noise current density responses of TIA at different operating temperatures.

Figure 5 (a) shows the simulated transimpedance gain responses of TIA at different temperatures and process corners. At the nominal temperature of 40 °C, the TIA gain is about 81.6 dB (or 12.0 kΩ) and the 3-dB bandwidth is 14.7 GHz which is adequate to 25-Gb/s transmission. As the temperature changes, the gain and the bandwidth varies from 78.0 to 86.6 dB and from 13.0 to 16.3 GHz, respectively. Decreased bandwidth can be overcome by pre-emphasis at the transmitter.

The input-referred noise current density responses at different temperatures are shown in Figure 5 (b). Total input noise current integrated up to 20 GHz is about 2.67 µA at the nominal temperature and varies from 2.13 to 3.25 µA as the temperature changes.

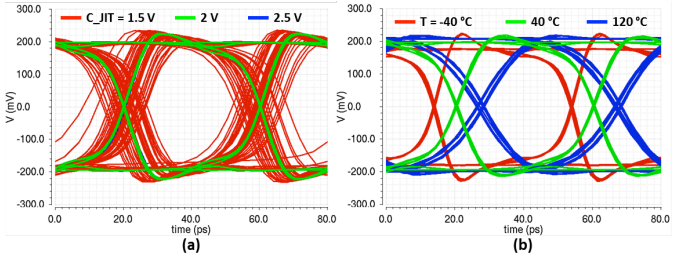

Figure 6: Post-layout simulated eye diagrams of VCSEL driver at different (a) jitter optimizations and (b) operating temperatures.

Figure 6 shows the eye diagrams at the data rate of 25 Gb/s and the input PD current of 100 μA_{pp}. The eye diagrams when adjusting the jitter optimization control voltages (C_JIT) show that jitter performance is optimized at 2 V, comparing to the eye diagram at 1.5 V which shows large deterministic jitter. The effect of different operating temperatures can be seen in Figure 6 (b). Degradation in jitter and rise/fall time at the high temperature is not significant and can be improved by optimizing bias voltages.

C. *Digital Control*

The Gen-2 ICs are equipped with a digital serial interface in order to enable advanced digital control functions such as channel on/off function, various digital controls, and diagnostic/status information.

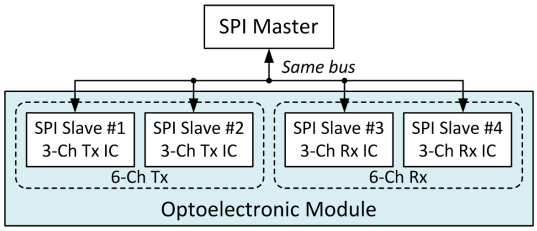

Figure 7: Serial communication interface configuration for 6-channel optoelectronic module.

Figure 7 shows the serial communication interface configuration for the optoelectronic module using SPI standard. Since the 6-channel transceiver module consists of two 3-channel driver (Tx) ICs and two 3-channel TIA (Rx) ICs, All 4 ICs should be connected to the same bus but controlled independently. Also, it should support autonomous start-up operation with pre-defined initial control values when the master controller is not connected.

The block diagram of the SPI slave is shown in Figure 8. The SPI block has basic SPI bus pins (SCLK, CS, MOSI, MISO) and a reset (RST) pin equipped with automatic power-on reset circuit. 2-bit address Addr<0,1> is used to indicate the chip ID necessary since identical SPI slaves are used for all 4 chips (Tx/Rx #1/2). It has 7/1 write/read registers (8 bits each) and the preset values for the write registers can be set by connecting each init pin with logic high or low. Supply voltage for I/O is downscaled from 3.3 V to 2.5 V to enhance single-event latch-up tolerance and reliability. In overall digital circuit design, triple modular redundancy flip-flops are used to enhance the radiation hardness.

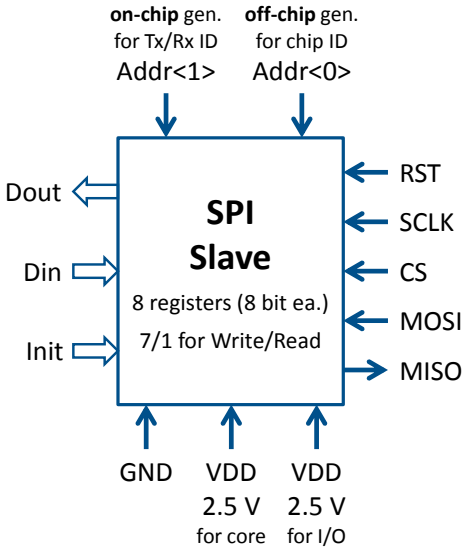

Figure 8: Block diagram of SPI.

Control parameters of Tx and Rx using digital SPI are summarized in Table 1.

Table 1: Control parameters of Tx and Rx.

Tx/Rx	Control	# Bit per Channel	Note
Common	Channel ON/OFF	1	
Tx	VCSEL bias current	4	0 – 5 mA
	VCSEL mod. current	4	0 – 5 mA_{pp}
	Pre-emphasis	3	
Rx	Jitter	4	
	Gain	4	4 to 13 kΩ
	Output amplitude	4	0 to 750 mV_{ppd}

III. Measurement Results

The Gen-1 3-channel 25-Gb/s VCSEL driver and TIA ICs have been fabricated with IHP's 0.25-µm SiGe:C BiCMOS technology. The chip photos of each IC are shown in Figure 9. They have three identical circuit cores and occupy the dimensions of 0.74 mm × 1.34 mm (driver) and 1.04 mm × 1.54 mm (TIA). The area for TIA is bigger than that of the driver because the gain stage/output buffer chain occupies quite much area.

Their performances have been characterized with on-wafer electrical measurements with 50-Ω equipment instead of a real VCSEL/PD array. Figure 10 shows the measured eye diagrams of the VCSEL driver at different cases. The eye diagrams at different data rates show that the driver operates well at lower data rates of 6.25 Gb/s for low bit rate option and even up to 40 Gb/s. The eye diagrams at different channels show good inter-channel uniformity.

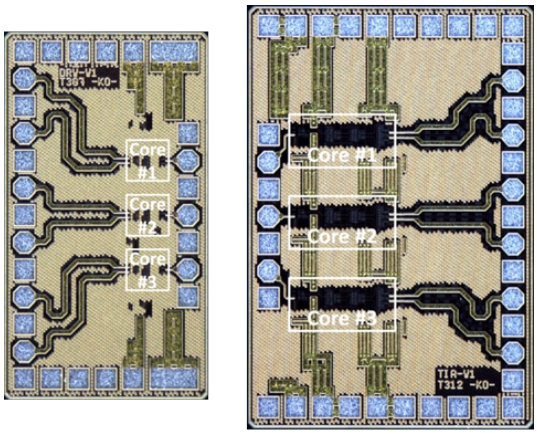

Figure 9: Chip photos of Gen-1 VCSEL driver and TIA.

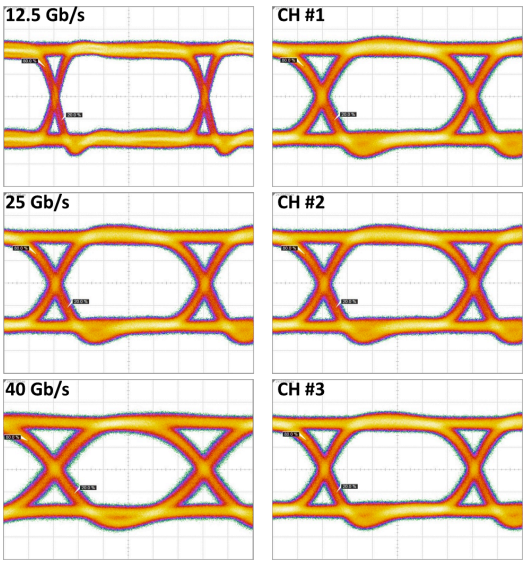

Figure 10: Measured eye diagrams of Gen-1 VCSEL driver.

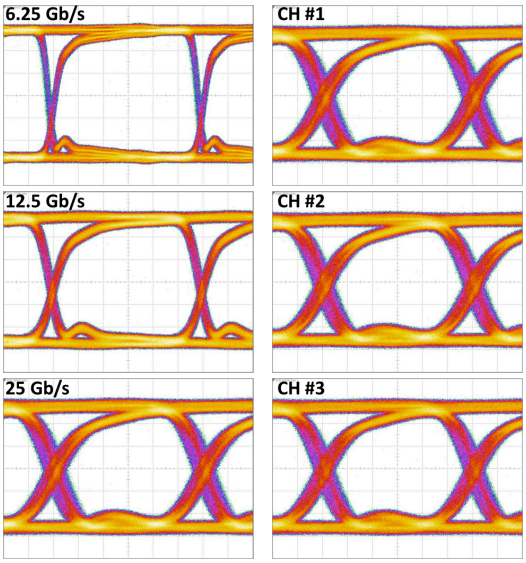

Figure 11: Measured eye diagrams of Gen-1 TIA.

Figure 11 shows the measured eye diagrams of the TIA at different cases. The eye diagrams at different data rates show that the TIA operates well from 6.25 to 25 Gb/s with clear open eyes. Also they show good uniformity among three channels. Figure 12 shows the output noise voltage and its histogram at the single-ended output measured by using an oscilloscope with channel bandwidth of 50 GHz. The input probe was detached from the chip to measure noise components only generated by the TIA. The measured rms value is about 3.5 mV and this is matched to the simulation result of 4.65 mV if considering the cable loss of about 2 dB from the measurement setup.

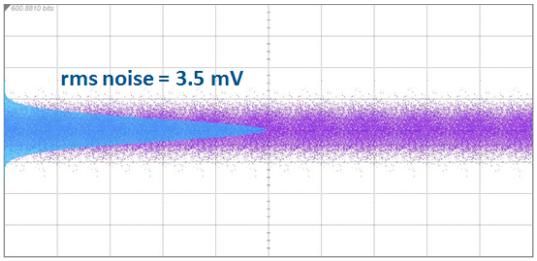

Figure 12: Measured output noise voltage of Gen-1 TIA.

IV. Conclusion

Monolithic SiGe BiCMOS VCESL driver and TIA ICs for multi-channel optical transceivers for space have been reported. The Gen-1 ICs have been electrically characterized up to 25 Gb/s for the TIA and even up to 40 Gb/s for the driver. The Gen-2 ICs with digital controls are under fabrication and rad-hard testing for Gen-2 ICs is under contemplation.

V. Acknowledgements

The research leading to these results has received funding from the European Union Seventh Framework Programme for research, technological development and demonstration under the Grant number 607274 (Multi-Gigabit, Scalable & Energy Efficient On-Board Digital Processors Employing Multi-Core, Vertical, Embedded Opto-Electronic Engines). The authors would like to thank the colleagues who have contributed the work.

VI. References

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