Si and CdTe Detector Readout ASIC in 0.35µm CMOS for Energetic Electron Spectroscopy for Space Application.

I. Introduction

TARANIS (Tool for the Analysis of RAdiation from lightNIng and Sprites) is a microsatellite aimed to atmospheric storms study. It embarks among other instruments IDEE (Instrument Détecteur d'Electron Energétique) which is dedicated to energetic electron characterization in the range from 70keV to 4Mev. To cover such a wide range, two types of detectors are required: Silicon (Si) and Cadmium Telluride (CdTe) based detector for the 70keV to 700keV and for the 300keV to 4MeV respectively. Si detectors are placed in front of CdTe detectors for angle measurement. Although the readout architecture of both detectors are similar, the time constants involved in collection of the charges for Si and CdTe are differents by almost 21 decades (60ns for Si and 3µs for CdTe). Two different readout circuits are thus required. CdTe type channels need to make use of Pole Zero Cancellation (PZC) technique in order not to impede the frequency of operation. Performance of the design has been characterized on a test board as well as interfaced with detectors. Finally, results of its characterized Single Event Latchup (SEL) performance is given.

II. ASIC design

Both type of channel are based on a charge sensitive amplifier (CSA), a CR-RC pulse shaper followed by a peak detector and a 8-bit ADC (analog to digital converter). The ADC design is the same for both channels [1].

A. Si and CdTe Analog Front ends

Si and CdTe channels both make use of a RC CSA for integration of the input charge. The CSA is based on a transconductance amplifier (OTA) with a feedback capacitor Cf to perform the charge integration and a resistor feedback Rf to discharge Cf and to provide a DC path for the detector leakage current. Such a differential approach improves the rejection of common mode external noise. In addition, based on the methodology extensively described in [1], sizing as well as biasing of the transistors are optimized for internal noise and bandwidth performance. The feedback R_f and C_f values depend on the required time constant. Then, in order to improve the Signal-to-Noise Ratio (SNR) and improve the signal amplitude, the CSA output voltage is filtered by a pulse shaper (PS). A first order semi-Gaussian PS (RC-CR bandpass filter) is used as PS for its high-speed response and its active bandpass filtering characteristics.

The relaxation time of the circuit defines the frequency performance of the readout channel. While 1-µs conversion time of the ADC is the limiting criteria for Si channel, time constants of CdTe analog circuit set the limit for CdTe channel. It becomes necessary to eliminate the undershoot created by the 2nd pole of the CSA-PS chain. A PZC circuit is thus implemented by adding an extra resistor Rz in parallel to the pulse shaper derivation circuit (Cd, Rd) as shown in Fig 1.

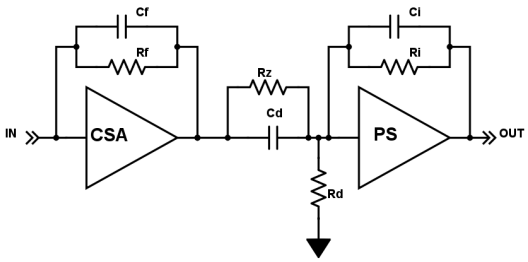

Figure 1: CdTe channel analog Front End simplified schematic

B. Peak detector and 8-bit ADC

At the output of the pulse shaper, the signal amplitude is proportional to the incoming particle energy, a peak detector searches the maximum value of the signal in a track and hold manner. The final value is digitized by an 8-bit SAR ADC.

C. Layout considerations

The circuit has been implemented in AMS 0.35µm HV CMOS technology. This technology has a triple well option allowing isolation of transistors from the bulk. This is an advantage in terms of noise and crosstalk reduction. To further reduce crosstalk, power supply of the analog part of the channel is isolated from the peak detection and ADC. A microphotograph of the chip is shown in Figure 2.

8 CdTe channels and 5 Si channels are integrated in the chip.

III. ASIC characterization

The ASIC (Fig. 2) has been characterized on a test board. A 1-nF injection capacitance driven by a signal generator has been used to generate the input charge. The ASIC input is loaded by a 40-pF capacitance representing the detector.

Noise measurement has been performed by sending 1000 events and standard deviation is computed. ENC of Si is of 3120e- while CdTe ENC is 2335e-, time constant of CdTe PS provides a better filtering of the noise.

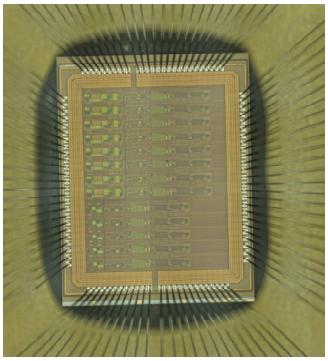

Figure 2: Si and CdTe readout ASIC microphotograph

IV. Interface Test with Si and CdTe detectors

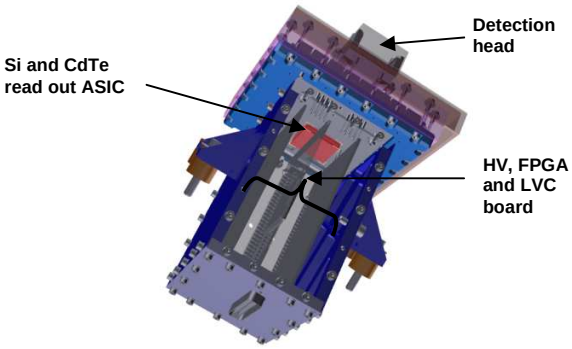

Figure 3: 3D model of the IDEE instrument

The ASIC is mounted in the instrument electronic box (Fig. 3). The electronic box is composed of a High Voltage, a FPGA and a Low Voltage board. The HV board generates the 100 and 300V necessary for Si and CdTe detectors biasing. The FPGA encapsulates the detected energy in the appropriate data frame and the low voltage board takes care of the supply voltage for each electronic board.

The detector head is made of 8 CdTe detectors placed behind a strip of 5 Silicon pixels. The centered Silicon pixel is about 40 times smaller than the others. It will be used alone for the South Atlantic Anomaly crossing that might saturate the instrument otherwise.

The detector head is exposed to a 207Bi source for final characterization of the instrument. The specified resolution of the instrument being 6 bits, only the first 6 bits of ASICs output are being collected by the FPGA. The spectrum of the 207Bi is given below. The source being centered in the middle of the Si detector strip, Si1 and Si3 receive the highest density of particles. Si2 being the smallest detector pixel the probability of having a count is small (Fig. 4).

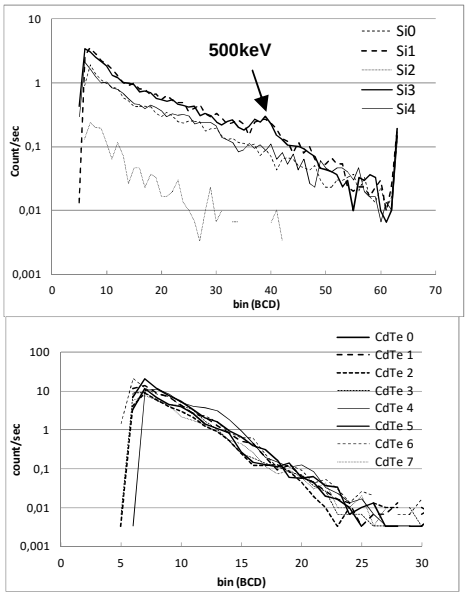

Figure 4: Si and CdTe 207Bi source spectrum

The electron emission around 500keV can be clearly seen on the Si spectrum while in the CdTe spectrum no obvious electron energy can be seen mainly due to obstacles between the source and CdTe detectors in the detection head.

V. Radiation Test

Heavy ion test has been performed at RADEF at University of Jyvaskyla (Finland) using their cyclotron accelerator test facility. Two samples were exposed to krypton ion at a tilt angle of 37°deg and showed a Single Event Latchup (SEL) occurring at a Linear Energy Transfer (LET) level of 40MeV(mg/cm²). An analog de latching circuit on the test board detected the current surge on the chip supply voltage and powered it off. Functionality of the chip has been verified after occurrence of latch up event.

VI. Conclusion

A Si and CdTe detector readout ASIC for Energetic Electron Spectroscopy has been presented, it features a detection range from 70keV to 4MeV. The ENC Si is of 3120e- for Si channel and CdTe ENC is 2335e-. Both are loaded at the input by a 40pF capacitance. It has been tested both on a test board and in the electronic box of the instrument. SEL occurs at a LET of 40Mev(mg/cm²).

VII. References

[1] F. Bouyjou, O. D. Bernal, H. Tap, J.A. Sauvaud and P. Jean, " Low Noise CMOS Analog Front-End Circuit With an 8-bit 1-MS/s ADC for Silicon Sensors for Space Applications," *IEEE Sensors Journal.*, vol. 14, no. 5, pp. 1617-1624, May. 2014.

[2] P. Grybos, R. Szczygiel, " Pole-Zero Cancellation Circuit With Pulse Pile-Up Tracking System for Low Noise Charge-Sensitive Amplifiers " , *IEEE Transaction on Nuclear Science*, vol. 55, no. 1, February 2008.