Development of a Digital Temperature Transducer ASIC in a 28 nm FD-SOI CMOS Process for a Spaceborne Low Power Sensor Bus

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Abstract

A digital temperature transducer ASIC is being developed and prototyped in a 28 nm Fully Depleted Silicon on Insulator (FD-SOI) CMOS process. It features high performance and robustness at low power consumption. A thorough analysis defines the requirements for the transducer development, which are imposed by a future spacecraft application. The new serial bus sensor network architecture and harsh environmental conditions are the main challenges.

In order to achieve the required measurement inaccuracy of up to ±1 °C, over an extended temperature range spanning from -40 °C to +125 °C, several design measures are considered. A resolution of 0.1 °C is specified for the read-out circuitry. An integrated circuit "AMBER1" was developed in the frame of the European research project THINGS2DO, in order to prototype the central components of the temperature transducer. Among the various analog/mixed-signal and RF circuit blocks, a 1st order sigma-delta modulator and its constituent operational transconductance amplifier were integrated in AMBER1. The integrated circuit, in the new semiconductor process, was taped out in November 2015.

I. INTRODUCTION

Future spacecraft shall make use of electrical sensor networks based on serial buses, which provide both flexible and efficient ways to monitor important parameters. Since spacecraft housekeeping data is vital to a space mission, the reliability of such new sensor systems is crucial for their success. Traditional architectures rely on highly reliable sensors, interconnections and interrogators. It is usually difficult to improve the cost efficiency of such a design. A partial reduction of the temperature sensor count by improving the thermal design and heat transfer of the satellite was investigated at OHB System AG. Future spacecraft sensor networks, predominantly temperature measurement systems, shall however primarily reduce the cost of sensors, their interfaces, and interrogators, thus allowing to achieve high reliability by higher redundancy with better performance and cost effectiveness [1].

Large geostationary satellites typically employ several hundred resistive temperature sensors. These sensors are point-to-point wired to an acquisition unit, which is often a single central interrogator system. The application of platform temperature sensing was well suitable to introduce a new concept which shall reduce harness complexity and mass, while keeping system reliability, cost, and power consumption in mind.

Digital temperature sensors fabricated as integrated circuits (IC) have become a popular choice for use in thermal management systems in many commercial applications, featuring serial interfaces [2]. The temperature sensor and the digital interface circuitry for bus-type interfaces can be integrated on a single chip; thus enabling modularity and simplicity in the system design. Implementing a sensor network, in which the point-to-point connected resistive sensors are replaced with serially connected digital temperature
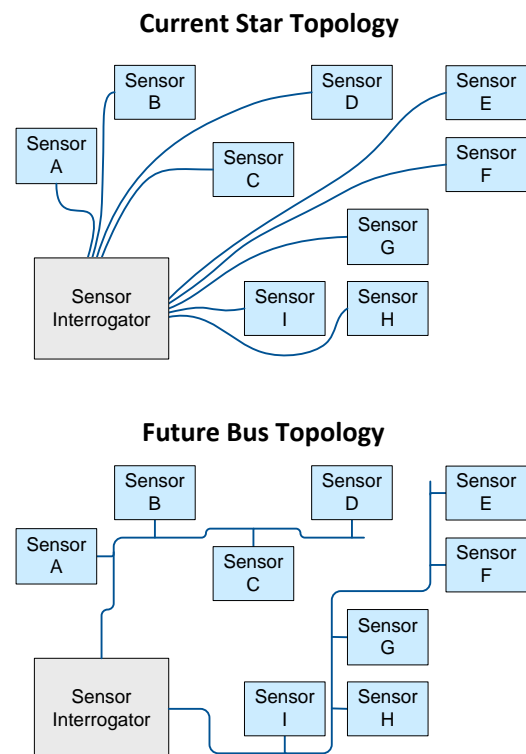

Figure 1: Replacing the star topology of the temperature sensor network with a bus topology

sensors, can result in a significant reduction in the amount of wiring. Figure 1 illustrates how the prevailing point-to-point star topology of the sensor-network shall be replaced with a bus topology.

The prevalence of portable electronics has caused a huge demand for process technologies that offer high performance at lower supply voltages and low leakage power. The 28 nm fully depleted silicon-on-insulator (FD-SOI) CMOS technology has become a state-of-the-art answer to this question. Apart from the various low power features offered by the FD-SOI devices, the inherent high robustness against transient radiation effects makes this CMOS process attractive for space electronics. The work carried out in the European research project called "Thin but Great Silicon to Design Objects (THINGS2DO)" project aims at realizing a sustainable ecosystem for the design and development of semiconductor components based on this modern technology in Europe [3]. An integrated circuit (IC) called "AMBER1" featuring various analog/mixed-signal and RF circuits blocks in the 28 nm FD-SOI CMOS process from STMicroelectronics was developed in the scope of this project [4].

This paper presents the system-level requirements of a temperature transducer (sensor) application-specific integrated circuit (ASIC), currently being developed in the 28 nm FD-SOI CMOS process. It shall become a part of a low power sensor bus system of a future spacecraft, where all the serially connected transducer ICs will communicate with sensor bus interrogator units. Section II gives a system-overview of the ASIC and describes its design requirements. A discussion about the FD-SOI CMOS technology and its radiation hardness properties is provided in section III. Section IV describes the AMBER1 IC that has been developed as an initial step towards realizing the temperature sensor ASIC. The target with AMBER1 was to design and validate some of the core components of the final system. The work presented in this paper is summarized in section V.

II. SYSTEM OVERVIEW

A. System-level requirements

The sensor network architecture on-board future spacecraft, introduced in section I, induces several requirements on the transducer, whose structure is depicted in Figure 2.

To maximize the benefit gained by the new concept, the packaging and wiring of the sensors needs to be optimized for a more cost-effective harness design and integration in the spacecraft. The main focus at the current stage of development, however, are the performance requirements and the reliability of the sensor system.

The targeted temperature measurement range is from -40 °C to +125 °C. The acquisition of temperature with a high resolution of 0.1 °C is desired in order to track dynamic temperature changes. A worst case measurement inaccuracy of ±1 °C is specified for the nominal operational temperature range of -20 °C to +20 °C. A maximum inaccuracy of ±3 °C is allowed for measuring temperatures outside this range. In order to meet the accuracy requirement, the analog-to-digital converter (ADC) has to provide a specific resolution, depending on the linearity of the temperature sensor. The
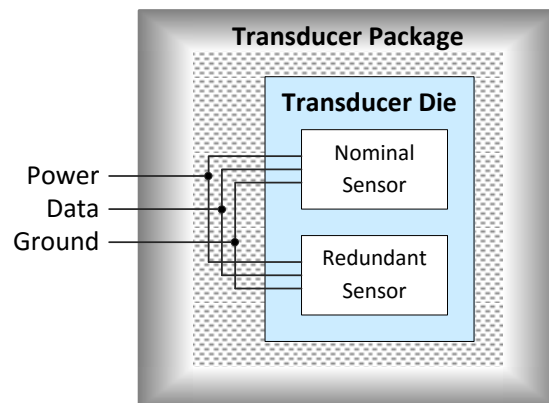

Figure 2: Packaged temperature transducer as final product

required target resolution of 0.1 °C translates to a minimum ADC resolution of 11 effective number of bits (ENOB).

The temperature transducer shall provide a serial interface, which allows the creation of sensor networks with up to 30 nodes, implemented as stubs. An optional analog input for an external temperature sensor is foreseen for higher flexibility in testing and developing new solutions based on the present transducer ASIC.

The application on geostationary satellites, with a typical lifetime of 15 years in-orbit operation, requires the sensor to support a 20-year lifetime which includes ground storage, manufacturing and testing.

High-energy particles are major concern for electronics in space, especially semiconductors with small feature sizes. Since the introduction of 65 nm and smaller gate lengths, single event effects (SEEs) have increasingly become a concern in ground based applications too. An SEE occurs when a sensitive node collects a sufficiently high charge from the carriers which are generated by an ionizing particle. If no suitable design provisions are implemented, the trend of lower critical charges in SRAM memory cells leads, in many CMOS technologies, to higher soft and hard error rates. One unit of measurement for the SEE sensitivity is the linear energy transfer (LET) threshold and the corresponding cross section, which is the probability of an SEE at a certain LET value. Digital space electronics aim at raising the SEE LET threshold on device level above the typically encountered particle spectrum. In geostationary orbit, lying in the equatorial plane at 6.6 Earth-radii and hereby outside the radiation belt with higher particle energies, the probability of encountering particles such as protons with 10 MeV or more is very low, except during solar events [5, 6]. The demanding geostationary transfer orbit (GTO) passed by the spacecraft is more crucial for the SEE tolerance requirement.

In the present case of the temperature transducer, a high LET threshold for hard faults, especially single event latchup (SEL) is required in order to allow not only a reliable operation of each sensing device, but also to avoid fault propagation of the sensor bus. Therefore, the used CMOS technology shall be classifiable as SEL-hard with an SEL-LET threshold >100 MeV·cm²/mg. Single Event Upsets (SEUs) in memory cells are of less concern because the digital design of transducer is required to provide error detection and correction for single faults. Occasional Multiple Bit Upsets (MBUs) which lead to

corrupted data are, on the other hand, identified by the measurement system and are thereby tolerable. After the application of error detection and correction (EDAC) mechanisms, an SEU LET threshold of >20 MeV·cm²/mg is deemed sufficient.

From the perspective of total ionizing radiation dose (TID), in order to determine the expected requirements, the placement of the transducer devices on the satellite has to be investigated. An analysis of the current geostationary satellite missions at OHB System AG showed that components mounted inside the spacecraft are subjected to radiation levels not higher than 100 krad for a 15-year mission. However, components outside the protective shielding can be subjected to over 5 Mrad. The strategy to not exceed the radiation load supported by the device is to optimize the packaging and operating place of the transducer in coordination with the obtained TID hardness of the device. In order to provide a certain flexibility in the application, a TID hardness of 300 krad is requested at die level.

B. System-level description

For implementation in CMOS technology, various temperature sensing concepts based on resistors, thermal diffusivity of silicon and MOSFET operating in the weak inversion region, are proposed in the literature [7]. However, the majority of the state-of-the-art digital temperature sensors employ parasitic bipolar transistors as the sensing element. With a single-point thermal calibration, inaccuracies less than ±0.2 °C have been reported for such sensors in the temperature range of -40 °C to 125 °C [7]. Figure 3 shows the working principle of a parasitic PNP bipolar transistor based temperature sensor. The difference between the base emitter voltages ΔV_{BE} between the two transistors are combined to generate a voltage V_{PTAT} that is proportional to the absolute temperature. The reference voltage V_{REF} is generated by adding V_{PTAT} to the base-emitter voltage V_{BE} of one of the transistors. The measured temperature is converted by the ADC as a ratio μ of the V_{PTAT} and V_{REF}, which is also proportional to the absolute temperature. It can be expressed as:
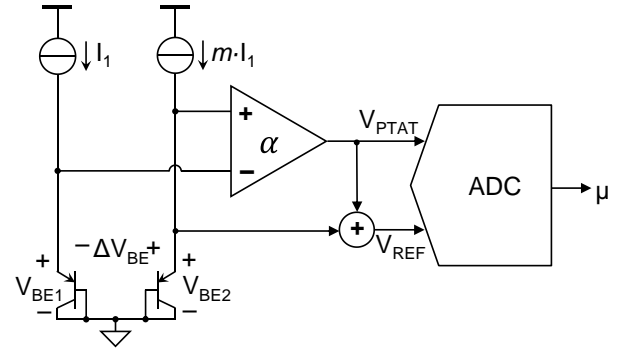

Figure 3: Working principle of a bipolar transistor based temperature sensor [8]

$$\mu = \frac{V_{PTAT}}{V_{REF}} = \frac{\alpha.\Delta V_{BE}}{V_{BE}+\alpha.\Delta V_{BE}} \qquad (1)$$

The measurement rate of the temperature sensors is limited by the thermal time constants of their packages; which are typically in the order of a few seconds. Therefore, sigma-delta ADCs are popularly used in such sensors because of their ability to trade low speed for high resolution [8].

On the system-level, the temperature transducer ASIC discussed in this paper, consists of three major design blocks: a bipolar transistor-based temperature sensor, a sigma-delta ADC, and a digital serial communication interface. Additionally, circuit blocks for the generation of the internal bias currents and low power digital calibration are included. The block diagram of the system is shown in Figure 4. A resolution of 14 bits is specified for the sigma-delta ADC.

The various design strategies that are considered for the mitigation of the radiation induced effects are as follows:

- System-level: Redundancy techniques such as triplicated clock tree, triplicated combinatorial logic and triplicated registers [9].
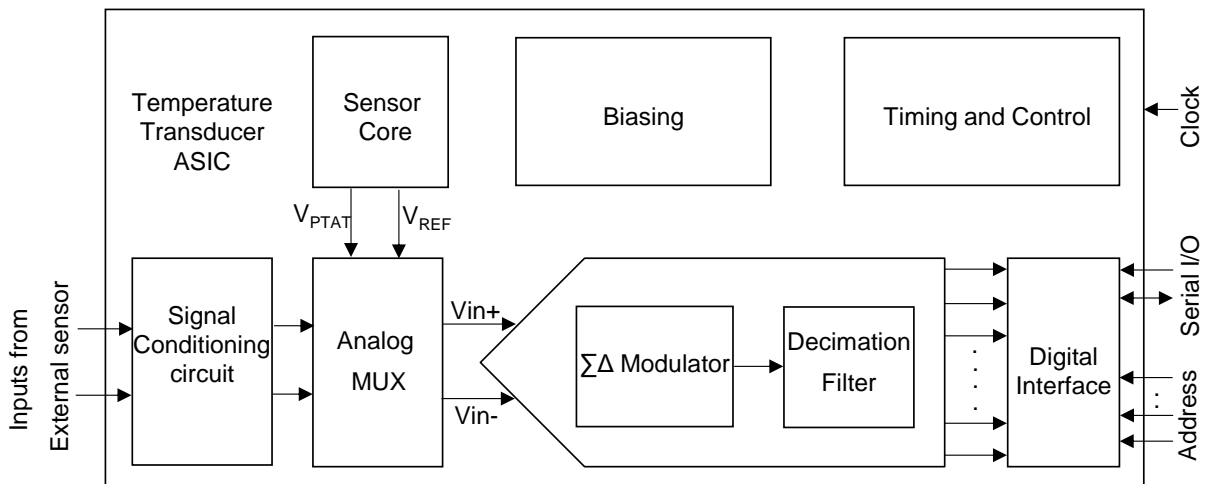

Figure 4: Block diagram of the temperature transducer ASIC

- Circuit-level: Optimal transistor sizing [10], circuit techniques for the compensation of leakage current [11], flicker noise and offset-compensation [12].
- Device-level: Design implementation on FD-SOI CMOS technology.
- Layout-level: Placement of guard-rings [13].

III. FD-SOI TECHNOLOGY

The 28 nm FD-SOI CMOS technology from STMicroelectronics features devices fabricated in a planar process with a 7 nm thin silicon film on a 25 nm Buried Oxide (BOX) [14] as shown in Figure 5. A minimum physical gate length of 24 nm can be achieved. The devices are fully depleted as the channel is left undoped because of the ultra-thin body. The construction of FD-SOI devices enables better control over the short channel effects. The 28 nm CMOS process offers many attractive features in this regard, namely, fast switching, low leakage currents, poly biasing and back-gate biasing for efficient power regulation, and expected latch-up immunity [15]. With the help of techniques like poly biasing and back-gate biasing the threshold voltage Vt can be effectively controlled to tune the circuit to achieve optimum performance and power-efficiency. Thanks to the BOX layer, these devices have reduced leakage currents and provide robustness against latch-up.

FD-SOI devices are found to be inherently resistant against transient ionizing radiation as a virtue of their construction. Reduction in the soft error rate (SER) is reported for designs based on these devices [16]. This can be attributed to the reduction in the effect of parasitic bipolar amplification, smaller sensitive volume for the ionizing particle to traverse, and inheren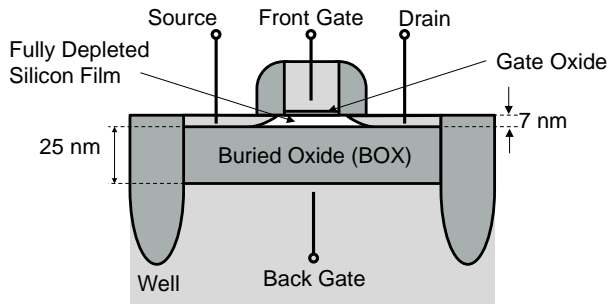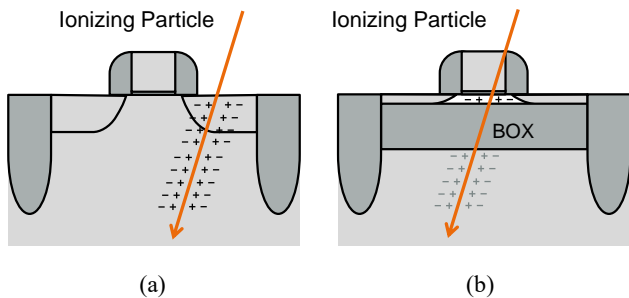t latch-up immunity [16, 17]. Figure 6(a) depicts how the charge generated due to an incident ionizing particle is collected into the drain region of a transistor in a bulk process. Figure 6(b) illustrates how the BOX layer is responsible for limiting this effect in an FD-SOI transistor. The FD-SOI devices are reportedly more susceptible to TID effects due to charge trapping in the BOX. However, the ability of these devices to withstand TID up to 1 Mrad has also been reported [18].

IV. AMBER1 IC

An IC named AMBER1 was developed in the 28 nm FD-SOI CMOS process and was taped-out in November 2015. RF blocks (Voltage Controlled Oscillator, Mixer, Low Noise Amplifier) and analog/mixed-signal test structures, realized at Fraunhofer EMFT, IIS, and EAS institutes, were integrated in it [4]. AMBER1 is developed to demonstrate the low-power features offered by this technology, and to design and validate some of the essential circuit blocks of the temperature transducer ASIC. As shown in Figure 7, the physical dimensions of AMBER1 are 1800 µm x 1800 µm. In total this IC contains 92 pads for the supplies and the signals. The analog and mixed-signal blocks are powered by 1.0 V nominal supply. However, for the digital input/output signals a supply voltage between 1.5 V and 1.8 V is required for the I/O ring.

A 1st order sigma-delta modulator and its constituent operational transconductance amplifier (OTA) were integrated on AMBER1. The sigma-delta modulator is fully-differential, switched-capacitor based circuit that features 1-bit quantization and operates with a bandwidth of 500 Hz at a sampling frequency of 200 kHz. The building blocks of the modulator include a fully differential single stage current-mirror OTA, a dynamic comparator, and a non-overlapping clock generator. Correlated double sampling technique was employed to reduce low-frequency noise and offset-compensation at the input-stage of the OTA.
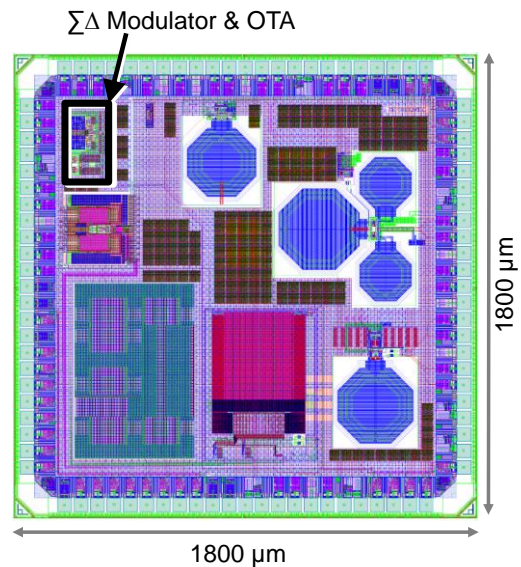

Figure 5: FD-SOI transistor cross-section

Figure 6: Effect of an incident ionizing particle on (a) bulk transistor (b) FD-SOI transistor

Figure 7: Layout of the AMBER1 IC

V. CONCLUSION

In this paper, we discussed the system-level requirements of a low-power digital temperature transducer ASIC targeted for incorporation in a sensor bus system of a future spacecraft. Temperature measurements, with a resolution of 0.1 °C, in the extended range of -40 °C to +125 °C is targeted. Accuracy requirements of ± 1 °C in the -20 °C to +20 °C range and ± 3 °C for the remaining temperatures are specified. The block level description of the ASIC and the strategies considered to mitigate the effects of radiation were also presented. The implementation of this ASIC is being carried out in the 28 nm FD-SOI CMOS process of STMicroelectronics. We discussed various features of this technology, pertaining to low power and radiation hardness. An IC named AMBER1, was realized with the goal to design and validate the crucial circuits of the final transducer system. A 1st order sigma-delta modulator and an OTA were integrated on AMBER1. It was taped-out in November 2015. Its silicon validation is planned for June 2016.

VI. ACKNOWLEDGEMENT

VII. REFERENCES

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