MEDA Wind Sensor Front End ASIC

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Abstract

This paper describes a rad-hard, mixed-signal ASIC designed in a standard 0.35 μm CMOS technology. It has been designed using Radiation Hardening By Design (RHBD) techniques aimed to reduce Single Events Effects (SEE) and to mitigate the effects of ionizing radiation. The ASIC function is that of an analogue front-end for a wind sensor that will become part of the Mars Environmental Dynamics Analyzer (MEDA) instruments set, for NASA's Mars2020 mission. The ASIC functionality, circuit approaches, and the RHBD techniques used in the analogue and digital sections are described briefly, and present test results are reported.

I. The MEDA Wind Sensor Concept

The MEDA instruments set [1] is being developed by a consortium led by Centro de Astrobiología (CAB) [2]. The wind sensor in particular is based on a concept developed at the Polytechnic University of Catalonia (UPC) [3],[4]. Essentially, a set of four heated silicon dies, which are spatially placed in a convenient configuration, are kept at a constant temperature over the environmental atmosphere temperature. The heat power required by each of the dies to maintain its temperature is measured, and from there, the wind speed in a direction related to the space distribution of the four dies, is computed.

Each of the four silicon dies includes two platinum resistors. One, R_x, biased with a constant current, is used to monitor the die temperature, while the other, R_{heat}, is used to heat up the die when required. An additional, unheated, identical, fifth silicon die (the cold die) is used to monitor the ambient temperature. Expected values of R_x and R_{heat} (at 0ºC) are in the range of 7.2KΩ and 80Ω respectively.

With a known R_x value at a reference temperature, a known constant current, and the well known, precise, platinum resistivity variation with temperature, there is a precise and stable correspondence between the voltage at R_x and temperature. In what follows, temperature measurements will be implicitly understood as voltage measurements.

Three of these wind speed sensors are used to obtain a complete three-dimensional wind speed vector measurement. This includes some level of redundancy to cope with some crossed effects, as well as with the wind disturbances produced by booms and other solid elements located within the rover vehicle in the vicinity of the sensors.

II. The MEDA Wind Sensor Front End ASIC

From the previous description, measuring the wind-speed vector requires monitoring the temperature of 15 silicon dies (3 x (4 +1)), and heating 12 of them, as needed, depending on their measured temperatures, so as to maintain their temperatures constant. The heating power (average current) delivered to each of the 12 hot dies must also be measured.

Temperature measurements are based on current-biased platinum resistors. The biasing currents must also be provided by the ASIC. The temperature of the 12 hot dies must be monitored continuously, within feedback loops, so as to maintain their temperatures constant. The measurements of the temperatures of the 3 cold-dies may be time multiplexed.

In fact, the hot dies temperature just need to be compared to a reference goal-temperature, in order to act on the heating current, in feedback loops. The actual values of the hot dies temperatures are not required. Therefore, simple voltage comparators (as opposed to analogue-to-digital converters) can perform that function.

On the other hand, the ambient atmosphere temperature, meaning the temperatures of the cold (unheated) dies, is actually needed, with their real values, because this information is required to establish the correspondence between the power delivered to the hot dies to maintain their temperature constant, and the wind speed. This means that precise voltage values must be measured. For signal integrity reasons, ease of communication, etc, ADC conversions are convenient and are done within the ASIC, close to the hot and cold dies. The ADC is then used to measure other magnitudes in the ASIC, like its own internal temperature (from a PTAT circuit), the power supply voltage, some internally-generated calibration levels for the ADC, etc, as well as other external magnitudes, essentially temperatures, used for instrument house-keeping functions.

Implicitly, it is clear that temperature stability of the ASIC is very important for precise measurements. In particular, concerning the bias currents and the voltage reference of the ADC. The ambient temperature operation range is quite large, as usual in space applications: -128 to 50 ºC. The operating die temperatures range will certainly be above those limits, due to self-heating. Precise analysis is still underway, depending on the final package thermal properties and the final heat flow from the package to the PCB and to the low density Mars atmosphere. The power dissipated within the

ASIC has significant variations as well, depending on the programmed values for the heating current sources.

In summary, the ASIC must contain an ADC, with a multiplexer for measuring several internal and external voltages, must provide current biasing for external platinum resistors, and must include 12 thermal control loops (each comprising current biasing, voltage comparison, and conditional heating currents). Three voltage-output DACs, one per wind sensor, are also included in order to set the reference goal-temperatures of the four hot dies. Here, again, the correspondence between voltage and temperature is based on the platinum resistivity variation with temperature, a known resistance value at a reference temperature, and a constant-current bias.

Finally, the ASIC contains a digital finite state machine (FSM) for functions control and data communications with the external instrument control unit (ICU).

The ASIC specification and design-process quality control have been done by CRISA [5]. CRISA has also been in charge of the high-level digital code of the control and communications FSM. IMSE-CNM-CSIC has been responsible for the design of the ASIC, including its analogue architecture and blocks, and the synthesis and back-end of the digital part.

The ASIC has been developed in a standard 0.35μm CMOS technology from AMS [6]. This technology, which is specially well suited for medium frequency, medium complexity, analogue and mixed-signal designs, allows the use of 3.3V and 5.0V transistors, among other several options. Only 3.3V transistors are used along the chip, simplifying the design and avoiding the larger ionizing radiation effects on thick gate-oxide transistors.

Along the past years, the authors have done previous efforts in the characterization of radiation and low-temperature effects on devices in this technology, in the development and validation of a rad-hard library of digital cells, and have developed several other mixed-signal space ASICs. [7],[11].

Figure 1: at the end of the paper shows a layout of the MEDA WS FE ASIC.

III. Functionality

Figure 2:, also at the end of the paper, contains a symbolic block diagram of the ASIC. There are three major functional blocks:

- Digital Control Block
- AD Conversion Channel
- Thermal Control Loops

and a number of auxiliary circuit blocks:

- RS-422 Transmitter and Receivers
- Power-On Reset (POR)
- Voltage and Current References Block
- Band-Gap
- Input-Signals Multiplexer
- Signal Conditioning Block
- ASIC Temperature Indicator
- VDD level indicator
- ASIC Temperature Alarm
- Wind-Sensors Temperature Alarm
- Signals Observation Multiplexers

Figure 2: shows the external connections of the ASIC as well, using dashed lines. There are three major pin sets:

- ICU connections
- External sensors (channels) connections
- External hot dies connections (including power sinks)

In addition, we have a number of power domains:

- VDD and GND connections

and a number of auxiliary/miscellaneous connections

- External biasing resistor (Iref) and Vref connections
- External reset and Power-On-Reset observation
- Scan Path
- Global observation nodes, analog and digital

The following paragraphs describe the circuit blocks and their functionality, and the external connections of the ASIC.

IV. External Interface

From an upper system perspective, the MEDA-WS-FE ASIC communicates with the so called Instrument Control Unit (ICU). The communication is performed through a serial, bidirectional, asynchronous link (UART) that uses an RS-422 differential physical interface. This interface serves both for control (commands) and data transmission purposes. Four pins are used for the differential, bidirectional data transmissions. A master 2.4MHz clock, used to govern the digital control block, is sent by the ICU to the MEDA-WS-FE ASIC using the same RS-422 physical layer. Two more pins are used for this purpose. The ICU connections require therefore a total of **6 pins**.

The ADC conversion channel is used to digitalize external and internal signals. Nine differential input ports are available on the ASIC, making a total of **18 pins**.

Concerning the 12 thermal control loops, for the 12 hot dies, each of them requires a pin for the current biasing of R_x, the platinum resistor used for temperature monitoring. This same pin (its voltage) is used as input to the comparators in the temperature-control feedback loops. Each die requires an additional pin for its heating current. The heating current, which can be quite large (up to 30mA for each die), is partially switched on and off from the heating resistor of each hot die during the operation of the feedback loop. The ASIC specs require the total current consumption of the ASIC to be constant, in order to avoid excessive ripples in the power supply. For this reason, the heating currents are maintained invariant in time, and (partially) switched to alternative, "power-sink" external resistors. One power-sink external resistor is used for each hot die, requiring a total of 12 pins. The power-sink resistors need to be external, as opposed to being built within the ASIC, because of the limits to the maximum power dissipation within the ASIC, imposed by the maximum junction temperature of the ASIC. In summary, each thermal control loop requires three pins, making a total of **36 pins**.

Some alternatives aimed to reduce the number of pins dedicated to power sinking were considered but discarded. One of them was the use of just one external sinking resistor for the 12 loops. This was discarded because the large range of the total current to be sunk, together with the voltage limits imposed by the technology, forced the use of a low resistor value, which in turn resulted in excessive power dissipation within the ASIC under some circumstances. The alternative of using a nonlinear external resistive load (e.g. several series connected diodes) was also discarded due to expected difficulties in finding the proper space-qualified components.

A total of **29 pins** are dedicated to power and ground connections. Six different power domains are used, in an attempt to prevent power and substrate noise generated by noisy environments (digital sections, heating currents, etc) from reaching sensitive nodes (ADC section, and thermal loops comparators). Because of the large heating current sources, which drive external resistors connected to ground, more VDD pads are used than GND pads.

Some additional pins are used for miscellaneous purposes. One pin is used to monitor the global reference voltage V_{REF}, generated internally, from which all other internal voltage levels are derived. Measuring its value for each individual ASIC sample, as well as its variation with temperature, allows a much higher accuracy in the final, calibrated system. An external capacitor can also be connected at this pin in order to reduce the noise bandwidth of the reference voltage. Another pin is used to generate a precise reference current using an external resistor with very low temperature coefficient. The current is derived from the internal reference voltage and the external resistor, using a continuous-time feedback loop. One more pin is used for FSM reset-related functions. It allows the observation of the internally generated reset pulse from the power-on-reset block, as well as forcing an external reset if needed. Four pins are dedicated to a scan-path testability function that was added for the digital control block, and another four pins are dedicated to the observation of many internal analog and digital signals, which can be multiplexed to these four nodes. This makes a total of **11 pins** for miscellaneous purposes.

The ASIC has a **total of 100 pins**. The package used for initial measurements and characterization is a CQFP-100. The final package to be used in the flying modules will also be a CQFP-100 but from a different manufacturer, due to qualification concerns.

V. Signal Conditioning and ADC

The signal conditioning and analogue-to-digital channel is designed to measure external and internal voltages. The principal external voltages to be measured are representative of temperatures, i.e., they are voltage drops generated across external platinum resistors, which must be current-biased. The input to the conversion channel is differential. The ASIC must provide the biasing current, and the voltage at the other end of the resistor. A secondary type of signal to be measured is the voltage across thermopiles. In this second case, some signal amplification is required. The internal signals to be measured include the three DACs outputs (which represent the target hot-dies operating temperatures), one signal representing the ASIC internal temperature, a down-scaled version of the power supply voltage, and six internal reference signals used for conversion channel calibration.

A. The input channels multiplexer

A multiplexer, built using CMOS switches, is used to convey one of the 9 external channels, or one of the 11 internal signals, to the preamplifier input. The on-resistance of the switches does not affect the measured voltages, thanks to the capacitive input impedance of the preamplifier at the input of the ADC. A four wires interface is used for the resistors to be measured, again avoiding the effect of the on-resistance of the switches connecting the bias current and the DC voltage at the other end of the resistor. The complete multiplexer for the differential signals with the four wires interface can be understood as a set of four multiplexers under the same control word. The multiplexer, and the whole conversion process, is controlled by the digital control block.

B. The bias current for the ADC Channel

As mentioned above, the ASIC provides a bias current for measuring resistor values by measuring their voltage under a known current value. Since there is only one conversion channel, the 20 signals (9 external, 11 internal) are converted sequentially, multiplexed in time. This allows the use of one single, programmable current source for all channels. The current source uses a cascode topology for improved output impedance, and can be programmed with four bits from 0 to 750μA in steps of 50μA. The bias current can take different values (including zero) for each of the signals, under the control of the digital control block.

In a similar form, the connection at the other node of the resistor, this is, at the negative node of the differential input signal, can be connected to different reference voltages for each of the channels, also under the control of the digital control block.

C. The ADC channel

Figure 3: shows a simplified block diagram of the conversion channel. It is composed of a preamplifier with two stages, and a dual-slope ADC. The dual-slope ADC is composed in turn of an analogue integrator, a comparator, a finite state machine (the ADC-FSM) for the control of the AD conversion process, and an oscillator used to generate a higher frequency clock for this ADC-FSM.

The ADC is designed to have 16bits (15 + sign) resolution, with conversion times below 1ms. Integral non-linearity and r.m.s. noise have been taken into account in the design, keeping them within the range of a few least significant bits equivalent voltage (V_{LSB}).

1) Preamplifier

A conventional instrumentation amplifier, with a differential architecture, is used at the input of the ADC channel. It provides capacitive input impedance, important to avoid the effect of the on-resistance of the switches in the signal multiplexer. The gain of the amplifier is 1 in general, for all signals to be measured, but can be optionally set to 150

for some external signals, when external thermopile voltages are to be measured. Special care has been taken in minimizing the amplifier offset so as to avoid saturation, in particular with the high gain configuration. Fully differential dual-slope converters often suffer from a zero-crossing discontinuity (or sign-dependent offset). This is not a problem for input signals given by voltage drops at current-biased resistors, or other signals whose polarity is well known a priori. However, this is not the case for thermopile voltages. For that reason, a level-shifting equal to 1/4 the differential input signal range can be optionally added to the input signal, mapping the central 1/2 of the bipolar input range into one side of the amplifier output range. This is done in the second stage of the amplifier, after the signal has been amplified, for accuracy reasons.

2) ADC-FSM

Dual-slope converters perform two time integration processes. The first one begins with a reset integrator (zero initial value) and integrates the input signal, while the second starts with the accumulated result of the first, and integrates the reference signal with sign opposite to the input signal.

The time required, during the second integration period, for the integrator output to cross zero is proportional to the ratio of the input signal to the reference signal. This time is measured using a digital counter, driven by a digital clock. The counter is set to zero at the beginning of the second integration period and stops (or its content is sampled in an auxiliary register) at the zero crossing of the integrator output. The zero-crossing is detected by a comparator, often a clocked, fast, regenerative comparator. The comparator is first used, at the beginning of the second integration, to select the proper polarity of the reference signal.

The ADC-FSM controls the sequence of operations and signal switching required to perform whole process, the clocked comparator, and the digital counter. The clock of this FSM must have a high frequency, because the conversion time is at least 2^N clock cycles, with N being the number of (magnitude) bits, 15 in our case. For that reason, the external 2.4MHz clock was not appropriate, and a higher clock had to be generated on chip.

3) Oscillator

A 50MHz (nominally) oscillator has been included in the ASIC, in order to drive the ADC-FSM. It is a relaxation type, with an RC time constant defined by the same components used in the integrator (same resistor and capacitor options among those available in the CMOS process). This ensures that, even under severe process and temperature variations, the integrator output will not saturate, because the integration time, measured in clock periods, and the integrator time constant become proportional. The oscillator frequency, or its stability with process and temperature, has no effect on the conversion process. Extreme frequency variations are in the range of ±25%, and have to be accounted only for worst-case conversion time. Clock jitter is not a dominant source of noise in this type of converters.

4) Analogue integrator

The analogue loss-less integrator is based on a typical, capacitive fed-back operational amplifier. It is fully differential, with the same common mode level than the preamplifier output. Some switches are required for integrator reset, and to connect the input of the integrator to the input signal or to the reference signal with one or the other sign. Special concerns in the design of the operational amplifier were offset and noise. The integrating capacitance, at each rail, is 90pF. During the first (signal) integration period, which lasts 2^{12} clock cycles, the input resistor is 1MΩ. During the second (reference) integration, which lasts a maximum of 2^{15} clock cycles, the resistor is 8MΩ.

5) Comparator

The comparator operates with the high-frequency ADC clock, in two phases. It is composed of a high-gain, open loop differential preamplifier, followed by a clocked sampling/regenerative stage, in turn followed by a latch. Note that hysteresis, which could be expected from the use of a high-gain preamplifier as a first stage, is not a big concern because the input to the comparator is always a well-behaved, slow ramp. Note also that the preamplifier offset, as well as the delay time of the comparator, with its low input signal at the zero crossing point, represents only an additional contribution to the ADC transfer characteristic offset. The output of the comparator is always well defined from a digital perspective, and well synchronized with the ADC clock.

6) Reference signal

A global reference signal (V_{REF}) of 2.5V is obtained by scaling up the voltage from a band-gap circuit. All other voltage references needed within the ASIC are derived from V_{REF} using a resistive string. In particular, the reference voltage (differential) for the ADC is ±2.0V around a common mode level of 1.5V.

Note that, because the reference signal is differential, the zero reference is error free. Also, the magnitude of the reference voltage for positive and negative inputs is the same, since the same two levels are used with one or the other polarity. The gain of the ADC transfer characteristic is affected by the magnitude of the reference voltage, as well as by several other sources within the ADC circuitry.

D. ADC channel calibration

The chosen type of ADC, a dual slope, is well known to be very linear, and have very good noise figures. On the other hand, the gain and offset errors of the static transfer characteristic can have relatively high values, and may result in measurement errors in the range of many V_{LSB}.

Offset and gain values will be different from ASIC sample to ASIC sample, but they may be measured, for the specific ASIC samples used in the final instruments, and their deviations can then be compensated through calculations. This is not a problem in the context of space applications. In particular, when the final objective is to measure some magnitudes and send the information to Earth, the corrections may be done on Earth, using the ASIC characterization data obtained at the time of building the instruments. However, offset and gain values may change in time due to their dependence with temperature, power supply level, aging, and other causes. For this reason, several fixed input voltages,

derived from the global reference V_{REF}, are included in the ASIC within the set of internal signals that are multiplexed to the ADC input. A careful measurement, on Earth, of the precise ratio of these reference voltage levels to V_{REF}, and assuming that this ratios will not change in time (they are given by ratios of resistors built using the same material, with the same current density, in the same environment, etc), the offset and gain errors of the ADC can be calibrated using correction parameters obtained in real time.

VI. The Thermal Control Loops

The function of the 12 thermal control loops is to maintain 12 external "hot dies" at a constant, prescribed temperature above the ambient temperature, and to measure the amount of heating current required by each external die for that purpose.

The 12 control loops are grouped into three sets of four control loops. The prescribed temperature for the four dies in each group is the same, but can be different from group to group. A digital to analogue converter (DAC) is used to set the reference temperature (equivalent voltage) for each group.

For each loop, the ASIC generates a bias current I_x, of nominal value 100μA, which is used to bias a grounded resistor R_x in the external hot die. The voltage (V_x) at the current output bonding pad (voltage at R_x) is compared to the DAC output. A constant heating current (I_{base}) is permanently applied to the heating resistor (R_{heat}) in the die, and an additional current (I_{delta}) is conditionally applied if the die temperature is found to be below the prescribed temperature. The feedback loop operates in discrete time, under the control of a low frequency clock generated in the digital control block by division of the master 2.4MHz clock. The low frequency can be chosen between 8.2 and 16.4 KHz. The controlling FSM counts the number of times the additional current was applied to each die. A common (to all loops) master counter of 14 bits controls every measuring period. Individual 14 bits counters are used for each loop to store their corresponding data. The overall measuring frequency is 0.5, 1.0, or 2 Hz depending on the selection of clock frequency. For the 2Hz mode, the maximum resolution is 13 bits, instead of 14.

A. *The bias current sources*

The 12 I_x bias current sources have a nominal value of 100μA, but can be individually programmed with 8 bits resolution between 94 and 106μA. This allows a precise compensation of resistors R_x variation (mismatch) from hot-die to hot-die. The current sources are calibrated to produce the same voltage drop in their corresponding resistors, at some reference temperature. This ensures that the four hot-dies in each group are actually kept at the same temperature.

The 94μA current source and the 0 to 12μA current-output DAC are implemented using conventional topologies. Again, cascode transistors are employed for high output impedance. The cascode transistors are also used as switches in this case.

All current values are derived from the reference current I_{REF} (see below) using current mirrors. High area transistors and careful layout techniques are used to minimize the effects of mismatch.

B. *The comparator*

A voltage comparator in each loops determines if the hot-die temperature is above or below the temperature prescribed for its group. It compares the voltage V_x at resistor R_x with the DAC output corresponding to the group. The result of the comparison is sent to the digital control unit which, if the temperature is lower than prescribed, enables the additional I_{delta} heating current and increases the digital counter used to measure the additional power delivered to that hot-die. This is repeated at the pace of the low frequency clock, under the control of the digital control block.

This comparator is a clocked, switched-capacitor comparator, with auto-zero. It is followed by a latch and a flip-flop, ensuring that the digital signal reflecting the result of the comparison is well defined during the whole clock cycle, with a relatively small delay (as compared to the slow clock cycle) after the hot-die temperature sampling instant. The control signals required by the switches in the comparator are generated by the digital control block.

C. *The heating current sources*

Heating current sources, I_{base} and I_{delta}, have some particular design concerns, because their maximum values are quite high. Each of them can be programmed, with common values for each group of four loops, from 0 to 15mA, with four bits resolution. This programmability is introduced because of the wide range of environmental conditions expected, which requires wide ranges of permanent and switchable heating powers. If all I_{base} and I_{delta} were set to their maximum values, the total current would be 360mA.

Special care has been taken in the power supply routing, using very wide metal lines, over the transistors area. Simulations of the distributed resistance effect have been carried out to ensure that the voltage drops in the power supply do not affect the current sources accuracy. Again, the current values are derived from the reference current I_{REF} using current mirrors. High area transistors and careful layout techniques are used to minimize the effects of mismatch.

As explained earlier, in order to maintain the ASIC supply current constant, the I_{delta} sources are actually not switched on and off, but redirected towards the heating resistor in the corresponding hot die (being added to I_{base} through the same bonding pad) or towards a sink resistor (through an alternative pad). Complementary switches are used for this purpose. The controlling signals of the complementary switches are overlapped in the on state, to avoid current glitches in the supply.

D. *The DACs*

Three voltage-output DACs, one per group of four loops, are used to set the prescribed temperatures for the hot dies in each group. Their resolution is of 10 bits.

The DACs use a conventional resistive divider and analogue multiplexer topology. The transfer characteristics are monotonic by construction. The reference voltage is obtained from V_{REF}, using a buffer to avoid kick-back transients on the global reference. Taking advantage of the (switched) capacitive input of the comparators, no buffer is

used at the analogue multiplexer output, avoiding offset effects. One single voltage buffer (with one offset value) drives the three resistive strings, which are shorted together every 32 unitary resistors, making the transfer characteristics of the three DACs essentially identical.

VII. The Communication and Control Unit

The digital control block, also called the communication and control FSM, performs the following functions:

- Receives and sends commands and data from the external interface with the instrument control unit (ICU). This is done through an Universal Asynchronous Receiver/Transmitter (UART) at a speed of 19600 bauds.
- Reads and writes configuration and data registers located in different parts of the chip. This includes configuring some programmable analogue circuit blocks, and reading the ADC channel output data.
- Controls the operation of the thermal control loops, its comparators, its heating current sources, and counts the additional heating current delivered to each hot die. It performs these operations according to various operating modes.
- Controls the AD conversion channel, and the sequence of conversion of the 20 channels that are time-multiplexed, according to various operating modes.
- Receives the alert signals from the over-temperature sensors corresponding to the hot-dies and the ASIC itself, and takes the corresponding actions when required.

The operating modes include a *cyclic mode* and an *on-request mode*, meaning that the ADC channel conversions and power measurements from the thermal control loops can take place periodically, or on-request. There are some auxiliary modes, like a test mode specifically devised to help in the characterization of the ADC, and others. The digital control block also interprets and executes the commands, enables and disables different circuit blocks in the ASIC, and receives parity checks from the many registers in the ASIC, reporting to the external ICU in case of errors. This digital block includes a scan-path port for testability purposes. The high-level design has been carried out by CRISA [5].

VIII. Auxiliary Blocks

A. The Band Gap and Voltage Reference

As mentioned earlier, all voltage references in the ASIC are derived from the global voltage reference V_{REF}, using one single resistive string taped at different points.

The global reference V_{REF}, nominally 2.5V, is obtained from a band-gap circuit, whose output is amplified using a feedback amplifier. The gain is defined by a resistor ratio. The global voltage reference is connected to a specific pad, and can be trimmed using four bits from an internal register, in order to cope with the opamp offset and resistor mismatch. Four additional bits can be used to trim the band-gap, in order to reduce the reference voltage variations with temperature.

B. The PTAT

A proportional-to-absolute-temperature (PTAT) current is generated from the band-gap. The voltage generated in a resistor is then used to measure the temperature of the ASIC die. This is one of the signals that is converted by the ADC channel, providing a real-time measurement of the ASIC temperature. This is important for two reasons. One is the possibility of compensating minor effects of temperature on the measurements for which the ASIC has been designed, provided that a previous calibration has been done. The other is to provide a safe-ward against excessive heating of the ASIC, something important due to the large heating currents and the low density atmosphere in Mars.

C. The Current Reference

A current reference circuit is used to obtain a stable current value I_{REF}. It is based on a voltage derived from V_{REF}, and an external resistor connected at a specific bonding pad. A feedback loop controls a current source that drives the resistor, until the resistor voltage is equal to the derived voltage (1.0V). The external resistor should have a temperature coefficient as low as possible. Values of 25 ppm/ºC are expected in the final flying modules. For the characterization of the ASIC, external resistors with 0.1ppm/ºC are being used.

Note that, neglecting the variation of the external resistor with temperature, it turns out that the reference current will change with temperature, and with ASIC sample, in the same way than the reference voltage V_{REF}. The offset of the amplifier in the feedback loop, which has been specifically optimized, has some effect but is negligible as compared to V_{REF} inter-samples variations. This V_{REF}-I_{REF} deviations correlation has relevant implications in measuring resistance values by means of measuring the voltage on a current biased resistor: because the reference voltage of the ADC and the biasing current (and therefore the resistor voltage) change in the same way, there is no effect on the resulting measurement.

Still, voltage and current stability with temperature are primary goals, because they do have an effect on other measurements, specially in the delivered current to the hot dies -with a squared effect on power-, as well as other voltage magnitudes not related to resistor measurements.

D. High-Temp Alarms & Auto Shut Down.

The ASIC contains some over-temperature protective functions, for it-self and for the hot-dies. The hot dies temperatures can be observed from their voltages V_x. These are compared to a reference, maximum voltage, representative of their maximum allowed temperature. Simple continuous-time, inaccurate comparators are used for this purpose, since accuracy is not too relevant in this function. The output of the four comparators associated to the four dies in each group is "ORed", and the result for each group is sent to the digital control block. If any die is over heated, the heating currents (I_{base} and I_{delta}) of that group are disabled. The internal temperature of the ASIC, taken from the output of the PTAT circuit, is also compared to a (different) voltage that

represents the maximum allowed temperature for the ASIC die, and sent to the digital control block. All heating currents are disabled in the event of an ASIC over-temperature.

E. Power-on Reset

A power-on-reset circuit is included to generate a reset event shortly after the power up. A specific pin performs the double function of allowing an external reset, and the evaluation of the internal power-up reset pulse. The ASIC can also be reset by software, using a reset command.

F. Measurement of the Power Supply Voltage

A resistive divider is used to down-scale the power supply voltage, placing it within the conversion channel input range. This is level is also multiplexed to the ADC channel, providing a real-time measurement of the power supply voltage. The purpose is to detect eventual improper power supply levels, and to allow the eventual calibration of power supply variations effects on the measurement function.

G. RS-422 Receivers and Transmitter

As mentioned earlier, RS-422 differential signals are used in the communications between the ASIC and the ICU. The ASIC receives two signals from the ICU: a 2.4MHz clock, and the incoming R_x data, at 19600 bauds. The ASIC in turn sends the outgoing T_x data to the ICU, at the same baud-rate. The receiver circuit is the same for R_x and clock, despite the different frequencies, for simplicity. Conventional circuit approaches are used for this function. The transmitter is designed to operate with self-limited slew rate, in order to reduce electromagnetic emissions from the transmission lines connecting the ASIC and the ICU.

H. Reference levels for ADC calibration

Six differential voltage signals with the proper common mode, which represent the 10, 50, and 90 percent levels of the (one side, positive or negative) input signal range of the ADC channel, for the gain 1 and the gain 150 configurations, are obtained from V_{REF} using a resistive divider. The same reference signals are used for both sides (positive and negative) of the input signal range by swapping the connections to the preamplifier input.

These signals can be observed and measured through the global nodes used for testing and observation of a large number of analogue and digital signals. This is important for precise calibration due to resistors mismatch, which limits the accuracy of these reference signals.

IX. RHBD and Low Temperature Measures

Concerning Radiation Hardening by Design (RHBD) measures, the design uses well known techniques, available in the literature, and builds on previous work by the authors in the characterization of radiation and low temperature effects on this specific CMOS technology [7],[8].

The analogue circuitry is full-custom, and uses enclosed-layout transistors (ELTs) for the nmos, and regular layout for pmos. Minimum length transistors are uncommon in analogue circuitry, and are avoided in general. These measures are aimed to increase the circuitry robustness against ionizing radiation. Although the specification of a maximum TID of 9Krad is quite low, and these techniques could probably be skipped, it was decided to use the procedures developed in previous RHBD mixed-signal ASICs [9],[11] to allow the eventual use of the ASIC in other environments.

Guard-rings are used around nmos and pmos devices, with the purpose of reducing the probability and the severity of single-event effects (SEEs) in the analogue circuitry. The type of converter used, the size of the capacitors employed in the sensitive signal nodes and switched-capacitor comparators, and other measures, makes it unlikely that a single particle impact could produce a single-event transient (SET) that could originate a severe degradation of the performance. Still, the role of the ASIC, being part of an atmospheric data measurement system, allows sporadic wrong behaviour without catastrophic effects. The situation is different concerning single-event latch-up (SEL). A latch-up event could potentially destroy the device, with permanent effects on the instruments. However, similar mixed-signal ASICs designed and tested using the same procedures in the same technology have been shown to be latch-up free up to at least 80 MeV·cm^2/mg. The same result is expected for this design.

The digital sections of the ASIC are semi-custom, and employ a library of RHBD digital cells developed in the past years by the authors. The RHBD techniques used in the digital cells are the same described above for the analogue circuitry. Several previous ASICs and test vehicles have shown more than sufficient TID tolerance, and latch-up free behaviour also up to at least 80 MeV·cm^2/mg. Regarding eventual single-event upsets, all registers in the ASIC include an additional bit for parity-check. Parity errors are reported to the digital control unit, which in turn reports this events to the ICU as part of an ASIC-status word.

With respect to temperature, the ASIC is specified to operate within -128 ºC to 50 ºC, ambient temperature. Concerning the electrical simulations used along the design and verification process, it must be noted that the foundry provided models are not qualified below -55ºC. The authors have measured transistors I-V characteristics down to -110ºC and verified that the transistor models can be used with reasonable accuracy down to this limit. Also, the actual temperature operation range of the die will be quite above the ambient-temperature operation range, due to self heating. This is specially true considering the low density of the Mars atmosphere, and therefore, the high temperature coefficients that can be expected from the ceramic package.

Specific radiation (TID & SEE) and low temperature tests in a "Mars Chamber", are planned for the coming months.

X. Experimental results

The ASIC has been tested from a functional perspective, at room temperature. Some specific magnitudes have also been measured in temperature down to -20ºC. Measurements further down are planned for the coming weeks. The following paragraphs describe present test results and measured performance.

A. Communication and Control functions

The ASIC is being tested using a specific test system based on a Raspberry Pi-2. The communication functions have been tested and are operative. Command executions, data transferences, and register configuration functions are also operative. In summary, the digital control block and the RS-422 receivers and transmitter are operating without problem. The transmitter output signals are slew-rate limited as required. The POR circuit is also operating within specs.

B. The ADC channel

The ADC channel has been functionally verified on a reduced number of samples. However, performance figures requiring measurements of a significant number of ASIC samples are still underway. Gain and offset values are correct. More detailed measurements are still required to separate noise from static characteristics, but preliminary results show that the Integral Non Linearity (INL) is within ±1 V_{LSB}, and r.m.s noise is also within specs, in the range of 1 V_{LSB}. The converter is inherently monotonic. Measurements show the same transfer characteristic for all 9 external channels, demonstrating that the multiplexer has no effect, as expected from the capacitive input impedance of the preamplifier. The bias current and reference voltages used to bias the external resistors have their expected values.

C. Thermal Control loops

The behaviour and stability of the thermal control loops has been verified using hot-die samples provided by UPC. In addition, the specific accuracy of the involved circuit blocks has been preliminarily evaluated, as required to asses their effects on the delivered power measurements.

The clocked comparators, with their auto-zero function, have an offset value below 0.1mV. The I_x bias currents have a dispersion below ±0.3%, and the heating currents below ±0.5%. These are measurements taken over the 12 units available in each ASIC. Concerning the DACs, which are monotonic by construction, their INL is below ±1 V_{LSB}.

D. Miscellaneous functions

The band gap, voltage reference, and current reference circuits are operating correctly. The observable nodes are the V_{REF} and I_{REF} nodes. The results are within specs. The average (over 12 ASIC samples) value of V_{REF} is 2.488V (nominally, 2.5). The standard deviation is 0.5%. Note that this includes the variations of the band-gap and those related to the amplifier, including the opamp offset. The nominal voltage at I_{REF}, where the external low-temperature-coefficient resistor is connected, is 1V. Average and standard deviation values are 0.9955V and again 0.5%. Further more, there is a very high correlation between the deviations of V_{REF} and those of the voltage at I_{REF}, meaning that resistors matching is quite good (non dominant) and that the feedback loop used to generate a current proportional to V_{REF} and inversely proportional to the external resistor is working properly. The maximum variations of V_{REF} with temperatures, between -20 and 100ºC, is below ±5mV (w.r.t. its central value). The equivalent variation at the band-gap output, assumed to be 1.2V, is 2.5mV approximately. In either case, equivalent to a ±0.2%.

The PTAT used to measure the ASIC die temperature is working properly. Accuracy figures are still to be determined, but are not too relevant since the main purpose of this function is to allow a correspondence between ASIC temperature and eventual correction/calibration factors, the precise value of temperature being somewhat irrelevant. The down-scaled version of the power supply voltage is also correct, with deviations in the range of resistors matching (~0.1%), again irrelevant. Finally, the temperature alarms (and corrective actions from the digital control unit) for the external hot-dies and ASIC die are also operative. Again, accuracy is not relevant because thresholds are usually set with enough tolerance. The analog and digital multiplexers used to observe internal signals are also operative.

XI. Summary

A rad-hard, mixed-signal ASIC in a standard 0.35 µm CMOS technology has been designed. It is an analogue front-end for the MEDA wind sensor for NASA's Mars2020 mission. The ASIC has been fabricated and tested. Some additional detailed measurements are underway. Radiation tests are planned for the coming months. They are expected to be satisfactory based on previous ASICs designed in the same technology using the same RHBD techniques and the same rad-hard digital library.

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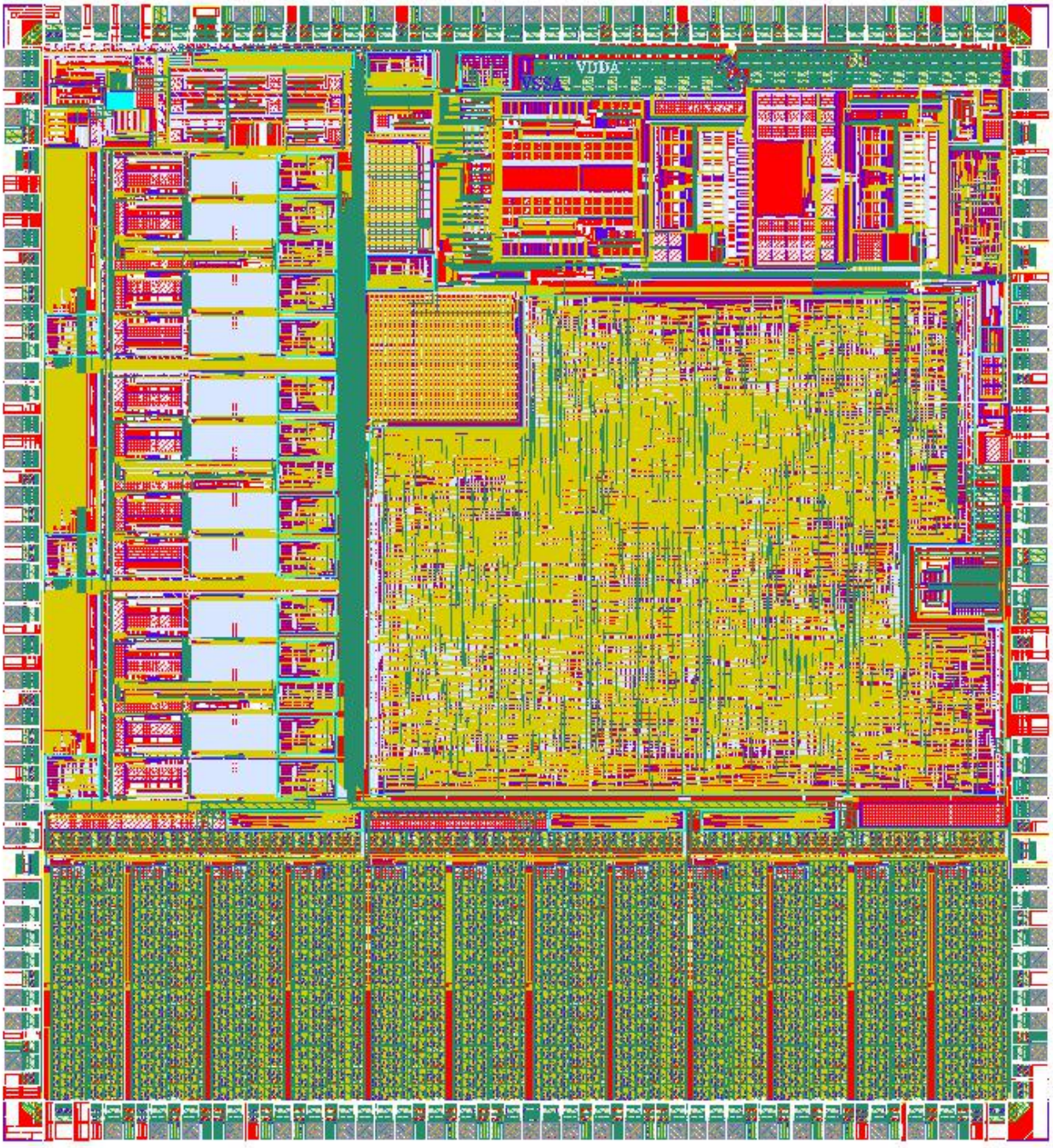

Figure 1: MEDA WS FE ASIC Layout. Dimensions are 5 x 5 mm.

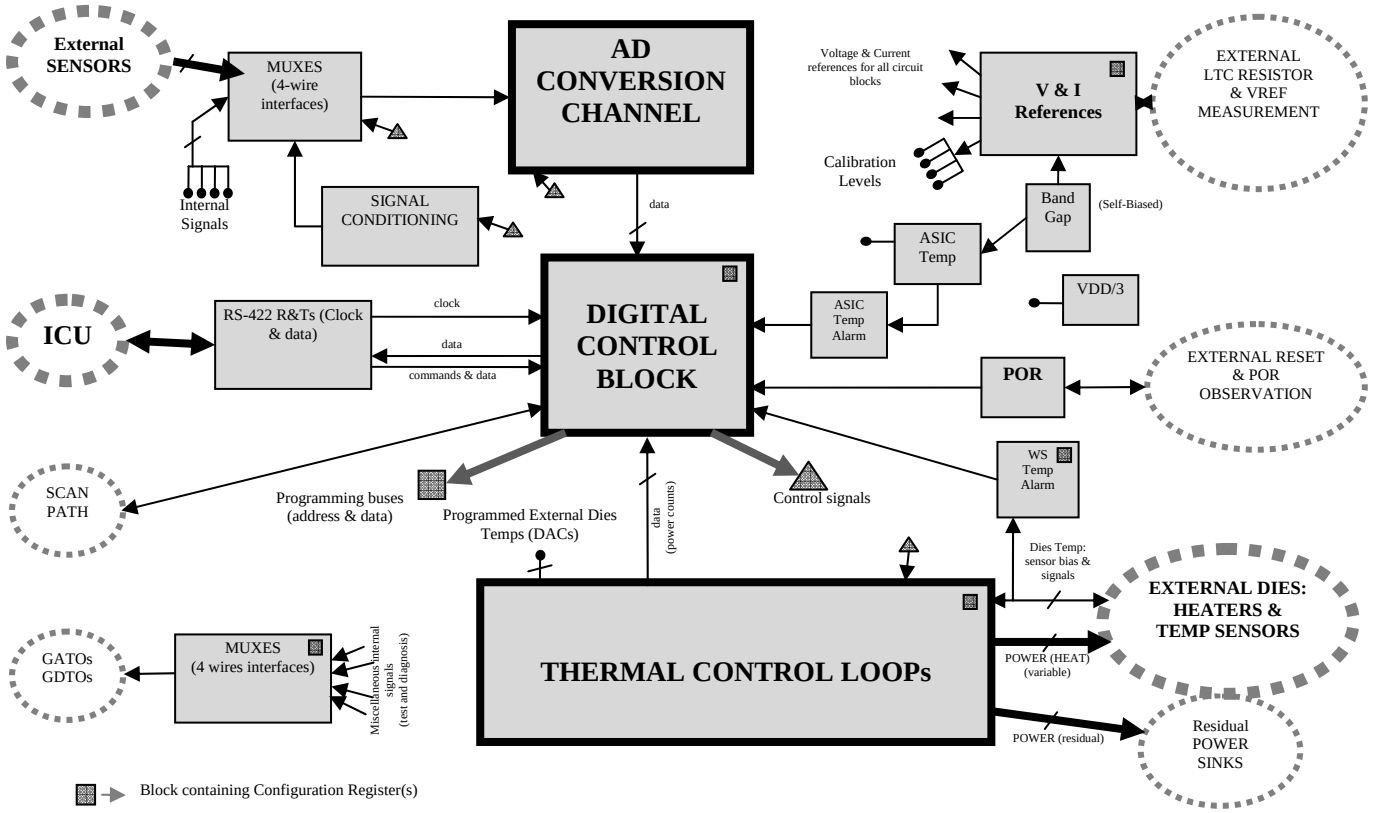

Figure 2: Simplified Block Diagram of the MEDA Wind Sensor Front-End ASIC.

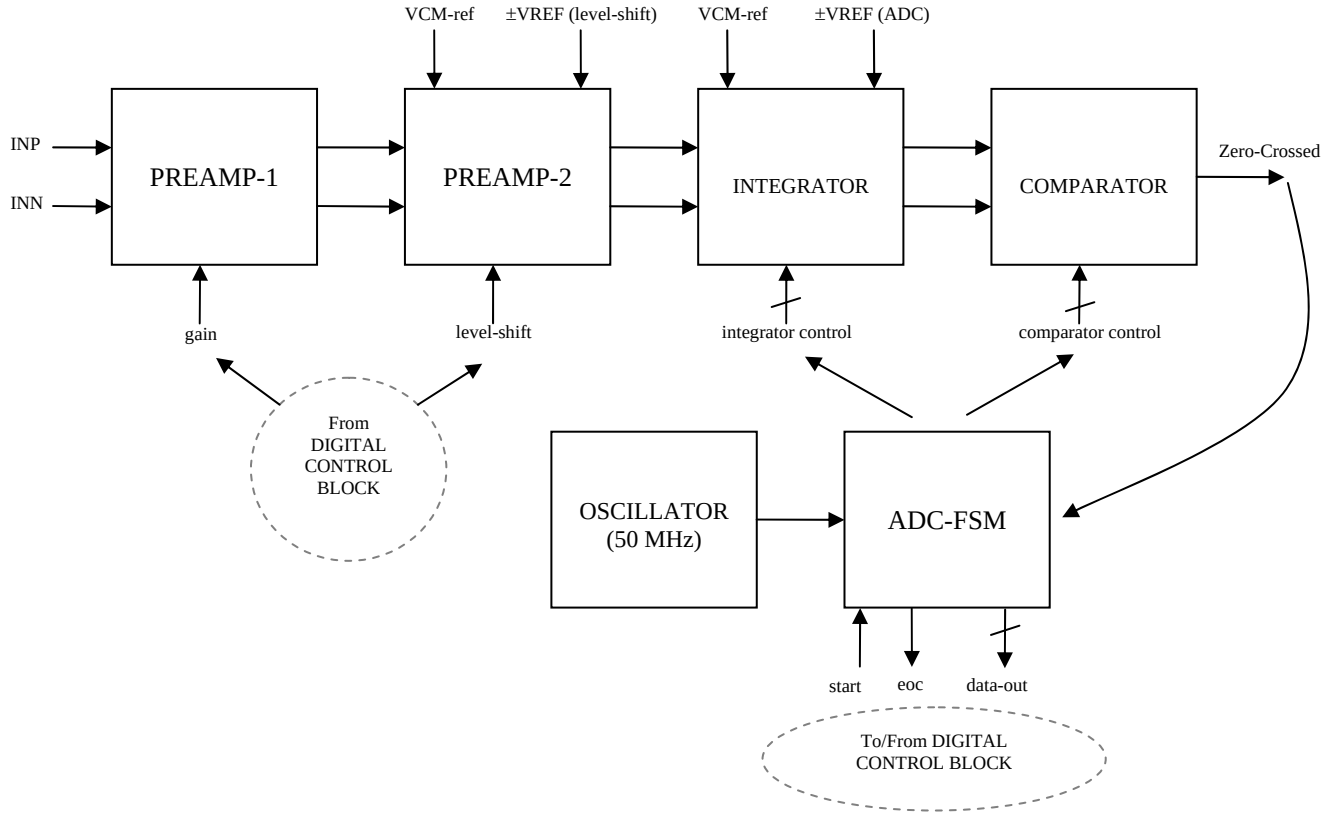

Figure 3: Block Diagram of the ADC conversion channel. Input multiplexer and bias currents are not shown.