Radiation Prediction Tool Dedicated to Analyzing and Hardening by Design Readout Circuits of Photonic ICs

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Abstract

This work presents a SEE prediction tool called MUSCA SEP3 and its interest in failure investigations and in providing a help for designers with the aim to optimize the SEE sensitivity of Sofradir readout circuit. Estimations and a failure analysis at circuit level were presented. Comparisons between predictions and experimental data obtained under heavy ion are consistent. The analysis of critical areas of the DFF design allows to propose hardening techniques with the aim to reduce the SEE sensitivity of the D Flip-Flop (D- FF) of the readout circuit.

I. INTRODUCTION

Image sensors are widely used in spacecraft for many applications [1][2]. Photonic imager technology has been developed for wavelength responses that range from ultraviolet, through visible, to infrared. Most radiation effects studies have been made on infrared detectors, and visible/near infrared technologies such as charge coupled device (CCD), charge injection devices (CID) and active pixel sensors (APS). Among many optical applications, like earth or space observation, the guidance system in a spacecraft (launcher or satellite) is particularly critical. Then, the reliability of such guidance systems based on image sensors is essential for the space mission.

CMOS (Complementary Metal Oxide Semiconductor) technology is mainly used in the readout circuit of photonic integrated circuits (ICs). However, CMOS technology is known to be sensitive to single event effects (SEE), such as single event transient (SET) [2]. SETs can be induced by various ionizing particles, i.e., heavy ions, protons, electrons the space radiation environment [3]. SETs can become critical for image devices and ICs boarded in flight because of their critical applications. Actually, SETs in D Flip-Flop can change the logic state and disturb the nominal behavior of the readout circuit.

One of the interests of prediction tools, such as MUSCA SEP3 (MUti-SCAle Single Event Phenomena Prediction Platform) [4][5], is to anticipate the sensitivity trends with the aim to help the designers to select the best layout considering of performances and reliability. Moreover, these investigations lead to reduce the number of testing runs during the qualifications of electronics under high energy particles such as heavy ions.

In this work is presented the interest of such approach to understand the failure origins at transistor level with the aim to be able to harden circuits of the readout system of photonic devices. This work presents an optimized design of the reference DFF used in the readout circuit of a infrared (IR) device, designed by Sofradir. The gain in term of SEU sensitivity is shown while the penalties in term of area and power consumption are non-existent, quite the opposite.

II. SEE PREDICTION TOOL

A. Simulation flow of the prediction tool

MUSCA SEP3 is a SEE prediction tool based on a Monte-Carlo approach which allows a complete simulation from the interaction of the radiation particles with the matter to the occurrence of the soft error in the IC [4][5] as shown in the figure 1. These simulations use nuclear databases (issued from GEANT-4 calculations) in order to describe in 3D the interactions (nuclear and Colombian) of radiation particles, such as, heavy ions, protons, neutrons, or muons, with the materials of the Back-End Of Line (BEOL). The modeling of transport and collection mechanisms is based on dynamic ambipolar diffusion, multi dynamic collection, and bipolar amplification. Details of analytical models of transport and collection mechanisms are presented in details in previous works [6][7]. The effects of bias voltage, the layout, and the fabrication processes are taken into account with the aim to build a realistic SET currents database. The modeling of the Front-End Of Line (FEOL) is based on the description (dimensions and locations) of active implants, i.e., drain and source of each n-MOS and p-MOS transistor directly extracted from GDS files. The process of the extraction of collection areas from the layout file has been presented in a previous work [8]. All required layout files and electrical models were provided by Sofradir. Next, this SET currents database is injected on each corresponding node at transistor level for an electrical simulation with Spectre simulator with the aim to estimate the soft error response of the circuit. The electrical transient simulations of the parasitic circuit were performed by the Spice simulations [9]. As previously, the schematic of the cells and the model cards of n-MOS and p-MOS transistors are provided by Sofradir.

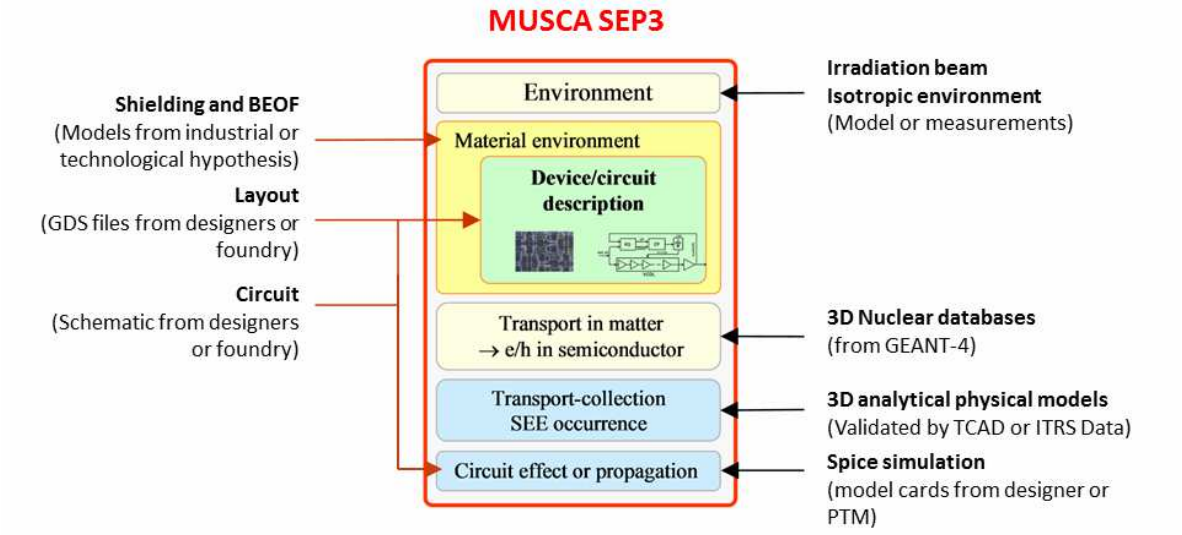
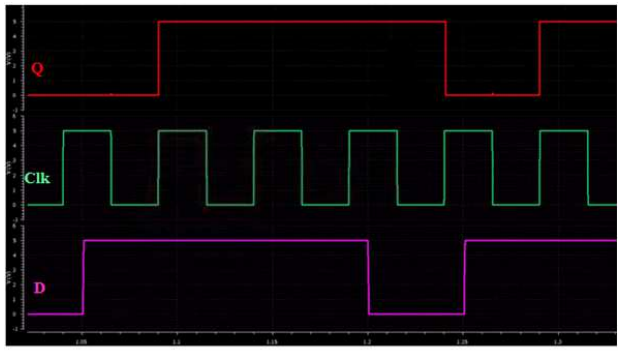
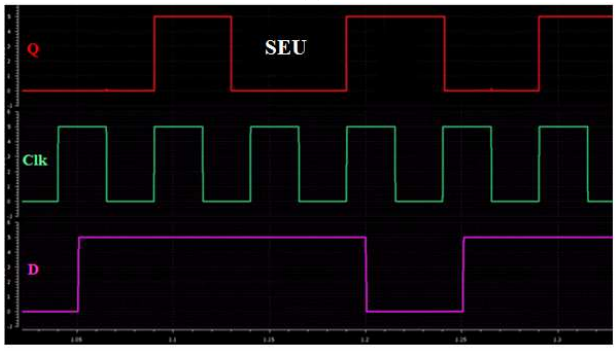


Figure 1: Simulation flow of the SEE prediction tool, MUSCA SEP3

An upset event is considered during the electrical simulation if the output signal Q changes of logic state ("1" to "0" or "0" to "1") while it should not. The chronograms of input, output and clock signals illustrate the SEU detection based on the electrical simulations, and are shown in the figure 2(a). It presents the nominal behavior of the DFF cell synchronized by the clock signal (i.e. Clk) of 20 MHz. On the other hand, the figure (b) reveals a SEU occurrence on the output signal (Q) induced by an incident heavy ion on the DFF cell. The output signal decreases from 5V (state "1") down to 0V (state "0") until the next rising edge of the clock signal.



(a)



(b)

Figure 2: Chronograms of input, D (in pink), output Q (in red), and clock Clk (in green) signal of the DFF in (a) nominal behavior and (b) impacted by a SEU.

Based on this simulation framework, MUSCA SEP3 is able to propose an estimation of the SEU sensitivity (SEU cross section, but also event mapping) of the DFF cells designed by Sofradir.

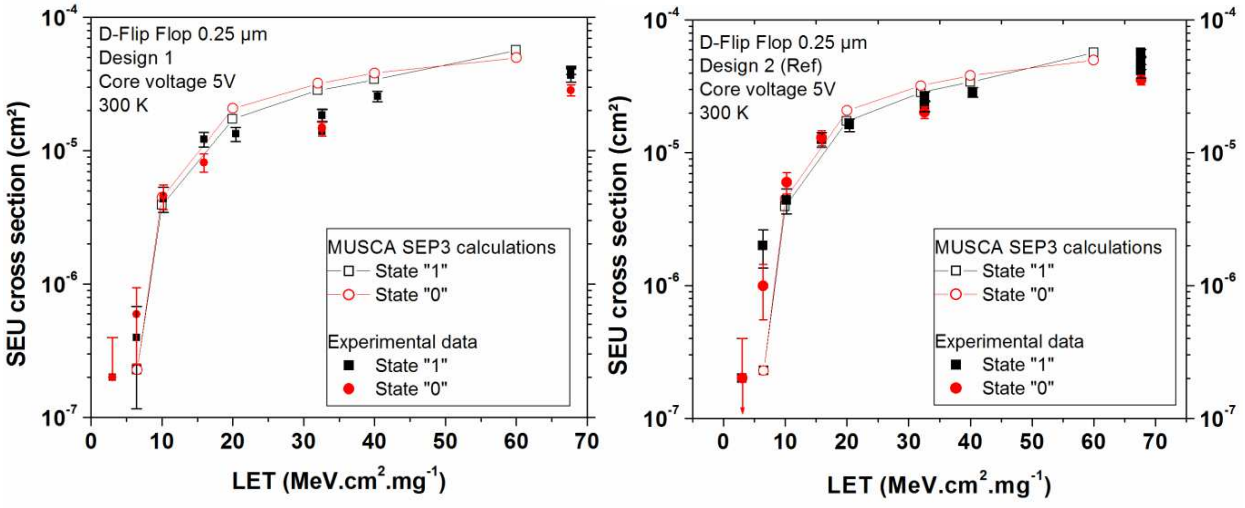
B. Comparison with experimental data under heavy ions

The experimental SEU test vehicle was developed by Sofradir and contains 2 main blocks. First a sequential block with 6 designs of shift registers are sharing Clock, Reset, Data input and Enable signals. Each shift register is composed by 200 cells of one design of flop and has its own clock gate and related clock tree. This leads to minimize the impact of the SEU over a unique and global clock tree. The second main block contains 2 x 350 arrays of memory point in shift configuration. In this work, only the sensitivity of sequential blocks is investigated. Even if all the designs were tested, in this work only two designs will be investigated because of their main uses in CMOS functions in Sofradir infrared image sensors.

The SEU test measurements have been performed during two campaigns in June 2014 and May 2015 in UCL (Université Catholique de Louvain) heavy ion test facility in Belgium. The CYClotron of Louvain la NEuve (CYCLONE) is a multi-particle, variable energy. Available heavy ions species are split in two "Ion cocktails", named M/Q= 5 and M/Q 3.3 for a range of LET from 1.1 MeV.cm^2.mg^{-1} up to 67.7 MeV.cm^2.mg^{-1}

The comparisons of experimental data and MUSCA SEP3 calculations at 300 K have been performed for 2 designs of DFF used in the readout circuit.

Good correlations in terms of LET threshold and SEE saturation of cross section are proposed, as presented in the figure 3(a) and the figure 3 (b) for the two design of DFF respectively, i.e., design 1 and design 2 (the reference design). Error bars represent the standard deviation.



(a) (b)

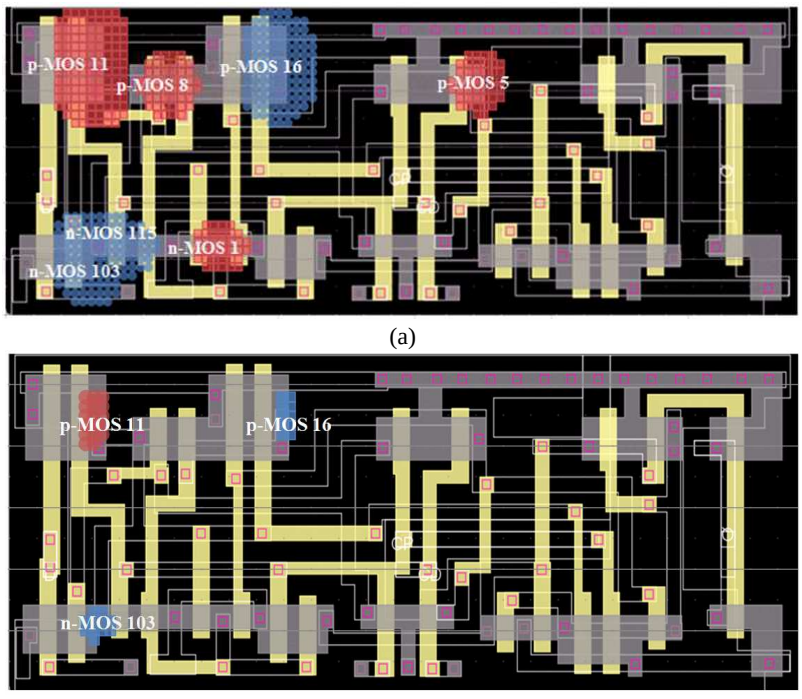
Figure 3: Comparison of experimental data with MUSCA SEP simulations f the SEU cross section of DFF for the design 1 (a) and design 2 (b), as a function and logic state, under heavy ion irradiation at UCL facility at 300 K.

After this presentation of the relevance of the prediction tool, the next section will show the failure analysis performed on the DFF cells. Actually, the other main interest of prediction tools is to allow a failure analysis at layout level with the aim to identity critical areas of the circuit.

III. Failure Analysis Dedicated for SEU Hardening

These failure analyses based on sensitivity mappings can be really useful for designers in order to determine which transistors of the cell are critical and to anticipate design optimizations. But, the kind of analysis can be also interesting to improve test plan of irradiation campaign in order to reduce the cost of space qualification of embedded devices. In previous works, MUSCA SEP3 had already shown the relevance of the estimated critical areas of SEU [10] but also for SEL (Single Event latchup) [11].

In this work, the simulation results highlight that the transistors of the input of the cell are more sensitive than the transistors of the output of the flip-flop cell as shown in figure 4. It is interesting to note that even if the global SEE cross sections are quite equivalent (Cf. Fig. 3) for the two stored logic states in the DFF, i.e., state “1” and state “0”, the locations of critical areas are strongly different.

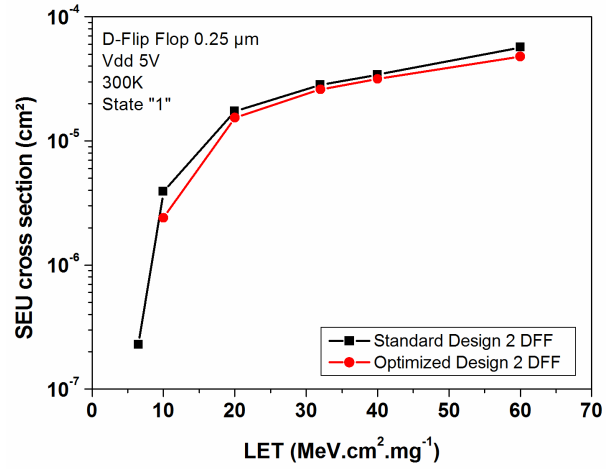


(a)

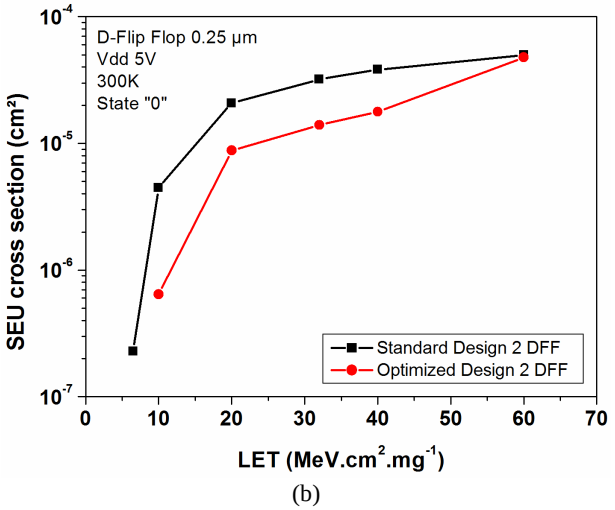
(b)

Figure 4: SEU sensitivity mappings obtained by MUSCA SEP3 calculations for the standard design of the DFF (design 2) for an ion with a LET of 58 MeV.cm^2.mg^{-1} (a) and with a LET of 10 MeV.cm^2.mg^{-1} (b), as a function of stored data: “1” (red squares) “0” (blue dots) at 300 K.

The analysis of this failure mapping at transistor level combined with the monitoring of SET on different internal nodes of the DFF cell allows for proposing design optimization. This optimization of the design cell is focus on the wider sensitive transistors, i.e., p-MOS 11 p-MOS 16, n-MOS 103, and the physical associated transistors (because of design rules). The initial cell area is kept, while the width of 6 transistors (4 p-MOS and 2 n-MOS) is decreased. This optimization allows for reducing the global power consumption of the DFF cell. Actually a decrease in width of these transistors induces a decrease in the drive current and so a decrease in the power consumption of the DFF cell during the transient states.



(a)



(b)

Figure 5: Comparisons of SEU cross sections between standard DFF design (black squares) and optimized design (red dots) at "state “1” (a) and state "0" (b) obtained by MUSCA SEP3 calculations for heavy ions for a range of LETs from 6.6MeV.cm^2.mg^{-1} up to 58.8MeVcm^2.mg^{-1}.

The figure 5 presents the comparison of the SEU cross section between standard design (black squares) and optimized design obtained by MUSCA SEP3 calculations for an ions with a range of LETs from 6.6 MeV.cm^2.mg^{-1} up to 58 MeV.cm^2.mg^{-1} at state "1" (a) and state "0" (b). The proposed design allows to reduce the SEU sensitivity of the DFF cell at all the LETs of the heavy ions. The figure 6 shows the percentage of the improvements of the SEU cross section obtained for the optimized design for the state "1" and state "0" stored as a function of the LETs. The LET threshold of the optimized DFF is increased by a factor of 1.5X, corresponding to an increase from 6.6 to 10 MeV.cm^2.mg^{-1}. It is interesting to note that the improvement in the robustness of the optimized DFF is more significant at state "0" than state "1". The difference is mainly due to the complete immunity of p-MOS 16 at state "0" for low LETs while n-MOS 1 is still sensitive at state "1". Actually, the higher sensitivity of n-MOS 1 at state "1" in the optimized DFF design is induced by the lower drive current provided by the adjacent p-MOS transistor of p-MOS 16.

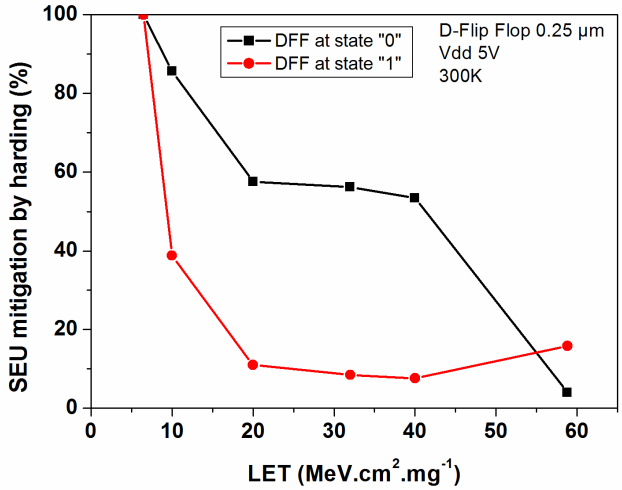


Figure 6: Percentage of SEU mitigation obtained for the optimized design of the DFF obtained at state "0" (black squares) and at state "1" (red dots) by MUSCA SEP3 simulation for heavy ions for a range of LETs from 6.6MeV.cm^2.mg^{-1} up to 58.8MeVcm^2.mg^{-1}.

IV. Conclusions

This work presents an SEE prediction tool and its interest in failure investigations and in providing a help for designers with the aim to optimize the SEE sensitivity of DFF cells used in the readout circuit developed by Sofradir. Estimations and a failure analysis at circuit level are presented considering the stored data configuration. Comparisons between predictions and experimental data obtained under heavy ion at UCL facility are consistent. The failure analysis allows for determining the critical transistors of the DFF cell with the aim to help designers to mitigate SEU by design optimization. Finally, an optimized design of the DFF cell is proposed and evaluated. The interest in term of SEU robustness is presented while the power consumption is also decreased and none area penalty is induced. The LET threshold of the new design is increased by a factor of 1.5X, while the mitigation of the SEUs varies from 85% to 10% depending on LETs and stored state. Actually, because of electrical feedback effects, the optimized design is more relevant when the state "0" is stored in the DFF.

In future works other DFF designs will be investigated and hardened with the aim to improve the global reliability

of the readout circuit of the new generation of IR device developed by Sofradir.

V. REFERENCES

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