High Performance COTS based Computer for Regenerative Telecom Payloads

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Abstract

Architectural solutions for improving robustness of space computers with regard to radiations effects enables the development of high performance computers based on commercial grade digital processing devices. The ESA study HiP-CBC (High Performance COTS Based Computer) has validated the radiation mitigation concept to soft errors with a TRL5/6 DSP demonstrator. This concept is now being applied for a new range of payload processing applications such as digital signal processing on regenerative telecom missions.

***Index terms*- Digital Signal Processing, Reconfigurable FPGA, COTS based computers, Payload Data Processing, Space radiations effects mitigation technique, HiP-CBC, SmartIO, SCOC3**

I. Context and Motivation

Commercial and scientific returns of satellite missions are closely linked with the on-board processing capabilities of a spacecraft. Higher on-board processing performance capability allows for more data to be acquired and processed in real time, thus increasing both the efficiency and the range of applications of satellite missions.

Among the main benefits, it allows to reduce the amount of information to be transferred to the ground segment for exploitation, which is typically done for science or earth observation missions. Higher processing capability also increases on-board autonomy of a spacecraft, reducing the need of a distant mission operation planning as well as the delay for delivering space data products to the final customer. At last, it enables on-board direct usage of the processed data for advanced applications such as autonomous vision based navigation and regenerative telecom payloads, opening the door to new opportunities and innovations.

Using commercial off the shelf (COTS) components for space application is a long standing idea for the space industry [1][2][3]. Its main purpose is to take benefit from an increased processing performance and from a better power efficiency driven by the mass production of electronic markets, in which the competition is fierce. With the constantly increased performance gap between state of the art space and ground technologies, standard COTS reprogrammable processing devices such as multi-core processors or FPGAs achieve today better performance than the latest space qualified ASICs.

That is why the use of COTS based computers for high payload processing applications has become an interesting alternative to fully space-grade systems. However, they generally do not fulfil space mission's expectations mainly in terms of radiation tolerance and thermal dissipation.

II. Processing Devices Radiation Tolerance

Radiation tolerance is usually divided into three main categories; Total Ionizing Dose (TID) and hard errors which result in a permanently faulty device, and soft errors resulting in temporary faulty behaviour that can be recovered.

Over time an accumulative dose of radiation degrades the transistors of circuits; tolerance to TID effects is therefore a first aspect to be taken into account when using COTS devices and must be in line with the mission requirements (duration, orbit, shielding thickness which is constrained by both the weight and the size of the payload budget).

Then, hard errors such as Single Event Latch-up (SEL), Single Event Burnout (SEB), and Single Event Gate Rupture (SEGR) may not be reversed by resetting or power cycling the system and can lead in the worst case to the destruction of the device. As a consequence, immunity to such effects is a fundamental prerequisite to enable the use of COTS for space applications.

At last, soft errors such as Single Event Upset (SEU), Single Event Transient (SET), and Single Event Functional Interrupt (SEFI) can be mitigated by various methods reviewed in [4]. In this way, by using such methods for monitoring and control of soft errors, selected COTS devices may deliver extreme processing performance with an overall level of reliability and availability which is fully acceptable for a given mission.

The traditional way for implementing space on-board computers is to achieve robustness through radiation mitigation techniques inherent to the EEE component technology and the processor design thus making them robust to all radiation effects. We call these devices "rad-hard". But this approach induces a long and costly development process which duration also increases the technology gap w.r.t. commercial devices given the fast micro-electronic technology evolution. The proposed alternative is to use selected COTS processing devices which technology ensures a sufficient robustness to radiation destructive effects (e.g. TID and hard errors). We call these devices "rad-soft". External mitigation mechanisms for monitoring and control of

the device w.r.t. non-destructive radiation effects (e.g. soft errors) are then built within the computer system itself. There are currently many rad-soft devices that can achieve much higher processing performance than existing rad-hard devices.

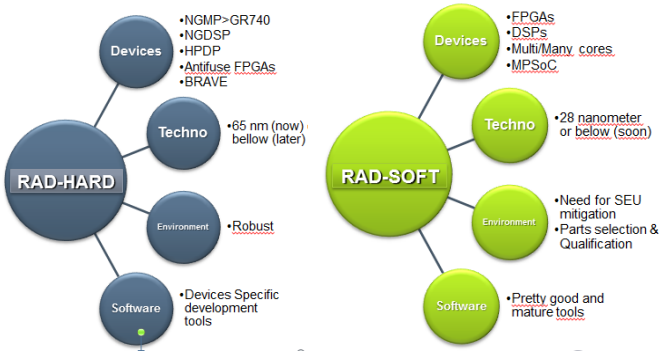

Figure 1: "Rad-hard" and COTS "rad-soft" processing devices features and examples.

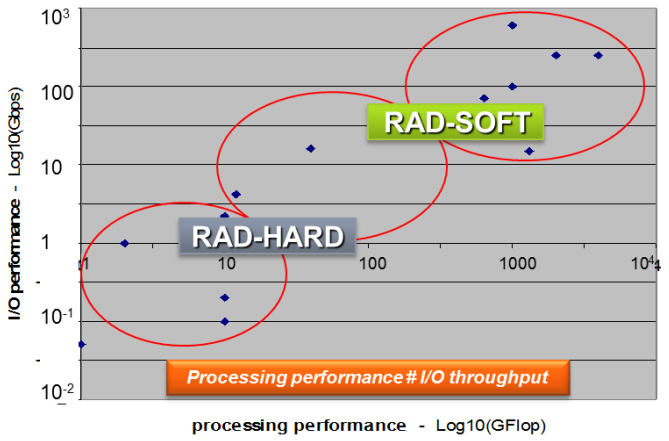

Figure 2: COTS "rad-soft" devices can achieve much higher performance than currently existing "rad-hard" devices.

III. SmartIO Mitigation Concept

A. *High Performance COTS based Computer*

Within the framework of ESA TRP/GSTP studies devoted to the development of High Performance COTS Based Computers (HiP-CBC) in space applications, a generic architecture has been defined by Airbus Defence and Space to efficiently mitigate the erratic behaviour of commercial grade processing devices such as DSPs, general purpose micro-processors, or FPGAs when they are submitted to the space radiation environment [5].

Functions for detection and management of the sporadic errors induced by the radiation effects are developed with standard space-grade device - called **SmartIO** - interfacing with one or several high performance data processing boards implemented with commercial processing devices.

SmartIO ranks among macro-mitigation techniques that tackle all types of soft errors (SEU, SET, and SEFI). It is based on an external radiation hardened unit that monitors the execution of COTS units called Processing Modules (PMs). The checking of the execution is performed at the I/O level, which is used as a coarse synchronization point to facilitate the implementation of the mitigation strategy. For that purpose, input data are divided into processing batches, are sent for computation of the COTS units, and results from COTS are finally checked. In this scheme, SmartIO is always a master while PMs are acting as slaves.

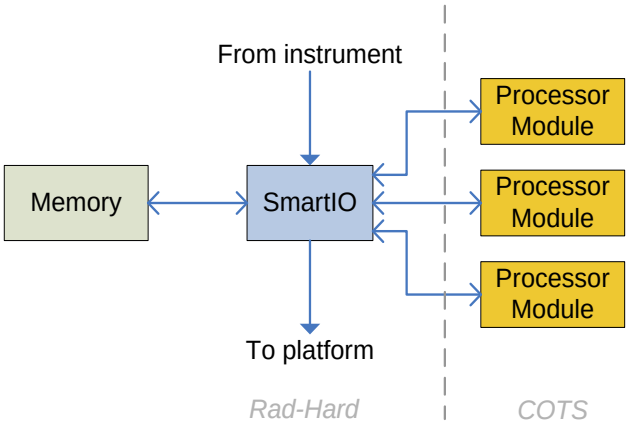

Figure 3: HiP-CBC generic architecture using 3 processor modules implementing the Triple Modular Redundancy (TMR) mitigation strategy to mask potential faults/failures into one of the channels.

Voting strategy is flexible and depends on the availability requirement of the mission:

- Hardware triplication (TMR) that allows to mask potential faults/failures without interrupting the processing;
- Hardware duplication (DMR) in which the duplicated components work in parallel and allow to only detect faults/failures;
- Time redundancy that performs the same operation multiple times on one component to compare and detect faults/failures.

Following this approach, the analysis of faults/failures is straightforward. Indeed, only three scenarios have to be taken into account:

- The PM gives an incorrect result (data corruption);
- The PM does not accept input data;
- The PM does not provide output data.

For the first case, error checking is achieved by simple comparisons of each of the result data sets, or by computing and comparing the digital signature (typically a CRC) of each of the result data sets to relax memory constraints. For the latter cases, the correctness of the execution is achieved by a configurable watchdog timeout.

SmartIO is also linked to a fast memory used as an intermediate buffer to support pipeline processing on a large number of data as well as to enable a replay mode in case of detected faults/failures.

Finally, SmartIO also brings the reconfigurable unit that is required to safely restore the context after a soft error. Recovery phase requires re-synchronizing the faulty channel with healthy ones in case of hardware redundancy, which is relatively simple for most payload applications using a coarse synchronization at the I/O level.

B. *HiP-CBC Concept Validation*

Through the HiP-CBC study, a TRL 5/6 prototype implementation with a SmartIO based on a SCOC3 component (SCOC3 is a Spacecraft Controller on a Chip including a LEON3 processor with several interfaces such as 1553, CAN bus, and SpaceWire) and COTS based processing board made around Texas Instrument TMS320C6727 DSPs has been designed and manufactured within the frame of this ESA project [6].

Figure 4: HiP-CBC SmartIO prototype is implemented with a SCOC3ASIC.

This demonstrator has validated the concept and the maturity of the so called Generation 1 of SmartIO (i.e. based on fully mature 2015 existing technologies) which remains limited to the coverage of applications with moderate needs in term of data processing due to the limited bandwidth of SpaceWire (up to 200 Mbps) and processing performance of the SCOC3 (80 MIPS). Higher rates will be required for e.g. on-board image, radar, or telecom signal processing with a support of serial links in the 1-10 Gbps range such as Serial RapidIO or the SpaceFibre currently in development.

Figure 5: DSP board developed by OHB_{CGS} with Texas Instrument TMS320C6727 DSPs.

Figure 6: The full HiP-CBC demonstrator.

IV. Application to Regenerative Telecom Mission

A. *Context*

In this paper, we introduce a typical architecture of COTS based computers that mitigates soft errors for regenerative telecom payload applications, in which digital signal processing needs are strongly increasing and lead to a “technological breakthrough” for on-board payload processing architectures.

Indeed, telecom satellites were historically mostly used as transparent repeaters (also known as “bent-pipe” repeaters), which only amplify uplink signals without processing. Nowadays, telecom satellites are often made of regenerative payloads that implement on-board demodulation, decoding, encoding, and modulation, allowing to process incoming data with advanced network functions such as scheduling and packet routing, short-term and long-term storages as well as acknowledgement and control flow features. These new functions induce a high level of complexity in the development of the last generation of telecom rad-hard regenerative Digital Signal Processors. This is a typical case for which advanced on-board processing architecture based on the use of COTS components could help to save time to market and overall cost with an increased flexibility.

B. *Machine-to- Machine communications*

Machine-to-Machine (M2M) communications, serving the broader Internet-of-Things (IoT), are receiving increasing interest. They have a very large market and growth potential, with increasing needs in the low-cost, low data rate segment. Complementing the ground networking through satellites is the only solution to provide global continuous coverage including remote and desert areas, with growing interest in low altitude satellite constellations embarking Software Defined Radio (SDR) payloads.

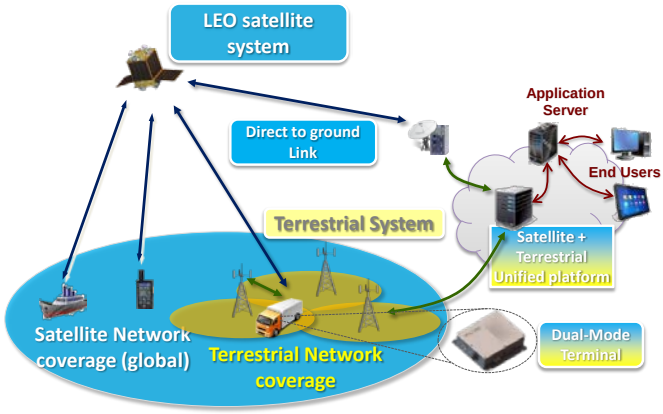

Figure 7: Overview of a M2M hybrid system with a satellite/terrestrial solution.

However, current space technologies are not adequate to offer a competitive solution for commercial services with a satisfactory level of quality of service. To be commercially successful, flexible and regenerative payloads, delivering very high performances under severe cost, size, and energy constraints are mandatory. This is where the HiP-CBC concept and its SmartIO comes in; "enabling access" to the processing performances of latest COTS components based on more power efficient silicon technologies, which is identified as the most promising strategy. Many other applications related for instance to data collection, spectrum survey or air-traffic control could also benefit of such development.

C. *Generation 2 of the SmartIO*

Exploring this promising technical path, Airbus Defence and Space is currently working on an innovative architecture of a generic Radio-Digital Processing Module (R-DSP) based on COTS components with the Generation 2 of the SmartIO. This development is performed with the support of ESA through an ARTES program and CNES through the "*Machine DSP à base de FPGA COTS*" R&T study.

To fulfil the requirements of a typical SDR payload, a preliminary analysis has shown that the SmartIO function developed in the frame of the HiP-CBC – a spacecraft controller - is not best fitted for SDR processing. For such applications, the instrument is actually a single or even a multi-port RF front-end providing one or several ADC and DAC LVDS interfaces, with a resolution of samples greater than or equal to 8 bits. Furthermore, the nature of the processing, with independent input and output data stream of samples, promotes the use of a pipelined streaming architecture for implementing the SmartIO. To achieve this, a Radiation-Tolerant (RT) FPGA offering a sufficient number of I/O pins and bandwidth capacity to be interconnected with a RF front-end has been identified as the most effective solution.

Another fundamental aspect is related to the DSP performance of COTS devices. The PHY layer of the SDR protocol developed for M2M communications (ranging from low to medium data rates) requires a theoretical capacity of at least 50 GMAC/s to process 20 MHz of cumulated bandwidth. To satisfy these needs, COTS FPGAs have been selected since they offer a good trade-off between performance and flexibility.

Among the different types of FPGA technologies, SRAM-based FPGAs – in which both the configuration and the application layers are based on SRAM cells – have been chosen for several reasons. As summarized in Table 1, each FPGA technology comes with its strengths and weaknesses. SRAM-based FPGAs provide the most powerful devices in terms of throughput and capacity and are the only type of FPGAs to support online reconfiguration feature. In the context of SDR payloads, flexibility to support multi-missions and upgrades being a major asset, this technology is obviously the most promising.

However, SRAM-based FPGA is also the most sensitive technology to soft errors, mostly because of the nature of the configuration memory based on SRAM cells. On the contrary, flash and anti-fuse based FPGAs provide better intrinsic resistance since their configuration memory is soft error immune, but lack behind in performance and capacity due to the use of old CMOS processes; respectively 65 nm and 150 nm compared to 16 nm for latest SRAM-based FPGAs. A significant gap in the electronic world!

Nevertheless, this weakness can largely be compensated by the efficiency of the SmartIO mitigation technique, in which the availability is scalable and can be adapted by choosing the appropriate voting strategy thanks to a modular architecture.

Table 1: Comparison of FPGA technologies (2016)

Feature	Anti-fuse	Flash	SRAM
Reprogrammable	No	Yes but limited	Yes
Volatile Configuration	No	No	Yes
Online Reconfiguration	No	Not Recommended	Yes
Capacity	Low	Medium	Very High
DSP Performance	Low (125 MHz)	Medium (350 MHz)	Very High (700 MHz)
Soft Error Sensitivity	Low to Very Low	Medium to Low	High
TID Tolerance	High	Low to Medium	High

The resulting architecture for COTS based computer for regenerative telecom payload is depicted in the following picture (Figure 8).

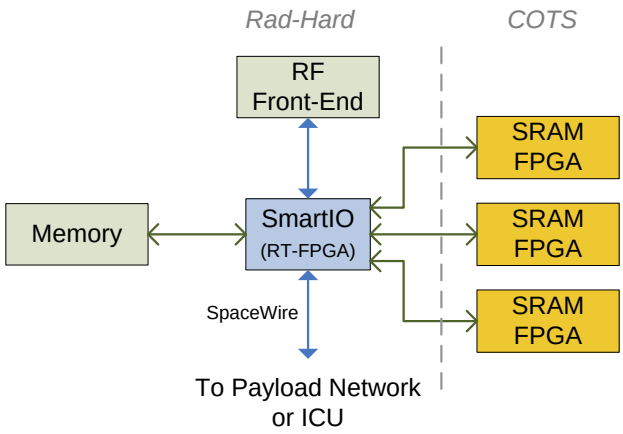

Figure 8: R-DSP architecture based on RT-FPGA for the SmartIO and 3 SRAM FPGAs for PMs.

In this scheme, SmartIO function is implemented using a RT anti-fuse FPGA while commercial SRAM FPGAs are used to implement the high processing layer of the R-DSP module. A non-volatile memory is used to store multiple bitstreams that contain necessary information for the configuration of SRAM FPGAs for a given mission. Since the SRAM FPGA configuration memory is volatile, this is required each time the R-DSP is activated. This is also necessary for the recovery phase when a soft error has been detected by the SmartIO. The configuration port of PMs is driven by the SmartIO FPGA, to ensure the correctness of the programming. At last, a SpaceWire link is also part of the design to provide a standard interface between the SmartIO and the rest of the payload network.

V. Conclusion

The use of commercial electronic components in space avionics is becoming an attractive solution for high performance payload processing applications, in which availability and reliability requirements can be achieved through the use of different design mitigation schemes. The growing performance gap between the commercial electronic components and the space grade components suggests that COTS based computers are a strategic research topic for space on-board data processing and avionics. Several studies with ESA, CNES, and other national agencies have explored this way at computer architecture level as well as for high performance processing COTS devices and technologies. This paper has introduced the development by Airbus Defence and Space of an advanced COTS based computer architecture based on FPGA technologies enabling flexible and high performance SDR data processing in future space applications. A TRL 5/6 demonstrator is expected at the end of the 2016 year.

VI. References

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