Digital Programmable Controller (DPC) : from Concepts to Space Applications

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Abstract

Thales Alenia Space has completed the development of a radiation hardened mixed-mode circuit: the DPC (Digital Programmable Controller). This system on chip is a major breakthrough in the availability of radiation hardened highly integrated European micro-controller. This component uses the IMEC RHBD DARE on UMC 0.18µ library [6] and analog IP designed full custom by ICsense [4]. The formal Qualification against ESCC9000 is under completion while the first flight models are launched in the manufgactruing process.

First DPC ASIC's were assembled in March 2014. Since this major project milestone, the device has successfully been integrated into quite a large range of applications.

Evaluation board was built allowing end-users to quickly start developing their application. The board is a rich self-contained prototyping tool (i.e. no other devices needed than a USB plug on the SW development PC). It contains a large set of analog peripherals together with classical interfaces used in space applications such as mil-1553, dual CAN, RS4xx … Hence external designers start developing with the DPC in an space system context within less than 2 working days [10] including learning curve of the associated software development tools.

The DPC is an essential building block for the development of intelligent avionics modules that for the first time allows to implement space grade-1 decentralized control such as promoted in the ESA-SAVOIR reference architecture for RTU. DPC is now the core controller of next generation avionics product from Thales Alenia Space where it is used to control power distribution, motor, thrusters, pyro for LEO and GEO satellites.

The DPC plugin module is a small space grade board containing the DPC, drivers, power supply and protection circuit. The designer of a new avionic module for specific scientific missions can easily plug it onto its customized mother board and has only to take care of high voltage or power interfaces.

The DPC has already been transferred outside Thales group to third parties like ONERA for the design of gyro module [10] and to DLR for the design of motor controllers for robotic arm.

I. DPC OVERVIEW

A. Development strategy

The construction of the DPC is the result of a 4 parties project involving IMEC, ICsense and Thales Alenia Space under an ESA development.

IMEC not only has provided the RHBD DARE+ on UMC 0.18µ library, but also extended it with additional features. Dual port memories are being used to transparently perform memory scrubbing in a seamless manner for the processing unit. The DPC embeds 60kbytes of memory split over several banks. Clock gating cells have been also added. As the DPC embeds a large range of features, power consumption may become an issue if all of them would be active simultaneously. At boot time, a hardware configuration is loaded in the circuit to only deliver clock toward functions relevant to the target application.

IMEC also performed top level layout integrating digital netlist and analog macros, performing DRC to check for compliance to particular radiation hardening rules and finally the interface with UMC foundry.

ICsense has designed a large set of analog IP blocks which were included on the die and successfully tested to reach targeted performances.

A. DPC architecture

Figure 1 depicts the DPC internal architecture. Intentionally, the DPC embeds a very large set of functions. As compared to a µC from the industrial world this may be overkill. However, the economics of space components is very much different. Production volumes are very low as compared to consumer or industrial markets. Hence the silicon area accounts for a very small amount in the total cost breakdown of such a project. The circuit was therefore equipped with so many features, that it is nearly impossible to find a concrete application using all the available resources at once.

As a drawback, not only silicon area increases with the number of functions but also power consumption. Therefore, prior to firmware execution, the DPC enters a hardware configuration cycle. During this phase, a "hardware configuration" map is loaded from the non-volatile memory that defines which functions should be active (useful for the application) and which functions will be made sleeping (clock gating and full sleep mode of analog blocks). Furthermore, operating frequency can be defined such as to match exactly speed performance and processing power needed for the target application. Using these mechanisms, the DPC power consumption can vary up to a factor 7, from minimalist low

end use cases up to the unrealistic worse case where all functions are used at maximum operating frequency.
It is really important to underline that the DPC is not a "multicore architecture" as named in µprocessors. The DPC- which is OS free- allows to program simply and separately 3 µC that are interconnected through DPRAM(mailboxes).

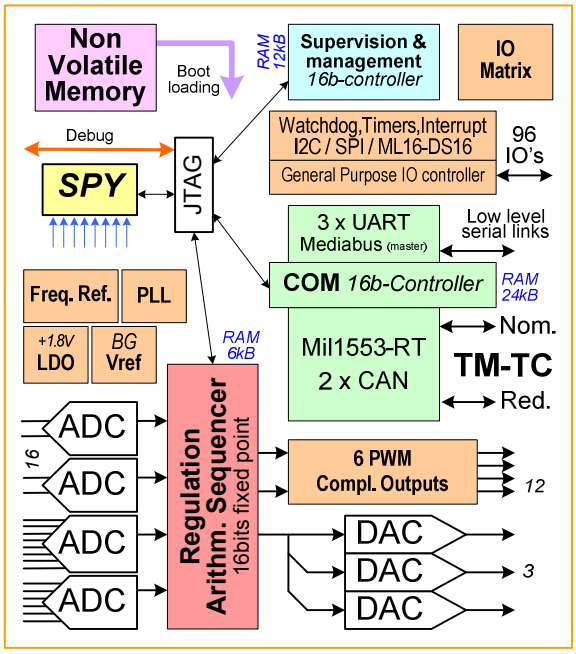

Figure 1: Block Diagram of the DPC

B. *On chip analog blocks*

The DPC is a mixed-mode circuit that contains the following analog blocks:

- Reference voltage and current generation
- Power-management block with LDO's
- 120 MHz frequency reference system (PLL) to provide the clock to the digital part
- 100kHz reference oscillator
- 4 flexible 13 bit , 1MSps ADCs with extensive input muxing capabilities
- 3 12 bit, 3.75 MSps DAC current-mode outputs
- Power-on-reset circuit and under voltage detector
- Rail to rail comparators, PGA (20dB)

Test results of the analog blocks (PLL, ADC, bandgap) can be found in [5]. The blocks design have been explained in more details in [4].

Thanks to careful design with either taking into account Vth shift with total ionising dose or using ELT transistors at specific positions of the analog design & the ICsense proprietary, automated SET hardening simulation environment (used to assess and decrease the SET sensitivity of the analog IP) the chip turned out to first time right in being radiation hardened.

C. *Digital processing*

Processing is based on several instances of the OpenMSP430 fixed-point 16bits CPU core. This processor features the instruction set of the PDP11 (1970) from Digital Equipment Corp. The openMSP430 [0] is a synthesizable 16bit microcontroller core written in Verilog. It can execute the code generated by any MSP430 tool-chain in a near cycle accurate way. To fasten the execution, the CPU is equipped with one hardware 32 bits MACC function and one integer divide unit.

On one hand, digital control is offering new possibilities in driving smarter and more efficient systems. On the other hand connectivity is being more and more present in all applications. In order to avoid searching for complex and touchy compromises between robust loop control and communications or host functionality the architecture offers one CPU per task, as presented on figure 1

For communications to the outside world, the CPU has several hard wired units: 3 x UART, 2 x CAN bus and a MIL-1553b remote terminal function.

Another CPU instance (the "RAS") is intended to execute a configurable and repetitive sequence of basic mathematical or logic instructions within a short cycle. This sequence can be programmed so that any mathematical expression typical of regulation scheme is realized: structures such as Proportional, Integral and Derivate (PID). This sequence can also be programmed to acquire and post-process multiple sensors or pre-process signals before being generated to hardware signals.

Finally one CPU is available to perform all local (host) supervision & management functions.

The highly flexible hardware unit "USI" (Universal synchronous Serial Interface) is able to drive with quite various timing requirements the following communication protocols: SPI, I2C, ML16-DS16, serial in-parallel-out IO extenders.

Figure 2: The DPC ASIC

D. *DPC status*

The development of the DPC was a long story that was initiated back in 2008 with a relatively long definition process investigating many applications needs and defining the requirements for future product generations of satellite equipments using micro-controller technology.
Started in 2012 in the frame of an ESA Artes 5.2 contract, the main development of the Digital Programmable Controller DPC has reached major milestones in 2015 : The ASIC successfully passed the analog characterization and the radiation tests covering heavy ions, protons, and Total

Ionisation Dose tests, allowing to proceed with the formal qualification process.

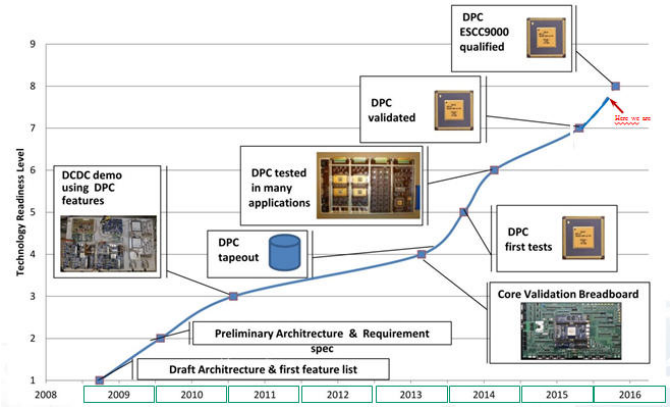

Figure 3: The DPC ASIC TRL maturation timeline

Intensive tests plans were successfully passed in order to validate the DPC performances under extreme temperatures and under radiation environment. The formal qualification for space use process (in the frame of an ESA Artes 3-4 contract) is under completion and first space grade 1 devices are in production.

Up to now, more than 400 DPC ASICs have already been produced for test, evaluation, supply chain validation and qualification purposes.

II. Using the DPC

A. DPC Reference Kit: hardware

In order to support the DPC dissemination, a DPC reference kit (DRK) has been built. This board allows the designer to takeover the DPC features and to start programming in a convenient and friendly environment.

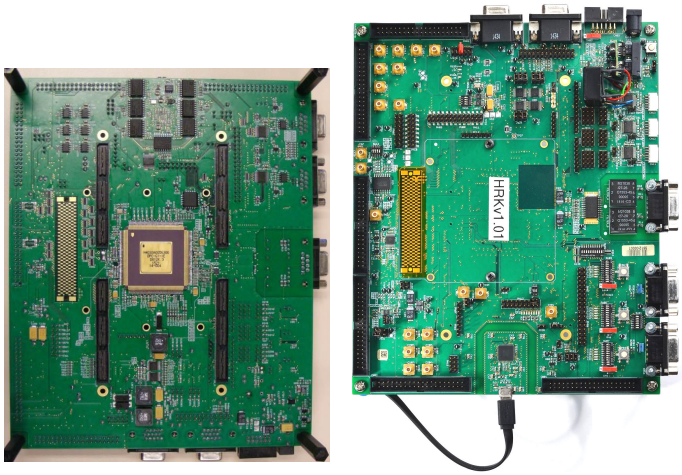

Figure 4: The DPC user Reference Kit hardware

The board is a very rich self-contained prototyping tool (i.e. no other devices needed than a USB plug on the SW development PC). It contains quite large set of analog peripherals together with classical interfaces used in space applications such as mil-1553, CAN, RS4xx … The USB to JTAG bridge allow a direct connection to a USB port of the software development PC. Buffers are foreseen at the output of the PWM generators and at output of the DAC to drive directly strong load connected to the DPC.

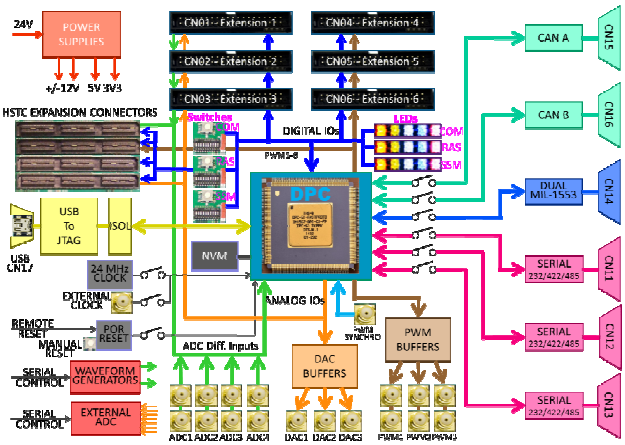

Figure 5: Content of the Dpc evaluation board

B. DPC Reference Kit: Software suite

The DRK is made available with a SW development toolkit including compiler , debugger, boot loader, … as listed here below in the table.

Tool Name	Function
msp-gcc	Open source tools for MSP-430, including: • compiler: msp430-gcc • Linker: msp430-ld • Object dumper: msp-objdump • Debuggers: msp430-gdb • Instruction simulalor: msp-debug • Size analysis: msp430-size
dpc-minidebug	Hardware-oriented graphical interface tool enabling simple interaction with the DPC openMSP430 cores. Allows examining and patching registers and memory, setting breakpoints, halt, run and step by step execution.
dpc-gdbproxy	Provides the proxy function for GDB. Replaces the msp430-gdbproxy provided by the mspgcc toolchain.
dpc-pkt	Transforms .elf file in a format compliant to the packet definition.
dpc-programmer	NVM programmer tool and global loader. Writes hardware configuration and program packets in the NVM or loads them directly in the DPC and cores memory through the boot manager.
dpc-configuration	Hardware configuration packets editor.
dpc-crc16	Utility to compute and check the CRC on hardware configuration and programming packets.
Mspdebug	Used in DPC as a MSP430 simulator.

Figure 6: Content of the DPC SW development suite

C. *DPC plugin module: Flight models*

After prototyping, the designer works comes to flight model design. A building block has been developed and is proposed for quick & easy integration of the DPC into equipment. This makes designer life easy as the DPC comes in the form of a mezzanine board that simply needs to the plugged onto the main PCB of new applications. The designer can focus on the main news parts of its system and can rely on a pre-validated & space qualified control module. In term of design effort, it saves therefore the effort of creating an electrical design and tricky layout of analog parts of the DPC and its peripherals and it seriously reduces risks.

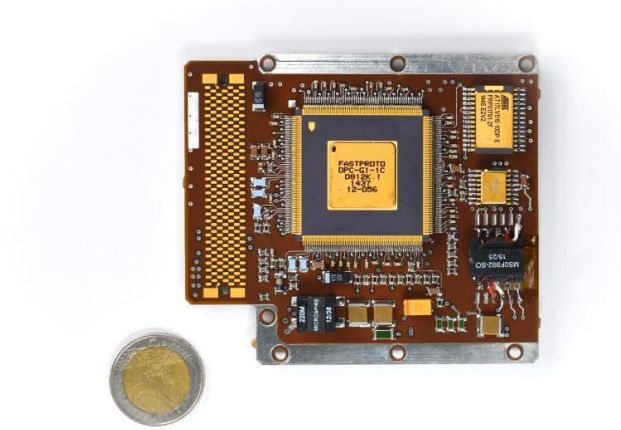

Figure 7: The DPC plugin module

Next to the controller, the DPM (DPC Plugin Module) contains (See figure 8) a 28V dc-dc power supply together with a latching current limiter such that it allows a fail-safe direct connection to an LEO unregulated bus. The board comes also with a dual CAN driver interface to address nominal & redundant communication bus that may for example be used as a backplane data bus [9] into a RTU.

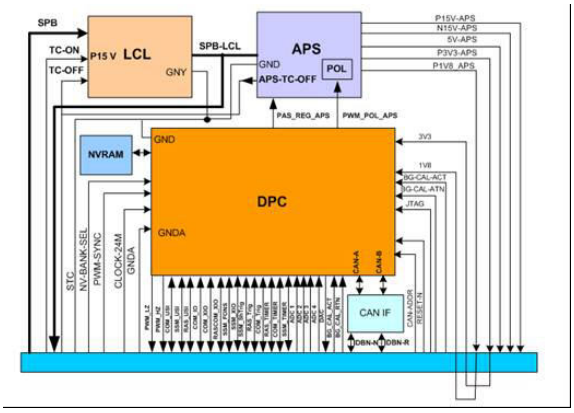

Figure 8: The DPC plugin module architecture

This modularity also simplifies the firmware development process & firmware pre-validation that pay take place at DPM level (without) the main application board. Finally a standardized controller board makes teaming agreements between different companies a much easier job, as each party can focus on its sub-module & associated functions without having to take care of the backplane interface and control.

III. USE CASE EXAMPLES

A. *Avionics*

In parallel with the DPC ASIC, Thales Alenia Space has developed a new generation of "high power" avionic equipment intended to be at the heart of the Spacebus NEO solution, the SDIU MK2 [8].

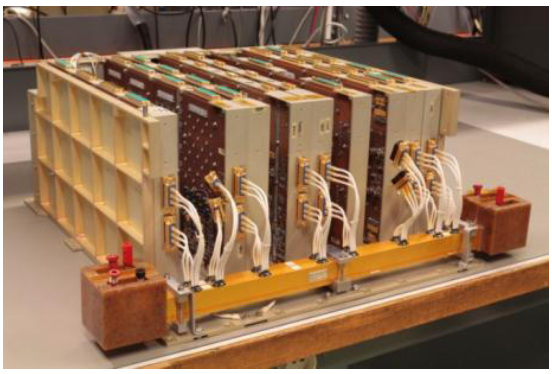

Figure 9: High power avionics using DPC

Thanks to the intrinsic versatility and flexibility of the DPC, the controller module was implemented with each of the different boards of the SDIU, covering a wide range of applications :

- Interface to the on board computer (external 1553) & data relay from/to the back plane bus. via CAN bus. All CAN communications being performed by DPC's.
- Full step motor drive is mainly for the positioning of the steerable telecom antennas, but the same module is able to cover both that functionality
- Distribution of power to platform units,
- Distribution and control of heaters
- Interfacing with the 4 reaction wheels on the satellite.
- Command and control of all of the elements of the chemical propulsion: valves
- Micro Step solar Array Drive: command and control of the solar array deployment and the solar array mechanism motor driving in micro-step mode.
- Monitoring of Li-Ion cell and battery voltages, and command and control of cell bypass and cell balancing elements.

All these functions are distributed over several boards such that there are no 2 identical boards: hence 7 different application software have been developed to perform these functions. This is a major breakthrough as the function was implemented in previous generation of the product using 6 different specialized ASICs.

The DPC ASIC is currently used in the new Thales Alenia Space RTU avionics product range, consistent with SAVOIR roadmap.

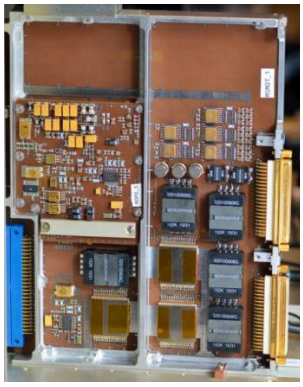

Figure 10: RTU board with the plugin module @ center left

B. Gyroscope acquisition & processing (ONERA)[10]

ONERA has been developing vibrating MEMS inertial sensors for various applications. The VIA cell (Vibrating Beam Accelerometer family) is already in use in the French civil and defence industry. The VIG cell (Coriolis Vibrating Gyroscope family) has been proposed for space applications, in the frame of low cost assistance gyroscope associated with star trackers on satellite platforms : detumbling, slowing down satellite rotation to allow star tracker acquisition, but also safe mode, short term navigation, with higher performances.

Electronic architecture of the gyroscope has been mapped on the DPC cores and peripherals, and requirements set in terms of A/D D/A converters, voltages, CPU usage, and communication with host. The required digital signal processing functions perfectly match the intentional asymmetric core design of the DPC, and all three cores are in use in the application. The program memory is tiny for each core (4K, 8K, 16K), but keeping an eye on assembler generated by the compiler allows the programmer to write clean yet efficient code.

The performance of several functions of the DPC have been evaluated in real conditions, such as ADC resolution. the word length of a single acquisition is 13 bits; when measuring a constant voltage, the ADC resolution is 0.1 lsb after averaging, which is equivalent to 16 bits at 10 ms, limited by 1/f noise. But when measuring a modulated signal on a carrier, the 1/f noise disappears and the resolution is 0.0005 lsb at 100 s (corner frequency is about 0.1 Hz), which is equivalent to 23 bits. Therefore we conclude on the use of the DPC for metrology applications

This work [10] has been funded by CNES, with special support of Thales Alenia Space Belgium.

C. Robotic arm motor control: (DLR

The DLR Institute of Robotics and Mechatronics is going to develop a new multi-sensorial robotic arm with seven joints for space applications like On-Orbit-Servicing. Each joint of this robot shall consist of a Force-Torque-Sensor, an absolute position sensor for the drive side and a motor commutation sensor for the used BLDC motor. All these sensor data are processed at each joint with the control loop frequency of 1 kHz. In addition, the motor commutation shall be performed at a rate of 40 kHz. Therefore two processors are used to decouple the basic tasks: Joint Control and Motor Control. The DPC from Thales Alenia Space Belgium is under prototyping as candidate for performing the Motor Control task.

The new multi-sensorial robotic arm CAESAR (Compliant Assistance and Exploration Space-Robot) shall consist of seven joints in an alternating rotational and bending arrangement. A CAD rendering of the intended design with an applied gripper at the tool center point is shown in figure 11.

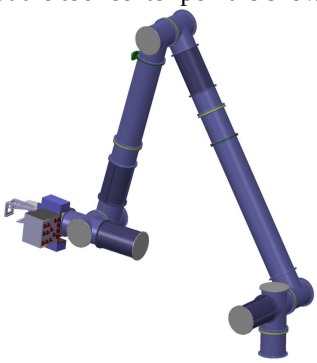

Figure 11: Multi-sensorial robotic arm CAESAR

Contrary to the preceding ROKVISS experiment [11] in which standard automotive part where used and performed well in outer space for more than 5 years, CAESAR shall be capable to meet multiples mission requirements. Additionally, since the design and manufacturing of the ROKVISS joints is now several years old, some of the used components are obsolete. Together with changed mission parameters, the envisaged improvements and changes in the design it is necessary to redesign the electronics of the robotic arm.

The approach for CAESAR is to use space qualified components where possible. If space qualified components are not available with the same functionality we will use military or automotive rated components which are radiation tested and if necessary protected against latch up. This approach is the only feasible way to build complex joints with the same functionality as the ROKVISS joints.

The main subsystems of each joint are:

- local power supply with latch-up protection
- motor power inverter
- communication and control unit
- joint torque and position sensor for each joint
- motor commutation sensor

The motor control of the BLDC motor is based on a current control algorithm and a Space-Vector-Modulation for the current set-point vector. The whole current control loop (incl. the Space-Vector-Modulation) must be performed at a rate of 40 kHz in order to enable a motor speed of 50000 electrical revolutions per minute.

The base of the current control loop are the measured current values of all three motor phases and the inverter voltage which must be sampled in parallel at one step to minimize the phase errors. In addition, some communication tasks and housekeeping data monitoring at a lower frequency must be performed, too.

For this challenging task, the DPC from Thales Alenia Space has all required peripherals on chip. DLR is right now evaluating the DPC in this robotic arm context.

IV. Analog IP transfer

In the frame of this DPC development, several analog function have been implemented in the DPC. These are available in the form of IP blocks [4] & [12].

As an example, Thales Alenia Space UK is currently running a ASIC development program based on the IMEC DARE+ library. That development will leverage on the DPC to reduce the risk involved with mixed mode design by integrating ADC, PLL & voltage reference from the DPC program.

The ESA SSDP development program will also re-use analog IP from the DPC.

V. Conclusions

Thanks to an efficient cooperation with IMEC, ICsense and ESA, Thales Alenia Space Belgium has built an innovative highly integrated mixed signals controller.

Its high level of configurability and its large set of communication interfaces allow the usage of the Digital Programmable Controller (DPC) in a broad range of applications such as scientific payload control, motors, actuators, battery management, power management … wherever a decentralized control makes the overall solution more efficient.

The outcome of the project is not only as a space qualified component but mainly a set of tools making end users life easier and reducing risks: a Reference Kit for rapid prototyping and a Plugin Module for quick integration into new designs. The software development toolkit includes all standard tools such as compiler , debugger, boot loader, …

These tools have been already extensively be used by Thales Alenia Space as “local” customer but also transferred to alpha customers: Onera & DLR. The DPC is now ready for large deployment into any space application.

VI. Acknowledgements

The authors would like to warmly thank:

ESA project team from both µE and power divisions for their great support and many advices in conducting this project.

Mr. Olivier Girard who spent hours in the design of the openMSP430 core and has finally posted it in free BSD licence [1] available to anyone’s usage on internet (http://opencores.org/project,openmsp430).

M. Durvaux for its clever guidance in the selection of this processor, the top-level chip architecture and the associated patent [2].

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Mr. Hans Juergen Sedlmayr from DLR for his kind support in publishing this preliminary information on testing the DPC in a robotic context.

VII. REFERENCES

[1] OpenMSP430 technical data by Olivier Girard http://opencores.org/project,openmsp430

[2] “Device with power electronics control circuits” European Patent EP20100171077 (2012-02-15*)* *M. Fossion M. Durvaux*

[3] “ Radiation Hardened Mixed-signal IP with DARE technology” G. Thys, S. Redant, E. Geukens, Y. Geerts, M. Fossion, M. Melotte, in Proc AMICSA 2012.

[4] Bram de Muer ICsense “Rad-hard, high-performance analog and high-voltage IP in 0.18um CMOS (DARE)” ESA IP-cores day Sept 2013

[5] "A mix-signal radhard micro-controller: DPC", *Marc Fossion Alain Van Esbeen, Richard Jansen, Eldert Geukens, Steven Redant, Claudio Monteleone, Yves Geerts,* June 2014 AMICSA @ CERN Zurich

[6] Introduction to the DARE platforms Mr. Steven Redant IMEC @ DARE User Day ESTEC 8 December 2014

[7] “Digital Programmable Controller – DPC” *M.Fossion & A. Van Esbeen* @ CCT CNES Nov. 2014

[8] “DPC application in Avionics / RTU” A. Nairn & Ch. Maillard @ 9th ESA Workshop on Avionics, Data, Control and Software Systems ADCSS2015

[9] "CAN Backplanes and the DPC "*Van Humbeeck Thierry & Lizin Gilbert@* CAN in Space ESA workshop, 10 March 2016

[10] “MEMS Gyroscope Demonstration for Space Application, using a DPC” Dr. Jean GUERARD *(ONERA) @ AMICSA 2016*

[11] Verification of Advanced Light Weight Robotic Joints and Tele-Presence Concepts for Future Space Mission *K. Landzettel and A. Albu-Schaffer and B. Brunner and A. Beyer and E. Kramer and C. Preusche and D. Reintsema and B.M. Steinmetz and H.J. Sedlmayr and G. Hirzinger* 9th ESA Workshop on Advanced Space Technologies for Robotics and Automation ASTRA 2006

[12] “Radiation hardened high-voltage and mixed-signal IP with DARE technology” Eldert Geukens, Jan Dielens, Bram De Muer, Geert Thys, Steven Redant(1) *@ AMICSA 2016*