Comparison Study of Bulk and SOI CMOS Technologies based Rad-hard ADCs in Space

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Abstract

The electrical and radiation characteristics of the bulk and silicon-on-insulator (SOI) CMOS based rad-hard analog-to-digital converters (ADC) in space are compared in this paper. A 10bits monolithic, high reliability pipelined ADC with 25MHz conversion rate is presented as a prototype to exhibit the benefits of radiation hardened by design (RHBD) and radiation hardened by process (RHBP) approaches. The ADC prototype hardened by RHBD is fabricated with 0.35um bulk CMOS technology and radiation hardened SOI CMOS technology with an identical technology node respectively. The experimental results show that the SOI-based ADC achieves the total ionizing dose (TID) tolerance of 300krad(Si), nearly one order of magnitude higher than the bulk ADC, and the single event upset (SEU) cross-section of 9.6E-6cm^2/device at 63MeV·cm^2/mg linear energy transfer (LET), lower than the bulk ADC by two orders of magnitude. The SOI-based ADC is also better than the bulk ADC in the electrical characteristics. It is more suitable for harsh radiation environment applications.

I. Introduction

In the harsh space environment, the integrated circuits within various electronic equipments often suffer from serious degradation due to the radiation effects, which lead to compromise spacecraft reliability [1,2] . As the interface between analog and digital circuits, analog-to-digital converters (ADC) are widely used in aerospace electronic equipments, and its reliability has received more attention. Radiation hardened silicon-on-insulator (SOI) CMOS technology has many advantages comparing with bulk CMOS technology, such as higher speed, lower parasitic capacitance, smaller short channel effects, etc. Especially due to its excellent capability of radiation hardness, the rad-hard SOI CMOS technology is more suitable for space applications.

Until now, intense interest has been paid in the radiation effects and hardened approaches of ADC [3-6], and the transistor level comparison between SOI CMOS technology and bulk technology is also studied extensively [7-10]. But there is seldom research on circuit level comparison between SOI CMOS technology and bulk technology for analog and mixed signal circuits, especially for ADC in space. In this paper, the electrical and radiation characteristics of the bulk and SOI CMOS based rad-hard ADCs in space are compared. A 10bits monolithic, high reliability pipelined ADC with 25MHz conversion rate is presented as a prototype to exhibit the benefits of radiation hardened by design (RHBD) and radiation hardened by process (RHBP) approaches. The ADC prototype hardened by RHBD is fabricated with 0.35um bulk CMOS technology and radiation hardened SOI CMOS technology with an identical technology node respectively. Both ADCs are tested under the same conditions and environment for comparison.

This paper is organized as follows: section II introduces the system architecture of the pipelined ADC prototype, section III describes the circuits design of the ADC prototype, the RHBD and RHBP approaches are provided in section IV, section V shows the experimental results and discussion on electrical and radiation characteristics, followed by a brief conclusion in section VI.

II. System Architecture

The block diagram of the pipelined ADC prototype is illustrated in Figure 1.

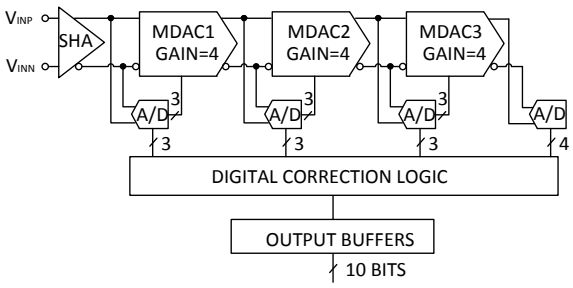


Figure 1: Block diagram of pipelined ADC prototype

In the front end of the converter, a sample and hold circuit is used to extend the input bandwidth of the ADC, followed by a cascade of three identical stages in which each stage performs a 2.5bits coarse quantization. The last stage is a 4bits flash ADC. Finally, the 13bits coarse quantization results are feed into digital correction logic to generate 10bits resolution at the output of the pipelined ADC.

III. Circuits Design

A. Sample and Hold Circuit

The sample and hold circuit (S/H) is based on a capacitor flip-around architecture [11], as shown in Figure 2.

Compared with a charge transfer S/H, the capacitor flip-around architecture S/H exhibits the advantages of lower power consumption, smaller die size and better radiation hardness capability due to its larger feedback factor and lower

load capacitor which can maximize the closed-loop gain and bandwidth of amplifier. In order to reduce the nonlinear effects of the switch caused by charge injection and clock feed through, the bottom plate sampling technique is adopted. To improve the input bandwidth of the S/H, the bootstrapped switch [12] is used on SW1, SW2, SW3 and SW4 in Figure 2.

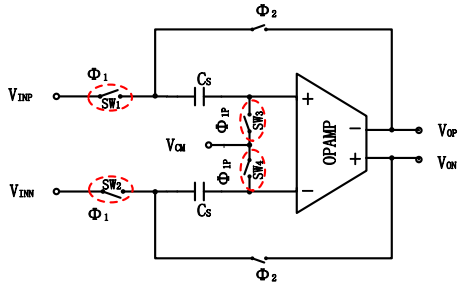


Figure 2: Sample and hold circuit

A high performance operational amplifier (opamp) is included in the S/H. Threshold voltage drift, migration rate and transconductance degradation caused by total ionizing dose will reduce the gain and the bandwidth of the opamp, increase DC offset, and finally affect the performance of the circuit, so the margin must be sufficient when designed [13]. A gain-boosted folded cascade amplifier is used in the S/H [14], as shown in Figure 3. This structure can efficiently improve the gain without reducing the bandwidth of the opamp.

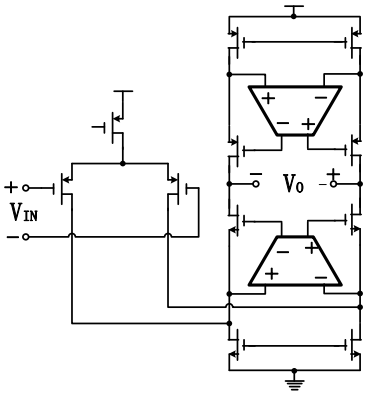


Figure 3: Gain-boosted folded cascade amplifier

B. Switched Capacitor Comparator

A switched capacitor comparator with a preamplifier is adopted, as shown in Figure 4.

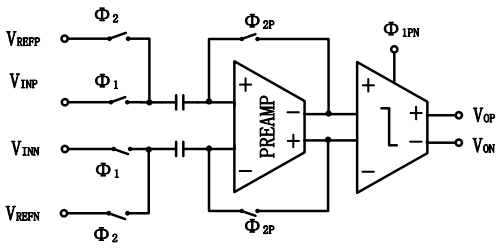


Figure 4: Switched capacitor comparator

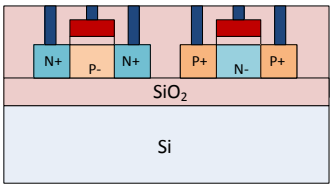
The switched capacitor structure can extend the input common mode range of the comparator, and the DC offset of the comparator can be reduced within a lower range due to the preamplifier. Thus the comparator allows larger tolerance for the error caused by radiation.

IV. Radiation Hardened Approaches

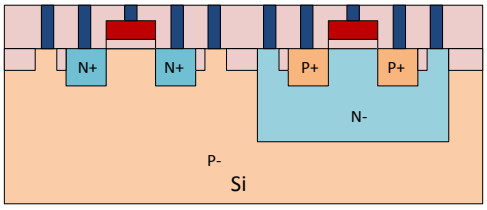
A. Hardened System and Circuits

In order to improve the radiation performance of the ADC prototype, the 2.5bits/stage system structure, the capacitor flip-around S/H, the gain-boosted folded cascade amplifier and the switched capacitor comparator with a preamplifier are all carefully determined and designed as described in section III. The values of the currents and capacitors in those sensitive parts are increased properly for the purpose of radiation hardness. By implementing the above RHBD approaches, the ADC prototype generates much smaller deviations when radiated. If the deviations from comparators are small enough to locate in the error correction range of the pipelined ADC, they will be corrected by the digital error correction logic.

B. Rad-Hard SOI CMOS Technology



(a)SOI CMOS



(b) Bulk CMOS

Figure 5: Cross-section views of SOI and bulk CMOS technologies

The SOI CMOS technology joins silicon dioxide as a buried insulator layer on silicon substrate as shown in Figure5 (a). The complete isolation between NMOS and PMOS eliminates any of the latch-up events [15]. Compared with bulk CMOS technology, the SOI CMOS technology could mitigate the sensitivity of single event upset (SEU) and single event functional interrupt (SEFI) due to its much smaller charge collection volume. As a result of the radiation hardened techniques, the total ionizing dose radiation tolerance of the rad-hard SOI CMOS technology has also reached a fairly high level. Figure5 (b) is the cross-section view of the bulk CMOS technology.

C. Hardened Layout

Contrasting with the immunity of single event latch-up (SEL) of the SOI CMOS ADC, the bulk CMOS ADC has to be implemented with reasonable and rigorous layout rules to mitigate the sensitivity of SEL. The substrate contact around the transistor should be sufficient to avoid the latch-up,

especially for the NMOS and PMOS which are close to each other [16], as shown in Figure 6.

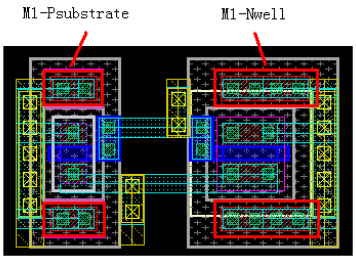
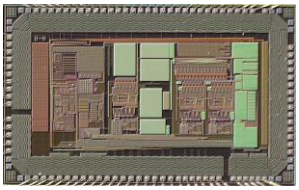


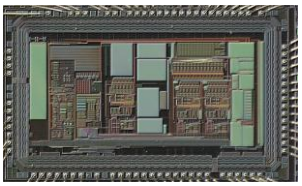
Figure 6: Hardened layout

V. Experimental Results

The micrographs of ADC in different technologies are shown in Figure 7, respectively. The electrical and radiation characteristics of the two ADCs are tested for comparison.



(a) SOI CMOS ADC



(b) Bulk CMOS ADC

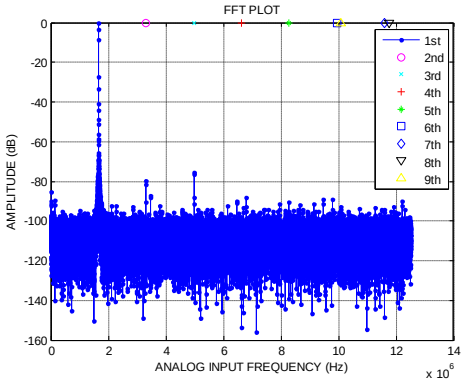
Figure 7: Micrographs of ADC in different technologies

A. Electrical Experiment

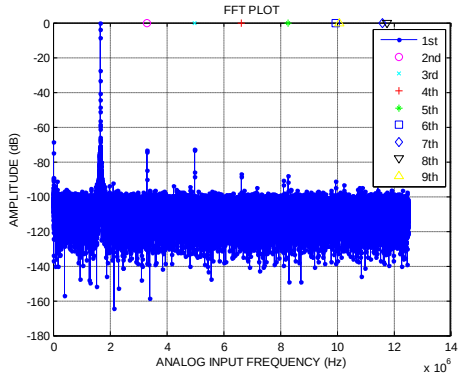
A high purity sine wave signal is feed to the ADCs with 25MHz sampling rate. The digital output data of the ADCs are captured and analyzed to obtain the electrical parameters such as SNR, ENOB, DNL, INL, etc.

Table 1: Electrical Characteristics Comparison of SOI-based ADC and bulk CMOS ADC

	SOI ADC	Bulk ADC
FS(Hz)	25M	
Freq_vin(Hz)	2M	
Supply（V）	5	
Consumption（mw）	240	
DNL(LSB)	±0.4	±0.4
INL(LSB)	±0.5	±0.5
SNR(dB)	60.5	59.6
SFDR(dB)	72.3	74.4
SINAD(dB)	60.2	59.2
ENOB(bits)	9.7	9.5



(a) SOI CMOS ADC



(b) Bulk CMOS ADC

Figure 8: Spectrums of SOI and bulk CMOS ADC with 25MHz sampling rate

The electrical characteristics experiment indicates both of SOI ADC and bulk ADC could achieve effective number of bits (ENOB) of 9.5bits, spurious-noise-free dynamic range (SFDR) of 72dB, differential nonlinearity (DNL) of 0.4LSB, and integral nonlinearity (INL) of 0.5LSB. The detailed performance characteristics are listed in Table 1. The spectrum analysis results of the SOI and bulk ADCs with 25MHz sampling rate are shown in Figure 8.

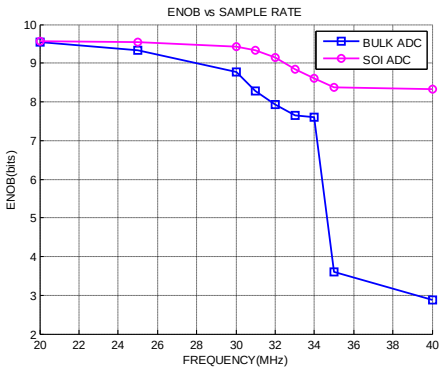


Figure 9: Comparison of the SOI and bulk based ADCs frequency characteristic

By changing the sample rate, the frequency characteristics of the ADCs are obtained. Test results show that the SOI ADC still maintains the ENOB of 8.2bits up to the 40MSps. The ENOB of the bulk ADC is lower than 8bits from 31MSps and only 2.5bits to 40MSps. The SOI technology exhibits better frequency characteristic because the SOI MOSFET has smaller parasitic capacitance and better I-V characteristic. The

comparison of the SOI and bulk based ADCs frequency characteristic is shown in Figure 9.

B. TID Experiment

The total ionizing dose (TID) experiment is performed by the Cobalt-60 gamma radiation source at Peking University.

The sample ADCs with different technologies are selected for the TID experiment. The samples are irradiated to 500krad(Si) with a dose rate of 50rad(Si)/s at the room temperature, and annealed 168 hours at 100℃ after last dosing [17]. During the experiment, samples are left static bias state, and measures are performed at pre-radiation, 50k, 100k, 150k, 300k, 500krad(Si) and after anneal.

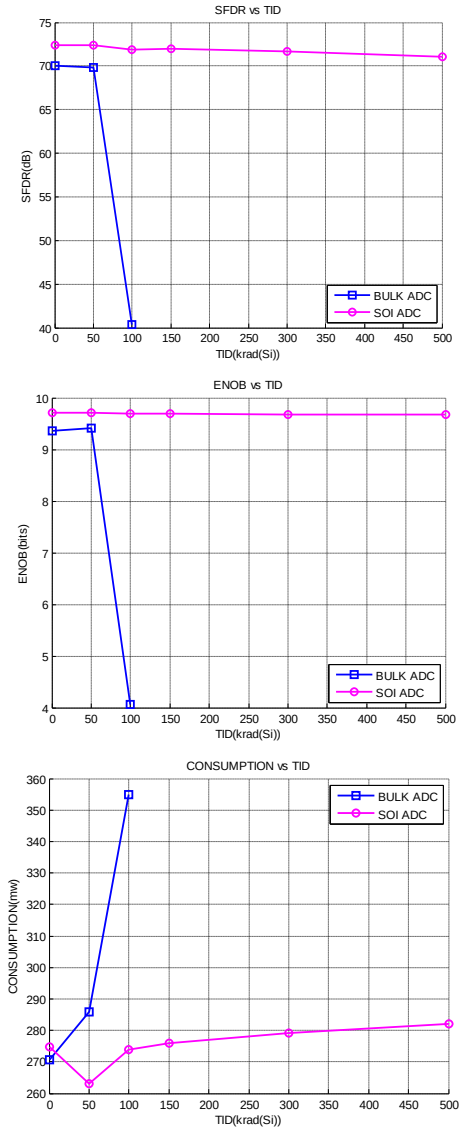


Figure 10: Comparison of TID responses between SOI and bulk CMOS ADC

The experimental results reveal that the SOI ADC maintains the consumption and spectral performances up to 500krad(Si), and the performances degradation are not observed after anneal. It achieves the TID tolerance of 300krad(Si) at least.

The bulk ADC performances with the identical circuit design and layout floor plan do not degrade until the radiation dose accumulation up to 50krad(Si). Drastic reductions are observed over 50krad(Si) , the ENOB of bulk ADC is only 4bits and the increasing of the consumption is over 25% at 100krad(Si). After annealing, the ENOB and the consumption of the bulk ADC both recover to meet all specifications.

Comparison of TID responses between the SOI and bulk CMOS ADCs is shown in Figure 10. It can be seen that the TID tolerance of SOI-based ADC is nearly one order of magnitude higher than bulk ADC. This is due to the radiation hardened techniques used in the SOI CMOS technology.

C. SEE Experiment

The single event effects (SEE) experiment is performed by the HI-13 tandem accelerator at the China Institute of Atomic Energy.

The sample ADCs with different technologies are selected for SEE test. At room temperature, all samples are irradiated by particles broad beams with stable DC analog input signals including -0.8V, 0V and 0.8V. The fluence is 1E7 /cm^2 with the 1E4 /cm^2• s flux. By monitoring the digital output and the consumption of the ADC, if the deviation of the digital output is more than ±4LSB from the expected value, or the consumption increases over 10% of the normal, the single event effect is confirmed [17].

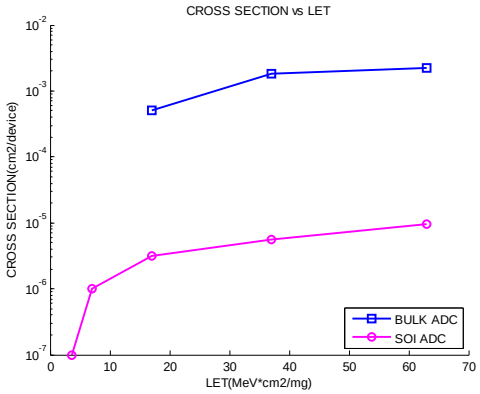


Figure 11: Comparison of SEU cross-section between SOI and bulk CMOS ADC

The experimental results indicate that neither ADC exhibits single event latch-up (SEL) and single event function interrupt (SEFI) sensitivity up to the maximum tested LET of 63MeV·cm^2/mg. This is due to the good nature of SEE insensitivity of SOI technology and the reasonable and rigorous layout rules of the bulk CMOS ADC.

The input voltage value does not have obviously effect on the device single event upset (SEU) sensitivity. At the LET of 17MeV·cm^2/mg, the SEU cross-section of the SOI-based ADC is about 3.1E-6cm^2/device, at the LET of 63MeV·cm^2/mg, the SEU cross-section of the SOI-based ADC is about 9.6E-6cm^2/device, both of the two points are lower than bulk ADC by two orders of magnitude. Due to implement the suitable RHBD approaches and take the inherent advantage of the rad-hard SOI technology, the SOI-

based ADC generates much smaller deviations when radiated. Because most deviations could be corrected by the pipelined ADC's digital error correction logic with the system redundancy, the SOI-based ADC acquires excellent rad-hard accomplishments. In contrast the bulk CMOS ADC with identical schematic design and layout floor plan could not be so efficient in SEE experiment. Figure 11 illustrates the differences of SEU cross-section between SOI and bulk CMOS ADCs.

VI. Conclusion

In conclusion, by implementing simple RHBD approaches and taking the inherent advantage of the rad-hard SOI technology, the SOI-based ADC achieves the TID tolerance of 300krad(Si) at least, nearly one order of magnitude higher than bulk ADC, and the SEU cross-section of 9.6E-6cm^2/device at 63MeV·cm^2/mg LET, lower than bulk ADC by two orders of magnitude, more suitable for harsh radiation environment applications.

VII. References

[1] D. Binder, E. C. Smith, A. B. Holman, "Satellite Anomalies from Galactic Cosmic Rays," IEEE Trans. Nucl. Sci., vol. 22, No. 6, pp. 2675-2680, Dec. 1975.

[2] R. L. Pease, "Total Ionizing Dose Effects in Bipolar Devices and Circuits," IEEE Trans. Nucl. Sci., vol. 50, No. 3, pp. 539-551, 2003.

[3] F. Baille, G. Borel,B. Commere, "A Multi MRad hardened 8 bit/20 MHz flash ADC," IEEE Trans. Nucl. Sci., vol. 39, no. 3, pp. 401-404, Jun. 1992.

[4] O. A. Kalashnikov, A. A. Demidov, "Integrating analog-to - digital converter radiation hardnesstest technique and results," IEEE Trans. Nucl. Sci., vol. 45, no. 6, pp. 2611-2615, Dec. 1998.

[5] A. L. Sternberg, L. W. Massengill, M. Hale, B. Blalock , "Single-Event Sensitivity and Hardening of a Pipelined Analog-to-Digital Converter", IEEE Trans. Nucl. Sci., vol. 53, no. 6, pp. 3532-3538, Dec. 2006.

[6] C. R. Grace, P. Denes, D. Gnani, H. von der Lippe, J. P. Walder, "Radiation-Tolerant Code-Density Calibration of Nyquist-Rate Analog-to-Digital Converters," IEEE Trans. Nucl. Sci., vol. 60, no. 2, pp. 1303-1310, Apr. 2013.

[7] G. Gasiot, V. Ferlet-Cavrois, P. Roche, " Comparison of the sensitivity to heavy ions of 0.25-µm bulk and SOI technologies," IEEE Trans. Nucl. Sci., vol. 49, No. 3, pp. 1450-1455, Jun. 2002.

[8] J. A. Babcock, P. Francis, C. Olgaard, J. A. Darmawan, "Comparison between Short Channel Bulk (Silicon) and Body-Tied Partially Depleted SOI nMOS for High Frequency Low Voltage Analog Circuit Design"IEEE Solid-State Device Research Conference, vol. 1, pp. 208-211, 1999.

[9] M. H. Han, C. Y. Chang, H. B. Chen, H. B. Chen, J. J. Wu, "Performance Comparison Between Bulk and SOI Junction less Transistors" IEEE Electron Device Letters, vol. 34, no. 2, pp. 169-171, Feb. 2013.

[10] A. V. Oliveira, P. G. D. Agopian, E. Simoen, "Comparison of analog performance between SOI and Bulk pFinFET," Microelectronics Technology and Devices (SBMicro), pp.1-4, 2014.

[11] Haitao Wang, Hui Hong, Lingling Sun, and Zhiping Yu, "A sample-and-hold circuit for 10-bit 100MS/s Pipelined ADC ," ASICON IEEE, pp. 480-483, Oct. 2011

[12] Andrew M. Abo and Paul R. Gray, "A 1.5-V, 10-bit,t14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," IEEE J. Solid-State Circuits, vol. 34, no. 5, pp. 599-606 May.1999

[13] Y. Yao, De sheng Ma, F. Dai, "A 12-bit interleaved opamp-sharing pipeline ADC for extreme environment application s," ICSICT IEEE, pp. 394-396 Nov. 2010

[14] K. Bult, G. J. G. M. Geelen, "A fast-settling CMOS opamp for SC circuits with 90-dB DCgain,"IEEE Journal of Solid-State Circuits, vol. 25, no. 6, pp. 1379-1384, Dec. 1990.

[15] Ru Huang, Guoyan Zhang, "Technologies and Applies of SOI CMOS," Beijing Science Press, Jan. 2005.

[16] Shicai Qin and Xiangluan Jia, "Electronics of Analog Integrated Circuits," Tianjin Science and Technology Press, Jan. 1996.

[17] "MIL-STD-883J_CHG-2", Mar. 2014.