SIPHRA 16-Channel Silicon Photomultiplier Readout ASIC

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Abstract

SIPHRA is an integrated circuit (IC) for the readout of photon detectors, such as photomultiplier tubes (PMTs), silicon photomultipliers (SiPMs), and multi-pixel photon counters (MPPCs). The IC has 16 input channels and one summing channel. Each channel can be used for pulse height spectroscopy and timing. The summing channel is important for the readout of detector arrays with monolithic scintillators. The programmable shaping time of 200 ns, 400 ns, 800 ns, or 1600 ns allows for pulse-height spectroscopy using scintillators with different light emission properties. The current mode input stage (CMIS) is designed for large negative charge (-16 nC, -8 nC, -4 nC, and -0.4 nC), depending on the programmable attenuation, and it accommodates large capacitive load (several nF) and large leakage current (up to -100 µA from dark counts). Alternatively, the CMIS can be by-passed to allow for positive charge depending on programmable gain (+40 pC, +4 pC, +0.4 pC). The IC contains one 12-bit analog-to-digital converter (ADC) that allows for digitization of the pulse-heights from all channels, including the summing channel at a sampling rate of 50 ksps. Every channel output is available for external use and provides either the analog or a digital trigger/timing pulse with fixed width or time-over-threshold. The programmable channel output facilitates many applications, such as external waveform sampling and digitization, pulse height and time spectroscopy, pulse counting, and triggering. The IC operates at 3.3-V supply voltage and dissipates about 15 mW without CMIS and 30 mW with CMIS active. To save power, any channel or function can be powered down. The ASIC has a serial peripheral interface (SPI) for programming its register settings and for slow ADC data readout; faster readout with up to 1 Mbit/s is possible via a serial data transmission line.

I. INTRODUCTION

A. ASIC Requirements and Applications

The requirements for the application specific integrated circuit (ASIC) requirements were derived from needs in Gamma-Ray Imaging, Polarimetry and Spectroscopy (GRIPS, [1]), scintillating fibers for a gamma-ray telescope (PANGU, [2]) and astro-particle missions (HERD, [3]). The circuit covers a wide range of detector technologies and applications in space and terrestrial, for example, high-resolution gamma-ray spectroscopy, detector front-end readout for diagnostic imaging in nuclear medicine, fast photon counting, and timing. The ASIC can be used with SiPMs and MPPCs, for example ref. [4]. Operation in space requires radiation tolerance and low power dissipation. Therefore, special design effort has been on latch-up immunity, single event upset mitigation and error corrections, as well as low-power design and programmable power-down.

B. Design Heritage

The SIPHRA is a design without predecessor. The circuit inherits a few functions and circuit elements from other IDEAS ASICs: buffers from IDE3466 [5], analog-to-digital converter (ADC) from NIRCA [6], and implementation with the radiation tolerant IDEAS ASIC physical and digital design kit. The ASIC was designed with the goal to provide a reliable solution for pulse height spectroscopy with arrays of silicon photomultipliers (SiPMs, e.g., [4]) and multi-pixel photon counters (MPPCs) and multi-anode photomultiplier tubes (MA-PMTs), and to support individual channel analog and digital output for analog waveform sampling, timing, triggering and counting.

C. Readout of SiPMs, MPPCs and PMTs.

Figure 1 shows the block diagram of SIPHRA connected to an array of 16 SiPMs. SIPHRA has 16 channels and one summing channel. Each channel processes the analog signal from the PMT/SiPM/MPPC and allows one to measure the charge (pulse heights), trigger time, and time-over-threshold.

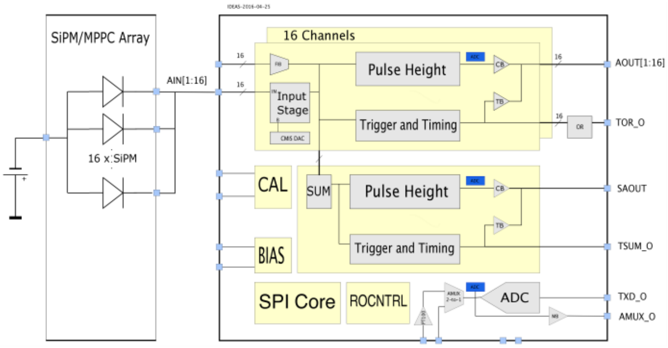

Figure 1: SiPM/MPPC array connected to SIPHRA IC.

II. ASIC Design Specifications

A. Overview

Table 1 summarizes the main features of the SIPHRA circuit, and Figure 3 gives the functional overview of the ASIC. SIPHRA has 16 input channels, one summing channel and one ADC. Every channel provides the functionality for analog pulse height spectroscopy and digital trigger timing pulse derived from pulse height discrimination. The trigger pulse initiates the digitization with the ADC and activates `TOR_O` and `TSUM_O`, to trigger the serial readout of digitized or analog pulse height (via `TXD_O`, and `AMUX_O`, respectively). The trigger pulse is programmable for fixed width or time-over-threshold. The outputs `AOUT[1:16]` can be programmed to provide the analog pulse height, the trigger timing pulses, or the time-over-threshold.

Table 1: SIPHRA features.

– 16 readout channels
16 current sensitive inputs (≤ 16 nC)
1 summing channel
– Programmable attenuation to handle charge up to
-16 nC, -8 nC, -4 nC, -400 pC at AIN inputs, or
+40 pC, +4 pC, +0.4 pC at FIN inputs
– Programmable shaping time
200 ns, 400 ns, 800 ns, 1600 ns
– 16 inputs (AIN) with programmable offset voltage
– Pulse height spectroscopy
16 shapers followed by track-and-hold
Programmable hold timing
12-bit analog and digital readout
3 ksps/channel max.
– Trigger generation
Internal from charge discriminator via programmable threshold in every channel
External (trigger on input, trigger on sum)
– Power
15 mW without CMIS, 30 mW with CMIS active
Flexible power down scheme of channels or functions
– SEL/SEU radiation hardened
– SPI Interface

B. Analog Channel and Trigger Circuit

1) Current-Mode Input Stage (CMIS)

Each channel has a current mode input stage (CMIS) with inputs `AIN1` to `AIN16`. The CMIS can be connected to the detector either directly (DC coupled, Figure 2) or coupled via a capacitor (AC coupled, not shown), although the CMIS is ideally suited for DC coupling to the detector. The CMIS has two main purposes: to downscale the detector current and to provide a stable input voltage at `AIN`. The input offset is programmable and sets the SiPM bias voltage. This allows one to control the charge released from SiPM and to compensate for the variation in breakdown voltage among several SiPMs.

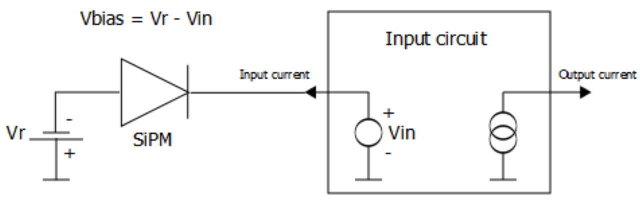

Figure 2: SiPM biasing principle.

Downscaling of the input current is required because the output current from PMTs, SiPMs and MPPCs is too large for on-chip current integration in a charge sensitive amplifier. The integrating capacitor would occupy an impractically large area on the chip. The CMIS is designed for large negative charge with programmable gain attenuation of 1/10, 1/100, 1/200, and 1/400, which causes charge saturation at -16 nC, -8 nC, -4 nC, and -0.4 nC, respectively. The inputs accommodate large capacitive load up to several nF, and large leakage current up to -100 µA from SiPM/MPPC dark counts. The input voltage is regulated to a stable bias voltage set via an 8-bit DAC over the range of 1 V. The CMIS also has a configurable bias current, 12 µA to 48 µA, which should be used if the SiPM has a very small dark current. The CMIS input impedance below 10 MHz is purely resistive between 5 Ohm and 30 Ohm depending on the bias current. Above 10 MHz, input impedance becomes reactive and peaks with a few 100 Ohm at 250 MHz. CMIS can be powered off and by-passed with the detectors connected to the inputs `FIN1` to `FIN16`. The `FIN` inputs allow for positive charge depending on programmable gain (+40 pC, +4 pC, +0.4 pC) in the current integrator.

2) Current Integrator (CI)

Each channel has one active current integrator (CI) with adjustable gain and an adjustable feedback device. The integrator input is fed from the output of the CMIS. If CMIS is powered down the input is taken directly from the `FIN` input pad. Figure 4 shows the block diagram of the CI. The CI integrates a current (positive charge) input, in first order to a voltage step of magnitude Q/C_{fb}, where C_{fb} is the feedback capacitor. The voltage step decays with a typically large time constant τ set to first order by $\tau = R_{fb} \times C_{fb}$, where R_{fb} is the feedback resistor. The CI has a programmable gain of 1V/30pC, 1V/27.75pC, 1V/3pC and 1V/0.75pC.

3) Shaper (SHA)

A pulse shaper (SHA) follows every current integrator. The shaper optimizes the signal to noise ratio (SNR). The shaper is programmable and can be by-passed. Each shaper has two analog inputs (one signal and one reference input) and one analog output. Figure 5 shows a block diagram of the shaper. The shaper has four different shaping times (nominally 200 ns, 400 ns, 800 ns and 1600 ns) that are programmable through a configuration register.

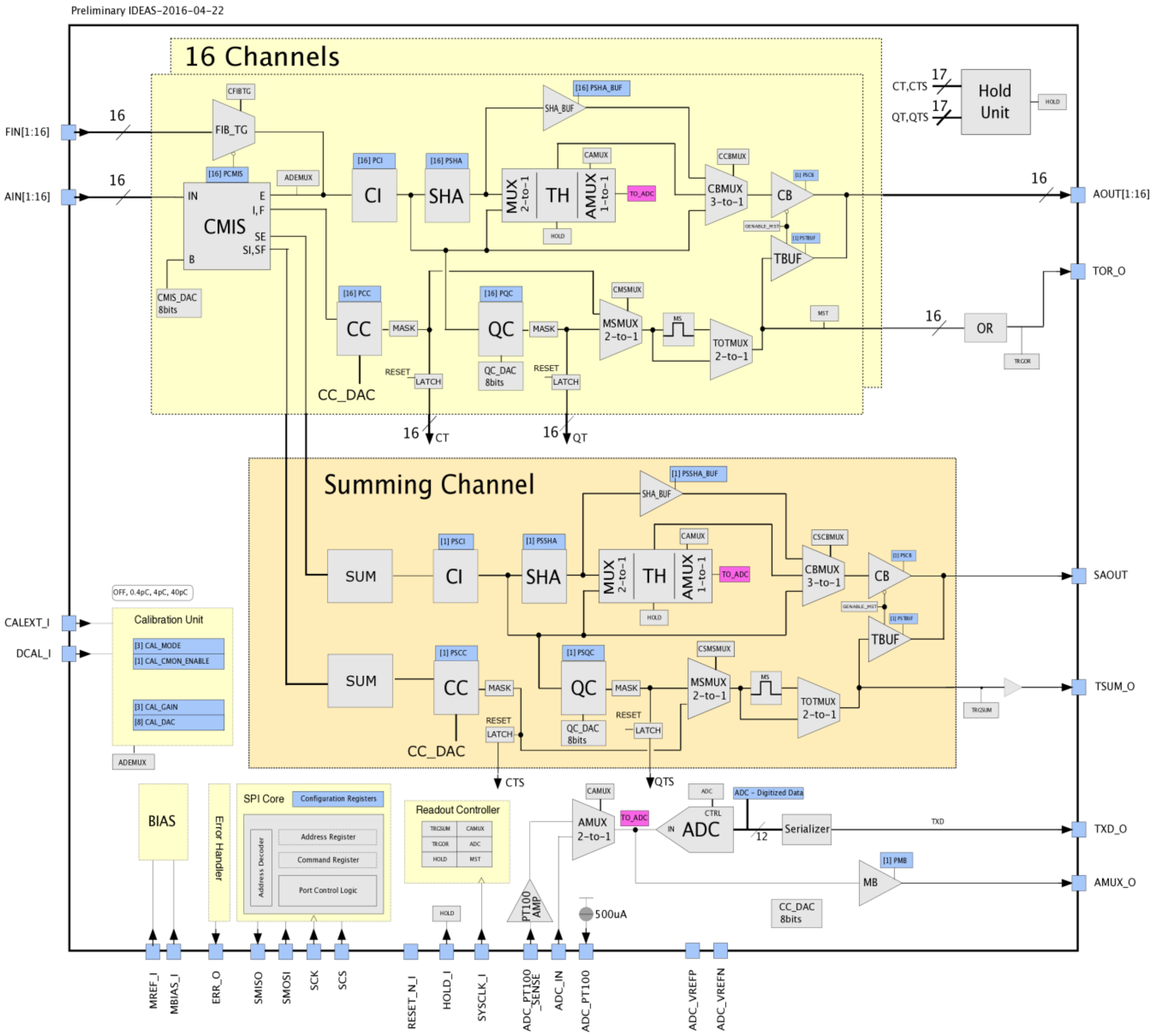

Figure 3: ASIC architectture overview.

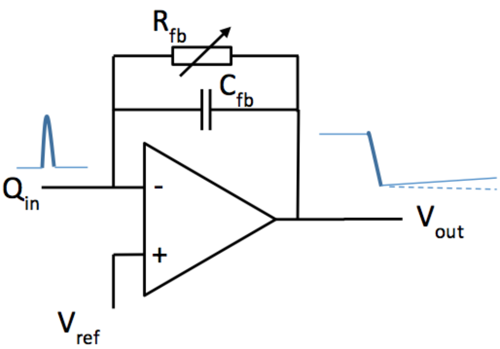

Figure 4: Current integrator block diagram.

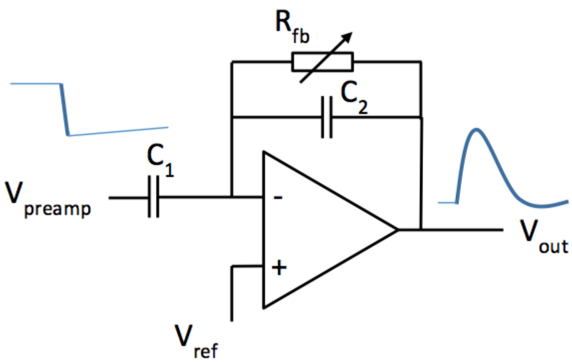

Figure 5: Shaper block diagram.

4) Pulse Height Spectrometer

The pulse height spectrometer consists of the current integrator (CI), the shaper (SHA), a track-and-hold unit (TH) and a channel output buffer (CB) capable of driving 10-pF external load. The TH circuit tracks the shaper output voltage waveform, and stops tracking and holds the signal when HOLD is asserted. The HOLD can be triggered from internal QC or CC or externally at HOLD_I. The held value remains constant with minimal distortion from voltage dependent charge injection and droop. The hold delay is programmable with respect to the trigger in the range typically from 69 ns to 4.7 µs. One can program the ASIC registers to provide the signals from the current integrators, or the shapers or the track-and-hold units at AOUT[1:16]. The output of the TH unit can be multiplexed (AMUX) to a 12-bit successive-approximation register (SAR) ADC. The ADC digitizes the signals from any or all 16 channels, as well as the summing channel and two externally applied input voltages (ADC_PT100_SENSE and ADC_IN), at a rate of 50 ksps. The digitized data is serialized and sent out at TXD_O. The multiplexed pulse heights are also available at AMUX_O for optional readout and digitization with an external ADC. This single-ended analog output is compatible with an external capacitive load of 40 pF.

5) Trigger Timing and Trigger Readout and Time-over-Threshold

The trigger timing pulse is generated in a charge comparator (QC) and in a faster current comparator (CC). The purpose of the comparator is: 1) to generate the internal HOLD signal for the track-and-hold and initiate the digitization in the ADC, 2) to generate a timing trigger pulse for the logic OR to indicate an event to the system, and 3) to provide a time-over-threshold (TOC) at AOUT[1:16] where TOC is related to the input charge. The QC compares the pulse height with an 8-bit programmable reference (charge threshold, individual for every channel) and triggers when the pulse height exceeds the charge threshold. The QC also incorporates programmable hysteresis to avoid retriggering from noise. The CC compares the current from the CMIS with a reference current which is generated by an 8-bit programmable current reference (global for all 16+1 channels). The purpose of the CC is to reduce time walk by providing an early trigger when a charge event occurs on the input of the channel. The programmable ASIC register allows one to enable or disable the triggering from individual channels. The mono-stable outputs of all 16 channels are connected to a trigger OR which outputs a logical OR from triggers in any of the channels (TOR_O).

6) Summing Channel

The summing channel consists of a differential summing integrator that integrates the sum of the currents of the CMIS outputs from all 16 channels and provides the same pulse height spectrometer and trigger/timing unit like any of the other channels. The summing channel allows one to trigger the readout based on the summed signals from all channels.

C. Floor Plan, Pads and Signals

Figure 6 shows the ASIC floor plan, with pad frame and signals.

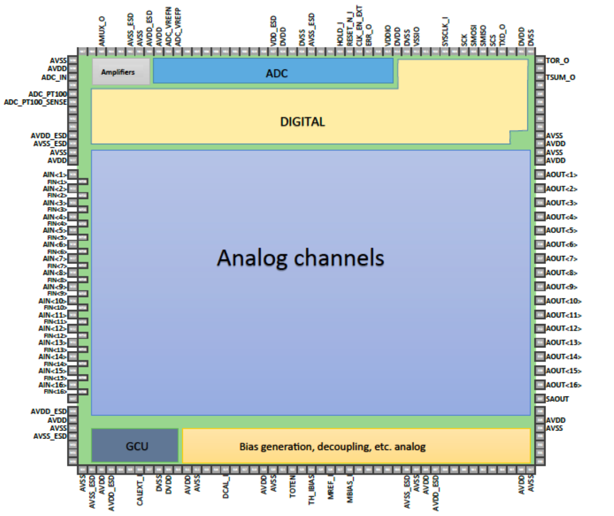

Figure 6: ASIC signals and chip pad frame.

At the center there are the analog channels with the input signals on the left side and output signals on the opposite side. The channels receive bias currents from the bias generation network, which generates all internal bias currents and voltages from one external reference bias current (MBIAS_I). The gain calibration unit (GCU) is near the inputs and allows one to inject calibrated charges up to 50 pC into any CI and measure the gain. The ASIC has a digital part with the serial peripheral interface (SPI), the readout controller, and the serial data interface. The readout controller generates the internal digital signals for the readout and digitization of the pulse heights.

III. ASIC Layout

Figure 7 shows the top-level layout of the chip. The active area is 7.6 mm × 6.8 mm. The SIPHRA has been designed in 0.35 µm CMOS and will be manufactured at AMS. All amplifier inputs are protected by diodes against over-voltage and electro-static discharge (ESD).

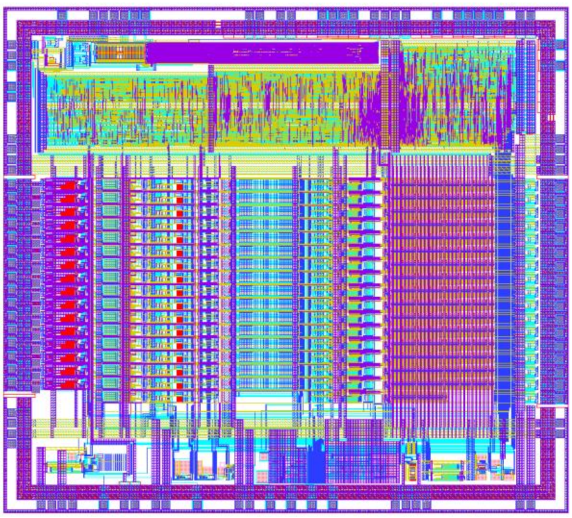

Figure 7: Top-level layout.

IV. ASIC Design Verification

We have performed ASIC design and verification using Spectre/HSPICE, Assura DRC and LVS, QRC for parasitic extraction, ModelSim for functional simulation and coverage, Encounter for digital implementation and RTL Compiler for synthesis and connectivity verification from digital to analog. We have verified the combined analog and digital circuit as follows:

1. Waveforms from the digital circuit simulation in ModelSim were used as input to analog simulations in Spectre/HSPICE.
2. We performed post-layout simulation on a fully extracted channel and analysis on the top-level analog part of the chip.
3. Top-level physical verification used the combined analog and digital circuit and performs layout versus schematics (LVS) and design rule checks (DRC) with Assura.

We have completed the design and verification and we have submitted the GDSII files to the foundry. The simulations were performed with SiPM directly coupled to the CMIS input. The SiPM model assumes 3.4-nF capacitance and 10-µA leakage current from pixel dark counts. The following are important outcomes of the design verification.

1) Power Dissipation

The total power dissipation is about 30 mW, corresponding to 1.87 mW/channel on average. The analog circuit power dominates, while power from the digital circuit is negligible. The CMIS contributes with about 15 mW, and, if the application permits, CMIS can be powered off, leaving a total power of about 15 mW.

2) Pulse Shaping

Figure 8 shows the simulated waveforms at the output of the CI and the shaper for different shaping time setting and the same negative charge injected into the CMIS input. The CI pulse rises when the negative charge is injected into the CMIS input (arbitrarily chosen at 5 µs). The shaped pulses peak after about 300 ns, 500 ns, 900 ns, and 1650 ns, which is only slightly longer than the nominal shaping time settings. The difference between shaping and peaking time is because of the 200-ns rise time of the CI output.

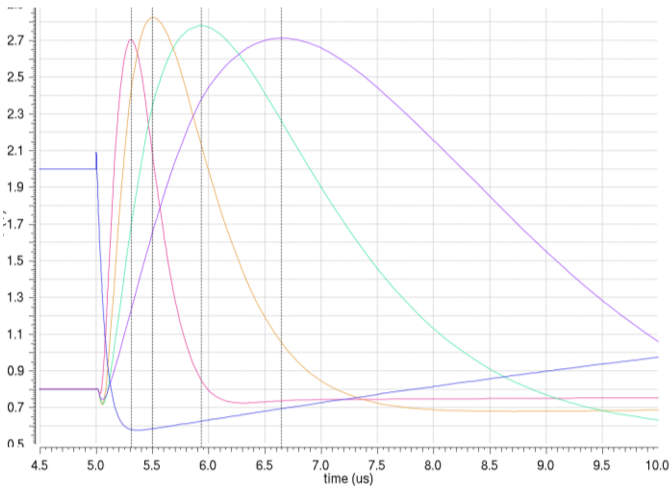

Figure 8: CI and shaper outputs at different shaper settings.

3) Input Charge Range, Noise and Dynamic Range

Figure 9 shows the simulated shaped signal at `AOUT` for different negative charges injected into CMIS. For the 6 charges shown (-3.9 nC, -7.75 nC, -11.6 nC, -15.5 nC, -19.4 nC, -23.3 nC), the semi-Gaussian pulses peak 500 ns after charge injection. The pulse shape for -23.3 nC distorts as the output voltage approaches the supply voltage of 3.3 V.

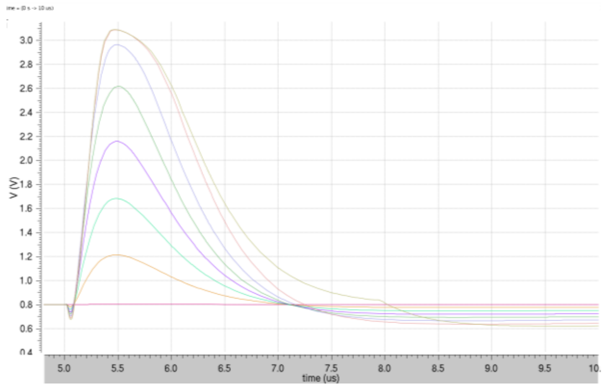

Figure 9: Shaped signal at AOUT for different negative charges at CMIS input.

Figure 10 shows the simulated peak values versus negative charge for the different attenuation settings and at 500-ns peaking time. The peak values increase linearly and saturate at different charges depending on the attenuation. We define the saturation charge as the charge where the pulse height reaches 90% of the supply voltage, i.e. 2.97 V. Table 2 summarizes the simulation results. One can see that the saturation charge increases, as expected, by factor 10 as the attenuation is changed from 1/10 to 1/100, and by factor 2 as the attenuation is changed from 1/100 to 1/200 and to 1/400. Table 2 also lists the simulated equivalent noise charge (ENC). This simulation was done with the SiPM directly coupled to the CMIS input. The noise increases by factor 2 as the attenuation decreases by factor 2. However, the noise at attenuation 1/10 is larger than one would expect by scaling of the attenuation. The dynamic range, defined as the ratio of the absolute saturation charge and the equivalent noise charge, is between 6000 and 8228 for the 3 largest CMIS attenuation settings. The dynamic range corresponds to almost 13-bit resolution, and thereby exceeds the 12-bit on-chip ADC resolution.

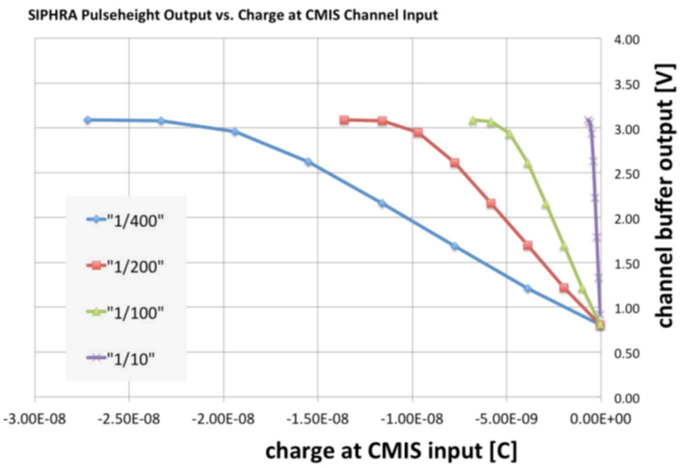

Figure 10: Charge range for different CMIS settings.

Table 2: Simulation results: saturation charge, equivalent noise charge (ENC) and dynamic range.

CMIS gain	Shaping time [ns]	Saturation charge [pC]	ENC [pC]	Dynamic range
1/10	200	-510	0.24	2125
	400		0.28	1821
	800		0.28	1821
	1600		0.28	1821
1/100	200	-4980	0.83	6000
	400		0.73	6822
	800		0.67	7433
	1600		0.63	7904
1/200	200	-9830	1.62	6068
	400		1.40	7021
	800		1.28	7680
	1600		1.18	8331
1/400	200	-19500	3.27	5963
	400		2.80	6964
	800		2.56	7617
	1600		2.37	8228

4) Readout Trigger Threshold Range

Table 3 shows the trigger threshold charge range from the absolute minimum to maximum value for the CMIS gain settings, simulated with the default SiPM at the CMIS input. One can see that the threshold range covers the entire charge range that can be read out for pulse height spectroscopy.

Table 3: Trigger threshold range.

CMIS gain attenuation	Trigger threshold charge range	
	Minimum [pC]	Maximum [pC]
1/10	-4	-560
1/100	-43	-5400
1/200	-87	-10800
1/400	-175	-20900

5) Readout Cycle

Figure 11 shows the signals that are important for the SiPM readout: the current pulse is injected at `AIN`[1], the current integrator output rises, and the shaped pulse appears at the shaper output. The hold signal is automatically generated, and the pulse height appears at `AOUT`[1]. The charge trigger, QT[1], activates and a trigger pulse appears at the trigger-OR output, TOR_O. The channel multiplexer, CAMUX, and the ADC clock are activated internally. The internal clock is synchronous with the externally applied clock (not shown). About 22 clock cycles after internal HOLD was activated, the ADC data becomes available at `TXD_O` (not shown). The readout ends with an internal reset.

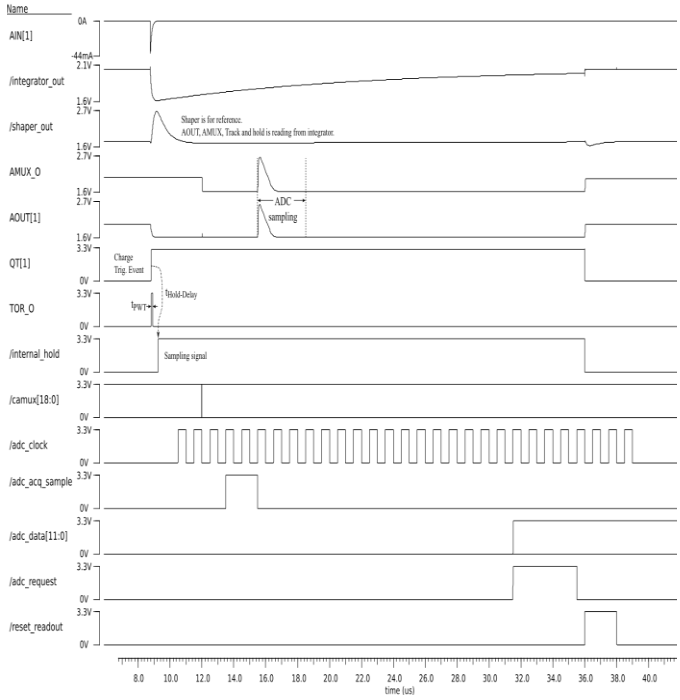

Figure 11: Simulation of signals in the channel.

V. ASIC Tests and Design Validation

Figure 12 shows the block diagram of the SIPHRA ASIC design validation system. The test system is based on the Xilinx Zync-7000 system-on-chip and custom-made firmware for the SIPHRA ASIC readout and control. The system is controlled via Ethernet from a standard computer. The SIPHRA ASIC is located on the ROIC test board, which allows one to connect to the detector array via standard SMA connectors or pin-rows. The test software is programmed in National Instruments LabView.

Preliminary design validation results are available from test devices: We have manufactured test devices with the ADC, SPI, registers and buffers, and have tested these design with respect to radiation. We measured a single-event-upset threshold of 50 MeVcm^2/mg and we do not observe any latch-up up to the maximum tested energy of 135 MeVcm^2/mg [7].

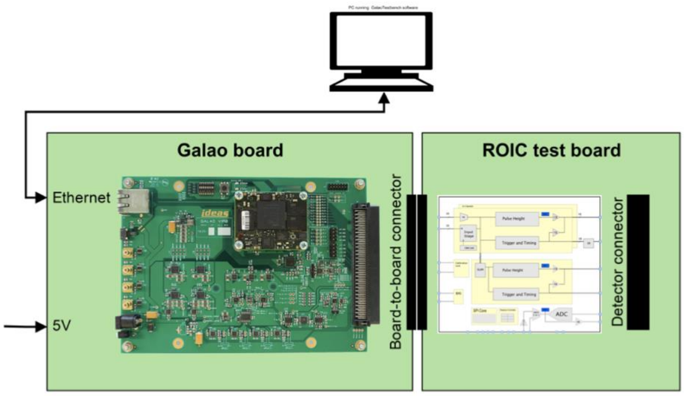

Figure 12: Block diagram of the ASIC design validation and test system.

VI. Summary

We have designed an integrated circuit (IC) for the readout of photomultiplier tubes (PMTs), silicon photomultipliers (SiPMs), and multi-pixel photon counters (MPPCs). The IC has 16 input channels and one summing channel. Each channel can be used for pulse height spectroscopy and timing. The current mode input stage is designed for large negative charge depending on the programmable attenuation and accommodates large capacitive load and large leakage current. Each channel has one output that can be programmed to provide either the analog signal from the current integrator, the shaper, or the digital trigger pulse, or time-over-threshold. The channel output allows one to test many features for further developments of the circuit. SIPHRA has a built-in ADC that automatically digitizes the pulse height and outputs serial digital data. The SIPHRA design will be manufactured in Q2 2016, and samples will be available in Q4 2016.

VII. Acknowledgements

We would like to acknowledge the support from the European Space Agency (ESA contract number 4000113026), the Norwegian Space Center (contract number BAS.05.14.1), and the University of Geneva.

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