Approval Process of an ESCC Qualified ASIC Supply Chain based on a Mixed-Signal IP Library

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Abstract

A fast and reliable development of a RadHard Space product benefits from a dynamic and efficient way of an ASIC design and supply chain. Design and qualification of a new ASIC is associated with a long development phase. Using an ESCC qualified supply chain with an IP library can reduce the development time to a space qualified product significantly and lowers the costs and risks of the product. This supply chain resolves the trade-off between a full custom design with all associated qualification steps and a semi optimized product based on standard ICs.
IMST and TESAT Spacecom are currently working in a DLR funded R&D project to built up such an ASIC supply chain that will be offered by IMST after approval by ESCC consortium. Completion of this project is planned for Q1 2017.
A first publication of this ASIC supply chain establishment has been given on the AMICSA 2014 in CERN [1].
In this paper an update will be given on the current status of this project with measurement results including TID and SEE evaluation. The designed library elements will be presented and an overview of the supply chain will be given with all supported technology features, package choices and the design flow information.

I. Preface

Prior to this funded project a technology evaluation phase has been initiated by TESAT Spacecom to validate the suitability of the XFAB's XH018 process for the intended RadHard ASIC supply chain. TID tests and SEE tests have been performed on digital cells and single transistors to prove it. In the current project two ICs have been designed: "spac2_eval" as the initial chip to test the principle suitability of the semiconductor process and the designed IP blocks and a second IC with additional IPs and redesigned IPs as the test device for the evaluation test program, called spac3_eval. The evaluation test program is currently running according to the ESCC specification 2269000 and first results are available. After this evaluation test a third IC will be designed as a MS-ASIC for the qualification according to the capability domain and manufactured as described in the process identification document (PID) IMST proposed for the ASIC supply chain. This supply chain begins with a certain specification of the ASIC, which will be commonly agreed between customer and IMST and finishes with the delivery of a space qualified ASIC with its accompanying documents. The involved steps of the supply chain are further described in chapter V.

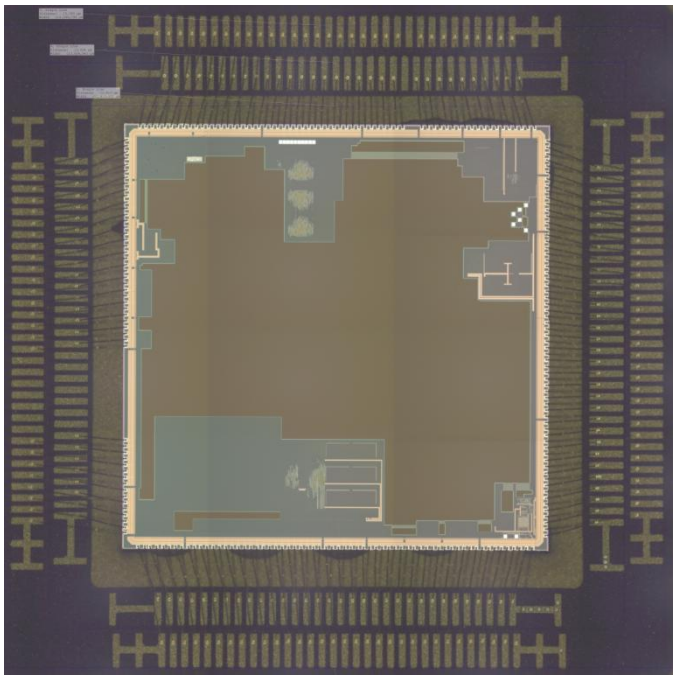

Figure 1: Photo of the bonded test chip "spac3_eval"

II. HARD Library Elements

The radiation hardened library designed by IMST, called HARD Library (HARD= Hard Against Radiation Design) supports I/O cells for 3.3 V and 5 V supply as well as level shifter I/Os for a negative supply voltage of -5 V on the ASIC. The other IPs are specified with the intention to cover a wide range of applications. The IP library contains data converters, biasing cells, memory modules, a reconfigurable opamp, LVDS driver and receiver, a SPI interface, OTP cells, a clk PLL, oscillators and special I/Os with cold spare functionality.
Different radiation hardening techniques have been implemented in the IP circuits to mitigate SEE and TID effects.

The following list gives an overview of the library elements with their key features:

IP Block	Main Characteristics
4-Wire SPI Interface	1.8V, extendible register bank with 8 register and 16 bit, each. Refresh logic for SEE mitigation implemented
I/O Cells	3.3V & 5.0V digital + Analog I/O, TMR In/Out
LVDS Driver	1.8V, Fmax=622 MHz
LVDS Receiver	1.8V and 3.3V, Fmax=622 MHz
Reconfigurable Multifunctional Operational Amplifier	•Inverting OpAmp with variable gain: -10 dB … +30 dB; 1dB step size •Non inverting OpAmp with variable gain: -10 dB … +30 dB; 1dB step size •LPF; 3 different cut off frequencies •I/U Converter with different input ranges •Schmitt Trigger with adjustable hysteresis •Voltage buffer •Open Loop configuration
Bandgaps	1.8V & 3.3V trimable
Reference Bias Generators	1.8V & 3.3V with PtoPR and constant currents & adjustable voltage references
Temperature sensor	1.8V, temperature range from -40°C…+150°C
POR Generator	POR delay: 5µs
LDO	Input voltage: 3.3V Output Voltage: 1.8V with adjustable short protection, 150mA I max
Level shifter High-Low	input signals with 0V…1.8V output signals with -5V…-3.2V
Level shifter Low-High	input signals with -5V…-3.2V output signals with 0V…1.8V
Digital Level shifter High-Low	3.3V-1.8V
Digital Level shifter Low- High	1.8V - 3.3V
16bit MUX	Max. signal frequency: 800 MHz
12 bit ADC	charge-scaling SAR ADC fast mode: 200 KS/s
Memory cell	2k x32 bit RAM module Clock frequency: 50 MHz.
12 bit DAC	segmented current steering DAC
Memory cell	64 bit OTP
Serializer / Deserializer	Data Rates: 600 Mbps with a reference clock Power: <500 mW
Clock PLL	16 bit 2nd order SDM fractional-N divider period jitter: 50ps (PK-PK)
DCXO	Supports 5 MHz … 50 MHz crystals
VCO with frequency divider bank	VCO frequency from 80 MHz – 600 MHz Divider bank ration from 1 to 128
CQFP package family	•Pin count: 256, 208, 132, 64 and 32 •100 Ω differential ports for LVDS interfaces •Die size from 2.2 mm^2 up to 100 mm^2

Table 1: Summary of the HARD library elements

III. Evaluation Tests

A. Test Chip & Electrical Measurements

A test chip spac3_eval containing all IPs as single blocks with their own individual supply pads has been designed and packaged in a 256 pin CQFP package. It is the largest defined package within the capability domain. The largest specified die size of 10 x 10 mm^2 has been chosen in order to have the worst case combination in terms of mechanical reliability like shock and vibration tests as specified in the evaluation test program. The picture of the bonded die is presented in Figure 1.

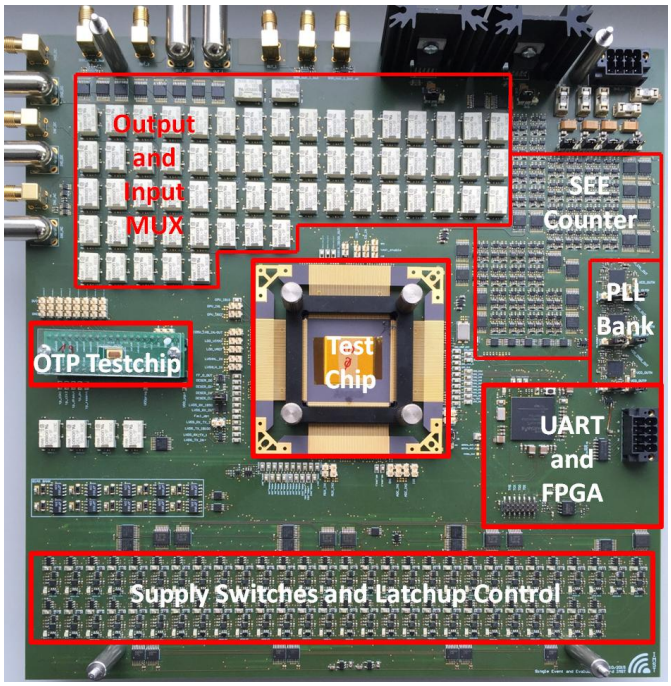

Figure 2: Evaluation board and SEE test board for the "spac3_eval" chip

Figure 2 shows the PCB used for electrical verification and SEE tests. It consists of different sections: the test chip mounted with a socket in the middle of the board and a further test chip containing the OTP test structure left of it. All signal input and output ports of the test chip are routed via relays to the SMA and BNC test connectors. The individual supply pins of the IPs are monitored against over current and latchup effects in the lower part of the PCB. For the single event transient tests a bank of comparators and counters with shift registers are used. SEE tested clock signals like DCXO, VCO or PLL are routed to external PLLs as reference clocks. The tuning voltage of the VCO from the external PLL and the lock detect signal is monitored during irradiation with heavy ions to detect any phase or frequency shift affected by the hits. A FPGA is the interface between the PCB and the PC. The evaluation board can be controlled by a programmed GUI.

B. SEE test

The SEE test for the shown test chip in Figure 2 will be performed in July 2016. Nevertheless the previous chip spac2_eval has been tested for SET, SEL and SEU at the CYCLONE110 facility in the Cyclon Resource Centre Louvain-la-Neuve. The test was performed based on the ESCC 25100 Specification (AD1), Single Event Effects Test Method and Guidelines.

The test PCB and test strategy is comparable to the current board shown in Figure 2. All IP blocks are enabled during the Single Event Effect test and were tested in the same way. All analogue circuit outputs are monitored by comparators to count all events over and under a specified and controlled threshold voltage. The counters have two comparators, one for -Vref and one for +Vref. Each time the signal passes over ±Vref a SET event is counted. Additionally all outputs are routed sequentially one after another to the oscilloscope for a specified time. If during this time a Single Event takes place,

Test	Ion M/Q=5	Energ. (MeV)	∢	Range (µm)	LET(MeV/ mg/cm^2)	Temp [°C]
1	^{20}Ne $^{4+}$	78	0	45	6.4	20
2	^{40}Ar $^{8+}$	151	0	40	15.9	20
3	^{84}Kr $^{17+}$	305	0	39	40.4	20
4	^{124}Xe $^{25+}$	420	0	37	67.7	20
5	^{125}Xe $^{25+}$	420	40	28.34	88.4	20
6	^{125}Xe $^{25+}$	420	40	28.34	88.4	125

Table 1: SEE Test conditions

the oscilloscope is triggered in single shot mode and a screenshot is stored in order to verify the SET amplitude and frequency of the ringing. At the end of the test every analogue output pin has been monitored by the oscilloscope for a certain time.

The Latch-up protection circuitry was designed for each power supply and test device. The Latch-up current limits were tuned individually for each circuit block to trigger for a supply current larger than 1.5 times the typical current.

Digital circuits like the RAM module and SPI controller are tested for SEU and SEL, only.

Table 1 shows the test conditions for the SEE test.

Representative results are shown for the 1.8 V bandgap circuit exemplarily in Figure 3 and Figure 4. Figure 3 shows the cross section of the counted hits while Figure 4 shows a screen shot of the transient plot for a hit with an Argon ion. Noticeable is the falling cross section between 67.7 MeV and 88.41 MeV. The reason is a detected SEU problem in the digital input pad of the chip control block leading to unintended interruptions of the SET measurement. Consequently the counter values are not reliable for the higher energy ions. The SEU problem has been resolved in a redesign and its effectiveness need to be proven in the upcoming SEE test. In a redesign of the bandgap, a topology has been implemented for a faster recovery of SETs and RC filters on sensitive nodes are added to further reduce the SET sensitivity. These modifications will be verified in the upcoming SEE test.

No SELs were detected in the measurement campaign.

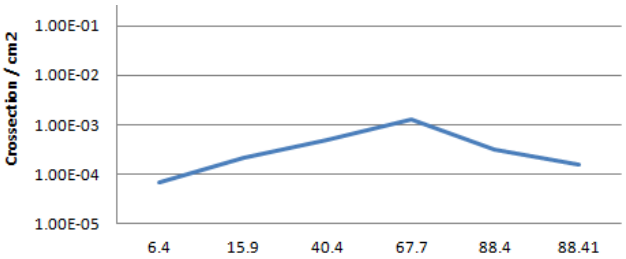

Figure 3: Cross section of the 1.8 V Bandgap vs. LETs at 25°C and 88.41 MeV*cm^2/mg at 125°C (last point)

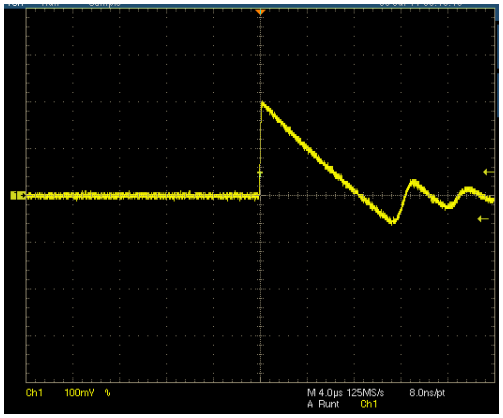

Figure 4: SET measured on the Bandgap output for a hit with an Argon ion

C. *TID test*

The TID test has been done according to the ESCC Basic Specification No. 22900 in the facility of ESTEC in Noordwijk. Figure 5 shows the irradiation board in front of the Co60 Gamma ray source. In Table 3 the radiation test plan is listed with the irradiation steps for the electrical measurements. Two initial measurements are done before irradiation has been started: 0_1 and 0_2.

LET (MeV/mg/cm^2)	hits
6.4	9
15.9	17
40.4	61
67.7	76
88.4	31
88.41	10

Table 2: Detected SET events

Total Dose [krad] (Si)	Dose Rate [krad/hrs] (Si)
0_1	0
0_2	0
9	0.275
33	0.275
104	0.275
200	3.3
300	3.3
24h annealing	0
192 h annealing	0

Table 3: Tested TID steps

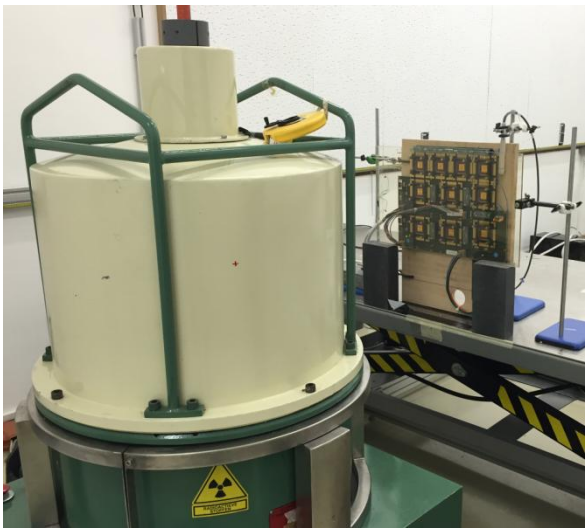

Figure 5: TID test board in the facility of ESTEC

First results with representative effects are shown here. A detailed documentation and evaluation of all results is ongoing at this time. The full documentation will be available after finishing the project.

The 1.8 V bandgap design show no significant effect on the irradiation neither on the output voltage, nor on the current consumption as shown in Figure 6. The variation of ± 0.25 mV is not correlated to the irradiation steps and can be explained with the measurement inaccuracy. According to the specified ± 2 mV variation over PVT, the TID variation is negligible. However, the 3.3 V bandgap shows a voltage drop versus total dose with a simultaneous current enhancement (Figure 7). Both parameters are falling back to the initial value after annealing. The variation vs. TID is with 8 mV larger as the specified ± 2 mV. A comparison of both designs show the advantage of the thinner gate oxide for the 1.8 V transistors compared to the 3.3 V transistors [2].

Another measured parameter is the resistance of a 3.3 V transmission gate. Shown is the resistance at a drain-source bias of 700 mV, where the NMOS and PMOS transistors are both contributing to the on-resistance. The resistance value drops versus total dose and goes back to the initial value after annealing (Figure 8).

In the previous test chip the ADC shows a drop of the output values for higher input voltages at higher TID levels (Figure 9, old version). The reason was supposed to be a leak of the small charge that is kept on the capacitors during the data conversion. In a redesign the leakage current effects have been improved and the new results showing the elimination of this effect.

The forecast of the final TID test summary is that the performance degradation due to ionising dose is very low for 1.8 V designs and has some effects on the 3.3 V designs. Circuits with low power consumptions can still suffer on the low remaining leakage of the 1.8 V transistors vs. TID as shown on the initial version of the ADC (Figure 9). But these effects can be handled by suitable mitigation techniques.

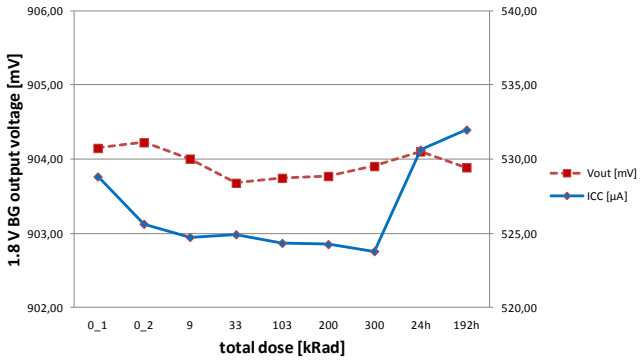

Figure 6: 1.8V Bandgap output voltage (dotted) and current (solid)

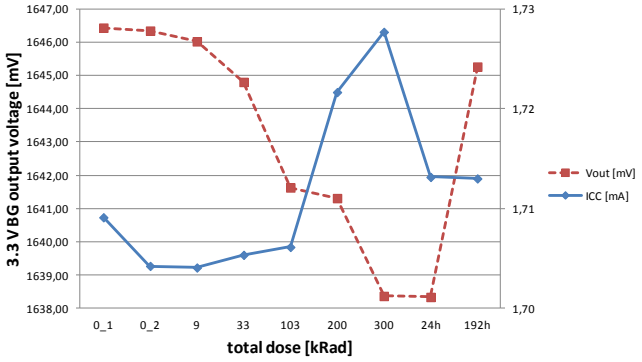

Figure 7: 3.3 V Bandgap output voltage (dotted) and current (solid)

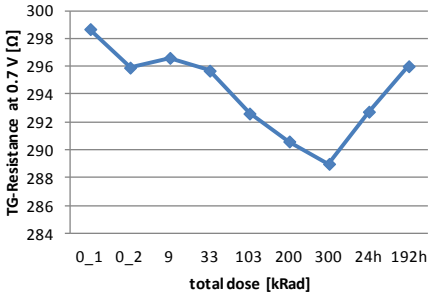

Figure 8: Transmission gate resistance

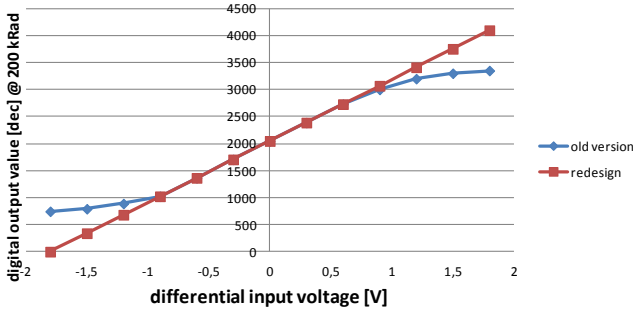

Figure 9: ADC old version vs. improved version

D. Mechanical tests

Aside from the electrical and radiation tests a set of mechanical tests are described in the ESCC 2269000 for the evaluation test program. Currently the assembly of the defined number of devices is ongoing together with the dimension, die shear and bond pull checks. Next steps are sealing the devices and continue with mechanical tests within this year. Since the test campaign is ongoing, no results can be reported up to now.

IV. ASIC SUPPLY CHAIN AND DESIGN FLOW

Two main design flows are targeted: One is a turn-key design by IMST based on customer requirements, while the other flow assists a co-design with the customer where the customer is allowed to provide encrypted VHDL codes. In the latter case IMST is creating the netlist with selected digital standard cells and implements TMR structures and scan chains in order to guarantee a RadHard design with test functionality. Analog features are handled by IMST using the IP library. On either case IMST delivers a tested, qualified and assembled RadHard ASIC.

A ceramic quad lead frame package family has been developed for the supply chain with different pin counts from 32 up to 256, supporting die sizes from 1.5 X 1.5 mm^2 for the smallest package up to 10 X 10 mm^2 for the largest package.

Figure 10 shows the involved steps for the ASIC supply chain, starting with ASIC specification, followed by the design and layout. After the layout, the production steps and test steps are shown.

For the quality assurance, the design and test phase will be followed by the "Space product assurance - ASIC and FPGA development" described in the ECSS-Q-ST-60-02C.

V. CONCLUSION

In this paper the current status and results are given on the DLR funded project 50 PS 1401 that has the aim to get the approval on an ESCC qualified ASIC supply chain. For this supply chain an IP library has been designed and first test results are presented. With this supply chain IMST will become a provider for qualified RadHard ASICs.

VI. REFERENCES

[1] ESA Requirements and Standards Division. Space engineering, product assurance. Techniques for Radiation effects. Mitigation in ASICs and FPGAs. 2009 © ESA for the members of ECSS

[2] J. Steinkamp, F. Henkel, V. Lück. 180nm CMOS Mixed-Signal Radiation Hard Library as base for a full ASIC supply chain. AMICSA 2014

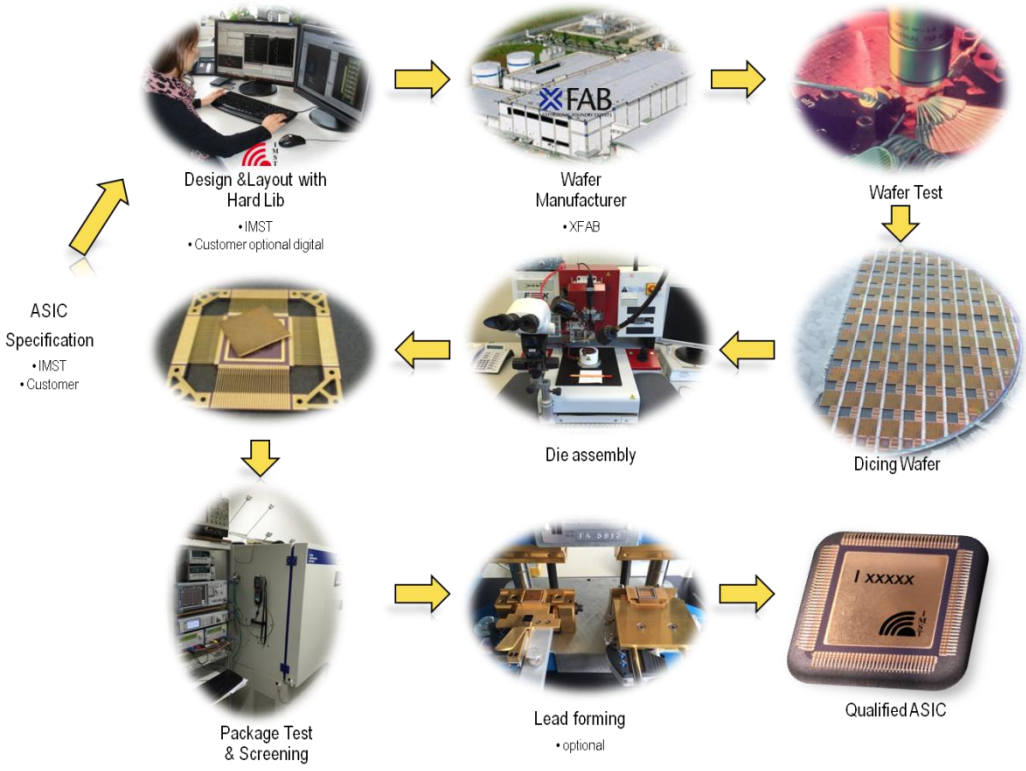

Figure 10: ASIC supply chain