Incorporating More In-Depth Radiation Knowledge in the DARE180U Analog Design Kit

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Abstract

DARE180U is a radiation hardened system-on-a-chip (SoC) design platform including mixed-signal and full-custom analog circuits. It is built on the commercial UMC L180 MM/RF 1.8V/3.3V, Single Poly 6 Metal (1P6M), P-Sub/Twin-Well CMOS technology. DARE180U is a member of the DARE family of radiation hardened full-custom/mixed-signal design platforms with a portfolio that extends over several technologies. In order to facilitate mixed-signal/full-custom radiation aware analog design an analog design kit (ADK) is provided to the designer as an extension of the foundry provided PDK.
Over the years, radiation related knowledge has been extended and built up with design of and testing on test vehicles, prototypes and flight models. Based hereon, improvements have been made to the DARE180U ADK to reduce design effort in order to fulfill the radiation hardness specifications. In this paper an overview is given of these improvements together with the continuous learning on which they are based.

I. The DARE180U Mixed-Signal/Full-Custom Radiation Hardened ASIC Technology

DARE (Design Against Radiation Effects) is a family of radiation hardened full-custom/mixed-signal design platforms. With the focus on mixed-signal and full-custom ASIC development it allows the use of an IP-based SoC implementation flow where digital parts are combined with reusable mixed-signal IP-blocks and dedicated full custom designed blocks. It also supports full-custom analog-on-top ASICs. First work has already been done end of last century on UMC L180 MM/RF 1.8V/3.3V, Single Poly 6 Metal (1P6M), P-Sub/Twin-Well CMOS technology and is still continuing today under the DARE180U name. No end is in sight as the 0.18µm technology is a long running analog node. Due to the flexible set-up of the platform other technologies can be supported to fulfill specific requirements. So later-on also the companion UMC 0.18µm CMOS Image Sensor (CIS) technology (DARE180UC) was supported, the 0.18µm XH018 XFAB tech (DARE180X) with support for high-voltage BCD devices up to 40V and non-volatile memory and the 0.35µm On-Semi I3T80 with high-voltage BCD devices up to 80V. Currently DARE65T based on 65nm TSMC technology is started. This in order to be able to provide higher compute power at lower power consumption together with higher frequency analog performance. A more in-depth historical overview and discussion of the different technologies and an overview of the ASICs produced can be found on the latest DARE User Day Site[2].
To facilitate full custom design an ADK is provided. As longest running technology the DARE180U one has made an evolution together with the improved learning based on dedicated test-vehicles and lessons learned on completed projects. In the paper this evolution will be presented and the rest of the paper has the following structuring: in section II the first version of the DARE180U ADK will be described; in section III several results and continuous learning over the years will be described; section IV will discuss the improvements done based on this learning; section V presents some other topics that can be candidates for implementation in future ADK versions and section VI will then summarize the paper.

II. First DARE180U ADK

1) CERN W/L formula

Based on the original specs for TID level of 1Mrad and experimental transistor measurements it was decided to use enclosed-layout transistors (ELTs) for the NMOS transistors. Example layout can found in Figure 2. With this layout W does not correspond directly to the drawn dimension in the layout and the extracted W from the layout by the foundry provided deck does not match with the expected performance of the device. Therefor the W extraction was implemented with a formula based on a paper from CERN[1]. This formula computes the W/L as function of L and B & H, the width and height of the inner diffusion area of the ELT. Increasing L and keeping the B&H the same also increases W. This results in a leveling off of W/L reduction with increasing L. In the original ADK an excel sheet was provided where realizable W/L values can be looked up. Additionally this formula was implemented for schematic capture and in the parasitic extraction deck.

2) ELT p-cell and Verification Support

In the standard UMC technology library p-cell (parametric cells) for the devices are given. In order to allow the same design productivity in the DARE180U ADK p-cells are provided for ELTs.

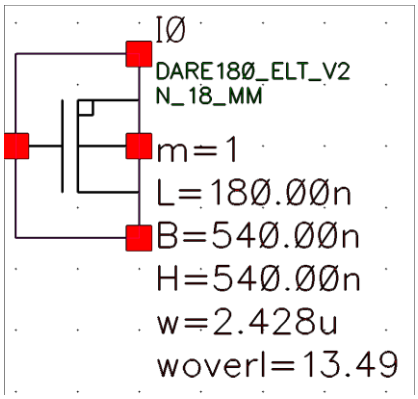


Figure 1: ELT p-cell symbol view instance

In Figure 1 an instance of the p-cell symbol view in a schematic is shown and in Figure 2 an instance of the layout view in another layout. When instantiating one of these p-cell views not the W is specified but B & H, the width and height of the inner diffusion area. Based on this, the W and W/L are computed with the formula as introduced earlier. The resulting values are shown in the schematic as reference. Additionally more correct estimates are done for the inner and outer diffusion perimeter and area so pre-layout simulation are closer to the post-layout simulation. For layout p-cell parameters are present that allow to choose on which side to put contacts in the outer area and at which side to put a P+ guardband.

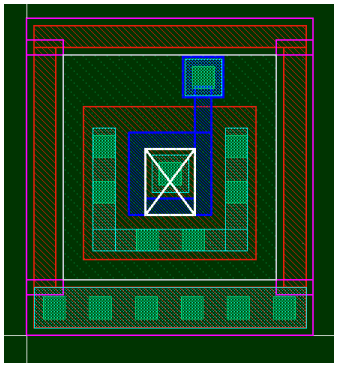
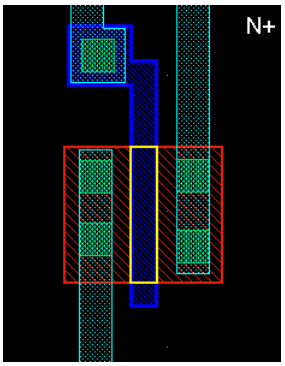


Figure 2: ELT p-cell layout view instance

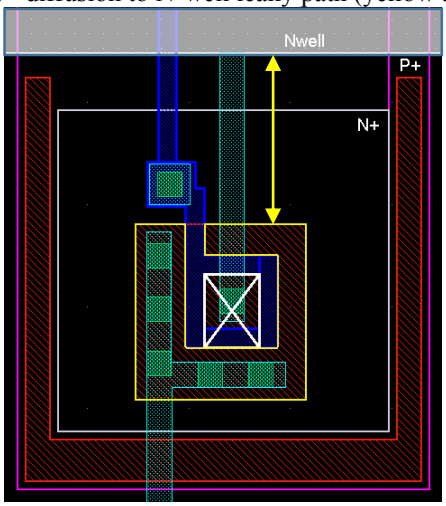
3) RAD check

In the first ADK an extra Calibre deck was provided to check for violations against agreed radiation mitigation rules. Following is a list with an example picture showing each of the rules:

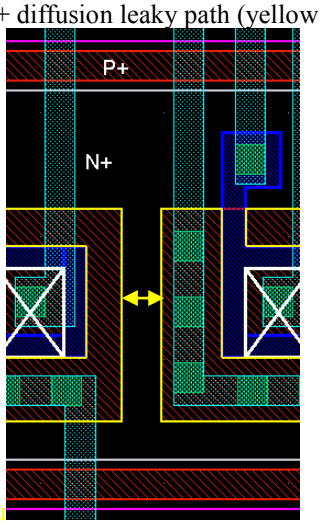
- Straight NMOS transsitor



- N+ diffusion to N-well leaky path (yellow arrow)



- N+ to N+ diffusion leaky path (yellow arrow)



III. Continuous Learning

Over the years several projects have been run using the DARE180U technology. Some of the projects included dedicated test-vehicles to increase knowledge on the radiation effects and mitigation, for other projects some ADK improvements were identified at the start and during the course of the project. The lessons learned in all the projects is also knowledge used as a guidance for ADK improvements. This section will summarize the learning for which improvements and extensions to the ADK have been implemented; section IV details the implementation in the ADK.

1) Latch-Up Mitigation

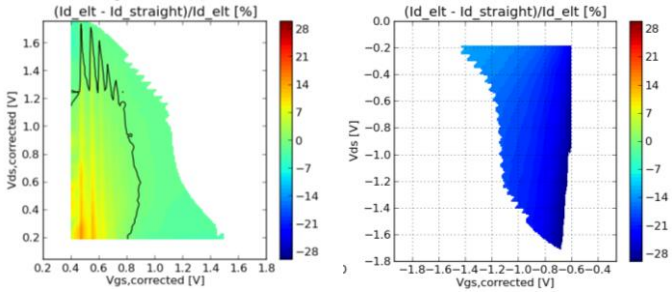
When using P+ guard bands in digital CORE and IO cells a good contact is made to the P-substrate. This prevents single-event latch-up (SEL); experimentally confirmed by never having seen a SEL on a DARE180U based ASIC. For analog designs, the use of big(ger) transistors, non-digital voltage levels and optionally triple-well devices could reduce the latch-up mitigation. For such cases extra rules may be wanted in addition to the default technology N-well and P-substrate contacting rules.

2) In-Depth Straight vs. ELT TID Experiments

In DARE+[3] - a follow-up project on the original DARE project - more in-depth measurements on unradiated and radiated test vehicles have been carried out. An overview of the ADK related results is discussed in this paragraph.

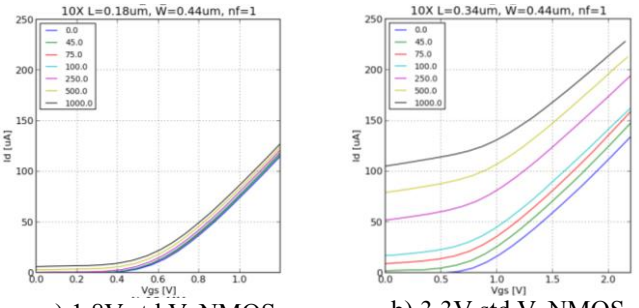
First the ELT W extraction as computed out of the W/L CERN formula is verified by comparing drain current between ELT and straight transistor with equivalent W. The measurements are done on the same die so process offsets are removed from the equation.

In Figure 3 the relative offset between the two is given, the equivalent W straight drain current is derived by interpolating results for a wider and narrower straight transistor. A black contour line is drawn where the drain current matches. For the given NMOS this is shown in the picture displaying reasonable agreement between the two, but for the PMOS the measured current on the ELT is always significantly lower than the equivalent straight transistor. The same trend is seen when looking at other device dimensions and the 1.8V, 3.3V, std. V_t & low V_t ones. The reason for this difference can have several causes and more work needs to be performed to fully understand this effect.



a) 1.8V std V_t NMOS b) 1.8V std V_t PMOS

Figure 3: Relative measured offset between straight and ELT with equivalent W



a) 1.8V std V_t NMOS b) 3.3V std V_t NMOS

Figure 4: measured TID induced leakage current for straight NMOS

Also measurements have been done at different TID levels for an extensive set of structures. In Figure 4 the I_d-V_{gs} curve for the straight NMOS transistor is shown; for a 1.8V device on the left and 3.3V device on the right. For the 1.8V device the curves are shifting in the Y direction as a function of the TID which corresponds with a leakage current that is only a function of TID. For the 3.3V device next to the much bigger shift in Y also a modulation by V_{gs} is seen in the sub-threshold area; meaning that this can't be represented with a leakage current being only a function of TID. In Figure 5 the extracted leakage current are given for 1.8V NMOS for different L & W values. Except for the narrowest device not much influence is seen of W on the leakage current; for L a maximum leakage current is seen around 0.7µm. Accurate measurement of the smaller currents can take quite a long time and due to the limited time window available for measurement during a TID measurement campaign the accuracy is capped. The I-V curves as presented in Figure 4 are measured over several dies and the extracted leakage currents with too much variation over the dies are filtered out. These results are left out in Figure 5 which occur for TID values equal and below 250krad.

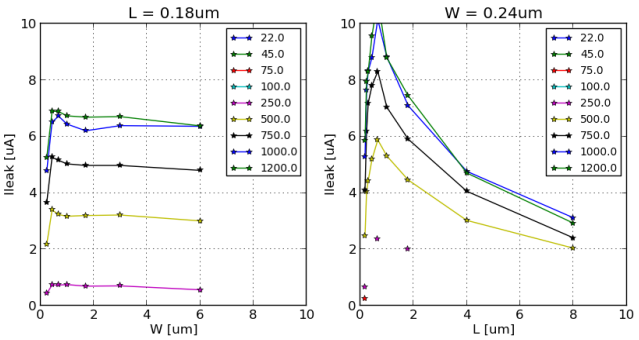
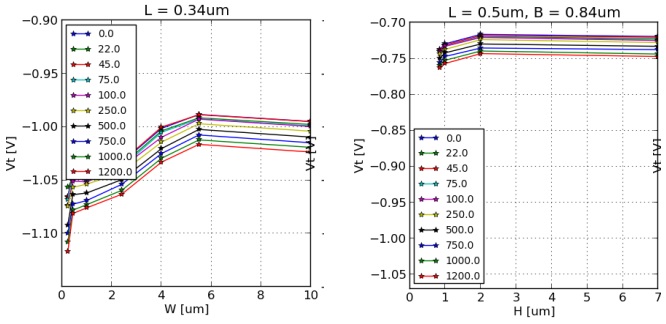


Figure 5: measured TID leakage current induced for straight std. Vt 1.8V NMOS as functions of W and L



a) straight std V_t 3.3V PMOS b) ELT low V_t 3.3V PMOS

Figure 6: Measure TID induced $V_{t,sat}$ shift on 3.3V PMOS

No TID induced leakage was measured on ELT NMOS transistors or on straight or ELT PMOS ones. For the 3.3V PMOS devices a small TID induced V_t shift was measured; results are shown in Figure 6. The V_t is in saturation and is extracted from the measurements by fitting a linear line to the I_d-V_{gs} curve; using a V_t fit method based on higher order derivatives of the I-V curves is difficult due to the measurement noise and repeatability. The absolute value will differ from V_t reported in other places using other fit methods. Next to the I-V results reported in this paragraph a much more extensive set of device parameters have been measured for TID sensitivity. A quick overview:

- Matching: no effect of TID observed
- C-V: no effect of TID observed
- Noise: no effect of TID observed
- Diodes: no effect of TID observed
- Bipolar: TID induced beta degradation measured
- Parasitic Field Devices leakage: TID induced leakage between n-type regions measured but the impact of poly and metal routing in between them is not understood. Measurements seem to indicate that the need of P+ guards can be relaxed in certain layout configurations but further investigation with an extended test set is needed to confirm that.

3) ELT Parasitics

In previous paragraph it was already shown that W/L formula of the ELT is a good approximation for the drive capability of the NMOS device and is also possible with some correction for the PMOS. Commonly, for analog designs not only the drive current of the device is important but also the parasitics; this includes for designs using high(er) frequencies, feedback loops,... . The layout for the ELT was already given in Figure 2 and in Figure 7 the well-known normal straight transistor is shown. The gate area used in BSIM3 SPICE models is assumed to be equal to (W+ΔW)*(L+ΔL); for the ELT the actual area is larger than the one computed with the equivalent W. The actual area increase starts from 30% for the minimal dimension device up to 90 % for a 10µm long transistor.

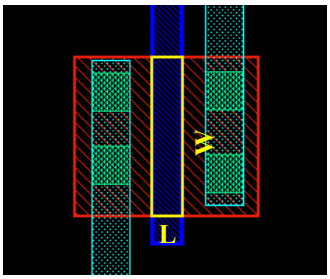


Figure 7: Regular Straight Transistor Layout

For the ELT as given in Figure 2 the gate to source or drain overlap is asymmetric between inner and outer diffusion area. BSIM3 model assumes that this overlap is symmetric and with the length equal to W. For this length and thus the gate to source/drain capacitance differences from 10% to 90% are seen; smaller for the inner diffusion area and larger for the outer diffusion area compared with straight transistor.

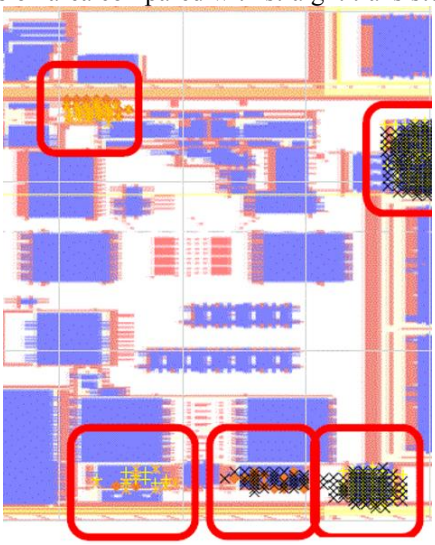


Figure 8: SET sensitivity laser testing report correlating with hot PMOS transistor locations

4) Hot-PMOS

As is shown in Figure 8, during SET laser testing of a chip it was found that some PMOS transistors with N-well not connected to the supply net were more sensitive to single-event effects than expected from charge injection based simulations. The physics are not fully understood yet although bipolar amplification is thought to have a play here. Without full understanding also no detailed design guide lines can be given. In the meantime as a precaution it is best to avoid using these devices or use MiM or MoM capacitances.

IV. DARE180U ADK IMPROVEMENTS

Based on the learning presented in the previous chapter, improvements have been made in different places in the ADK. The measured beta degradation of the bipolar transistor is not modeled but the measurement results are provided to the ADK users on request. For the P+ guard band checks the conservative approach of enforcing them in between all n-type regions on a different net is kept.
The next paragraphs will detail the improvements.

1) Schematic Capture Rad. Hard. Related Warnings

The RAD check from the first ADK is performed on the layout. Preferably already during design phase radiation hardness would be taken into account. For this purpose the "custom Virtuoso schematic checks" feature is used. In Figure 9 the list of checks as seen from the schematics rules checks setup window is given. Each of these checks can be put to be ignored, to give a warning or to give an error. The general default setting used when opening a schematic views can be configured for each of the rules in the setup of the ADK and thus be adapted to the designer's chosen radiation mitigation strategy.
When ADK setup is not changed the following checks are performed. The usage of straight 1.8V NMOS transistors will give a warning; the impact of the TID induced leakage can be verified by simulation as explained in the paragraph on improved modeling. The use of 3.3V NMOS devices gives an error and for these devices no TID induced sub-threshold current model is given. The modulation of the sub-threshold current by V_{gs} complicates the modeling and would need a more extensive data set than is currently available. Also by default a warning is given for the usage of the 3.3V PMOS to indicate the (small) TID induced V_t shift that is also modeled for simulation. And finally a warning is given for the use of hot-PMOS transistors that are possibly more sensitive for single events; for this check valid net names for the PMOS bulk connections have to be configured during setup of the ADK.

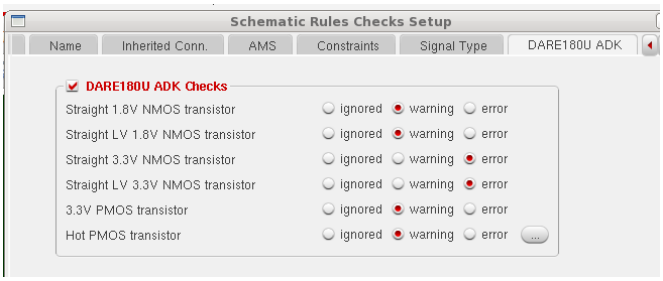


Figure 9: List and configuration of DARE180U ADK custom schematic checks

2) Optional LU Checks

The RAD check was extended with optional latch-up checks for more dense well contact placement and usage of guard rings at the edge of wells and in between wells. In Figure 10 an example is given. In the ADK manual the full list of the optional checks is explained.

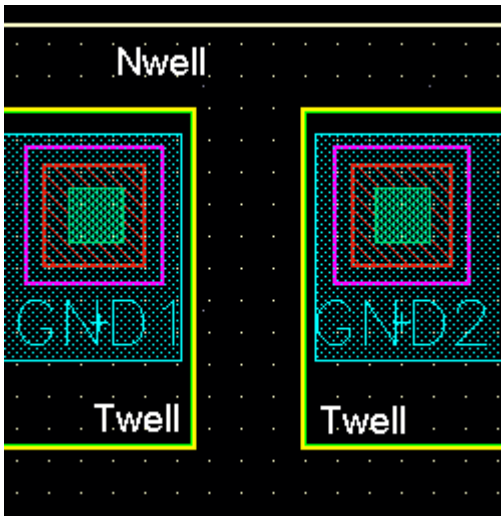


Figure 10: Optional latch-up check for Triple Wells inside same N-well connected to different nets and not isolated from each other

3) Modeling Improvements for Parasitics and TID

The transistor simulation models have been modified to include measured radiation effects as presented in previous chapter. UMC provided models are used as base to avoid a full calibration exercise and to minimize discrepancies with simulations performed using the original models. Below is an overview of the modeled effects.

- Correction of the computed equivalent W for the PMOS ELTs to account for the lower measured drive current
- Correction in computation of the gate area, gate-to-source/drain overlap capacitance and the inner and outer diffusion perimeter as explained in the paragraph 'III.3) ELT Parasitics'
- Modeling of the TID induced leakage current for straight 1.8V NMOS transistors. Simulation process corners at different TID levels are provided. Next to the tt (=typical-typical) corner also a tt_250k, tt_500k, tt_750k, tt_1000k corner is provided; this is repeated for all UMC provided process corners.
- Modeling the (small) TID induced V_t shift for the 3.3V PMOS transistor. This is also modeled by providing simulation process corners at the same TID levels as for the TID induced leakage.

4) Schematic Driven Layout Compliance

Over the years the Virtuoso full-custom/mixed signal design flow is extended to improve productivity of the designer. This includes tools like Virtuosos Layout (G)XL & EAD. For this to work well proper support in each of the views has to be implemented, including the ones provided in ADK by the ELT p-cell. In Figure 11 an example layout is shown; it includes a NMOS and PMOS ELT transistor and due to proper support in the p-cell the nets as defined in the schematic can be visualized.

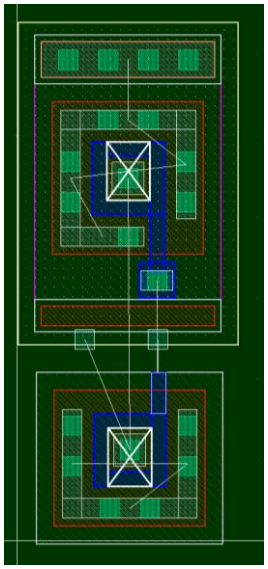


Figure 11: Layout showing connectivity compliant pcell layout view

V. Interesting Future Additions

Developing EDA tools and a mixed-signal/full-custom design flow is never finished. There will always be room for improvement or extension of the flow. Some candidates that came out of the discussions during all the designs and contacts with the community are presented in following paragraphs. For further discussion on one of the topics always DARE support [4] can be contacted.

1) Full physics based ELT device model

Currently the equivalent W and the parasitics computation of the ELT are based on geometrical based derivations. With the current availability of memory size, compute power and 3D process and device TCAD simulation tools it should be possible to simulate device performance based on device physics. This way it can also be validated if there is an asymmetric behavior in performance between current flowing through the ELT from inner diffusion to outer diffusion or in the other direction.

Setting up a 3D TCAD simulation for a non-conventional shape like the ELT is involved, especially if not only steady state effects are of interest but also transient effects like gate capacitance and the gate to source/drain overlap capacitance. For analog design already the transistor performance variation over the process corners is taken into account and in this light the effort to calibrate a full-physics based ELT model has to be weighed against the added value and reduced risk.

2) Modeling Parasitic Devices for SET Simulations

The foundry provided PDK provides support for digital and analog/mixed-signal design. In such a flow not all parasitic devices are important and not all of them may be modeled; for example for the UMC 0.18mm PDK the N-well to P-substrate diode is not modeled. When looking at single-event effects these devices may play an (important) role and models would be preferred for doing SPICE level simulations. Providing support for these parasitic devices not only the model has to be calibrated based on experimental results, likely well and substrate resistance has to be included in this exercise also.

Also the necessary views have to be provided and adapted so these devices can or have to be included in the schema and layout. The extraction deck has to be updated so the parasitic devices are recognized in a layout etc.
In the end, one may end up not with an ADK that is an extension of the foundry provided PDK for specific radiation hardness design requirements but a full revision of the whole PDK. PDK development is already considered a tough job by the foundries for their high-volume commercial processes so support is needed from the community if similar work needs to be performed for the low-volume space community.

3) SET simulation flow

The current ADK is now able to provide the necessary input to the designer to allow for easy investigation and mitigation of TID induced effects.
For single-event simulation currently manual or at best semi-automatic flows are used. Also at imec an internal flow is used for single-event simulation based on charge injection on selected nodes. It's a combination of semi-automated scripts and more manual work like node selection, ad-hoc simulation setup, etc. Another example of a flow is AFTU[5] working on Spectre netlist level and guided automation using Virtuoso Ocean simulation scripting.
Such flows are a perfect candidate to be much more automated by the proper use of scripting and the proper EDA tools and integrating in the ADK design flow. The work involved to go from an ad-hoc flow used in a specific setup to a more generalized and more automated one, should not be underestimated though. With cooperation with and support from the community it would be able to provide that as part of the ADK.

VI. SUMMARY

In this paper the improvement and the extension of the DARE180U ADK was presented based on continuous learning from IP development, ASIC tape-outs and test-vehicles. The combination of all added features in the DARE180U ADK allows designers to work in a flow that they are familiar with, benefiting from the productivity support provided by state-of-the-art EDA tools while including knowledge of radiation hardening-by-design of the technology. It allows the designers to focus on circuit performance and specific radiation requirements using a flow similar to the foundry-provided PDK flow enabling full custom/analog, digital standard cell and mixed-signal IP development.
Also some future improvements and extensions that can be implemented given the needed cooperation with and support from the European space community.

ACKNOWLEDGEMENTS

Due to the long history of the DARE180U a lot of parties have contributed to the advancement. First is the interaction and discussion with CMOSIS on the parasitic modeling of the ELT transistors. Conclusions on data can only be valid if hard work is put into the setup and dutiful execution of the measurement; in this case impossible without the dedicated work of microtest, Alter Technology and MASER Engineering. Discussions with and input from Thales Alenia Space Belgium and ICsense has been the seed for the latch-up checks. The other users of the ADK are always challenging us and thus help us to improve the tool to better fit their needs; this includes S.A.B.C.A, Cobham-Gaisler, Arquimea, RUAG, and IMSE-CNM.
Finally the expertise of the ESA officers is also invaluable as a guidance and help for getting projects successfully to completion and needs known to us.

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