DiReRa: New Rad-Hard Chip-Set for Radiometers

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Abstract

Current RF front-ends for L-band radiometers are implemented using discrete or low integration level devices, which leads to quite large complexity, size, weight and cost of such front-ends. This paper describes the first prototypes of an RF front-end chip-set – called DiReRa – which consists of an L-band RF down-converter and a 1-bit AD-converter, and which can be used to implement the RF subsection of a radiometer in a much more compact and simpler way. Although developed specifically for radiometer applications the DiReRa chip-set is general enough to cover also many other applications, mainly in the telecommunications domain.

This project is a collaboration between Saphyrion Sagl and TRYO Aerospace (former MIER Comunicaciones). Saphyrion is in charge of developing the DiReRa chip-set, while TRYO Aerospace contributed with the specification of the chip-set and is in charge of developing and manufacturing the next generation radiometers that will use the DiReRa chip-set in their RF subsystem. LICEF-3 EM units from the SMOS program will be used to verify the functionality and performances of the prototype chip-set.

Currently a 1st prototype chip-set, manufactured on the AMS S35 HBT SiGe process as MPW and electrically tested and characterized is available. The DiReRa chip-set demonstrated rather good performances, as well as good agreement between simulations and measured results. The next steps should be to first finalize the design of the chip-set, then proceed with its qualification and industrialization.

I. Introduction

Saphyrion Sagl is developing under an ESA contract [1] a new chip-set for L-band radiometer applications. The chip-set consists of an RF down-converter, which is called DiReRa, and a latched comparator (1-bit AD-converter), called DADC. The chip-set is being developed in collaboration with TRYO Aerospace, who will use it on their next generation of radiometers.

The objective of this work is to integrate the RF front-end subsystem of the L-band radiometer into a chip-set, such that its complexity, power consumption, size, weight and cost can be reduced substantially with respect to those of current discrete implementations. The devices will then be manufactured and assembled using a SiGe process [2] and techniques compatible with Space operation and qualified to ESCC9000 [3]. Such chip-set would have substantial potential in applications that need a large number of small highly integrated radiometers, such as the Soil Moisture and Ocean Salinity (SMOS) mission, with further potential e.g. in the SMOS-Ops, GEO-sounders or the Sentinel-3 missions.

In order not to compromise the performances or the radiometer the performances of the IC implementation of the RF front-end should be comparable to the ones achieved by the current discrete implementations. Since an integrated circuit is very different from a discrete design, some changes to the RF subsystem are needed to achieve such objective. It is quite fundamentally impossible to design an exact 1:1 replacement of a discrete design in IC form.

In this paper the architecture of the new chip-set and the radiometer including it, as well as the design choices and trade-offs, will be presented, followed with some circuit details. Results from the electrical characterization will be presented next. As a conclusion the remaining steps towards industrialization and space qualification to ESCC9000 of the chip-set will be shown, together with the planned road-map.

II. Circuit Description

A. IC Characteristics and Constraints

An IC is very different from a discrete design. When specifying an IC it is therefore important to consider these differences, otherwise the resulting specification is very likely not realizable. The most important characteristics that shall be taken into account when specifying an IC are these:

- **Single process must fit everything,** which means that all blocks shall be designed using the same component types with the same characteristics.
- **Limited component values with large tolerances.** Typically there are just 1-2 transistor types, resistors are limited to a few 10Ω to a few 100kΩ and have 20-25% tolerance, capacitors are limited to some 10pF and 10-15% tolerances, while inductors range between about 200pH and 5nH and have low Q. Distributed components (couplers, power splitters, etc.) do not exist at all at low GHz frequencies.
- **Excellent component matching:** this is a characteristic peculiar to ICs. Relative tolerances in the 1% to 0.1% can be achieved rather easily despite the large absolute tolerances of IC components.

- **Coupling through the substrate.** All components in an IC must share the same substrate. The achievable isolation between them depends on frequency and is limited to about 20-30dB at frequencies of 1-2GHz. This limits e.g. maximum gains, crosstalk between channels or attenuation of filters. Balanced circuits are almost always required.
- **Limited number of pins.** In RF circuits package and pins parasitics have a large influence on RF performances. The only way to reduce their influence is to use very small packages with short pins and bonding wires, which in turn limit the number of pins.

B. Radiometer Architecture

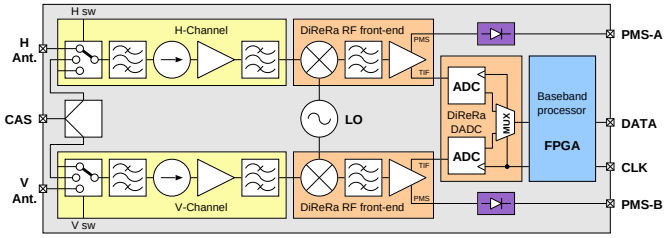

Figure 1: Block diagram of the radiometer.

A simplified block diagram of a future radiometer core using the DiReRa chip-set is shown in Figure 1: it implements full H-V polarimetric mode and is able to measure both H and V polarizations at the same time.

The RF subsystem consists of two identical RF front-ends that include a discrete RF path (LNA, isolator and filters) and a down-converter (mixer, IF-strip) implemented with the DiReRa chip-set, shown in orange in the figure. The local oscillator and PLL are implemented again with discrete components. In order to obtain the best possible isolation between H and V paths separate front-ends are used, which will be enclosed in separate cavities.

The outputs of the DiReRa RF ASIC then go to the power measurement subsystem (PMS) and to a DiReRa DADC 1-bit AD-converter (dual comparator) chip, where it is sampled and digitized. Baseband processing is finally implemented on an FPGA, whose output goes to a digital correlator.

The use of the DiReRa chip-set in the RF subsystem is expected to lead to a quite substantial reduction of weight and size of future radiometers. LICEF-3 EM units from the SMOS program will be used to verify the functionality and performances of the prototype.

C. Semiconductor Process Selection

The choice of a semiconductor process for DiReRa cannot be done based on performances alone, but also needs to consider additional parameters, both technological and non-technological. The most important requirements are:

- Proper RF performances at GHz frequencies.
- Available in quantities compatible with Space applications, i.e. a few 100 pieces yearly at most.
- Can be radiation hardened.
- Sufficiently low NRE costs, in particular the price of the full mask-set.

A space-qualified process fulfilling all requirements could not be found, thus the commercial AMS S35 process [2] was selected on the basis of the good experience made with the design and qualification of the SY10x7 GNSS chip-set [4], [5] that are designed using this same process.

The AMS S35 is a 0.35µm HBT BiCMOS process that includes NPN BJT with a transit frequency of 38GHz, 3.3V CMOS transistors, as well as high and low ohmic resistors and high quality MIM capacitors. Rad-hard standard cells and I/O pads libraries previously developed and tested by Saphyrion during the SY10x7 project were also readily available.

D. DiReRa RF Front-end Architecture

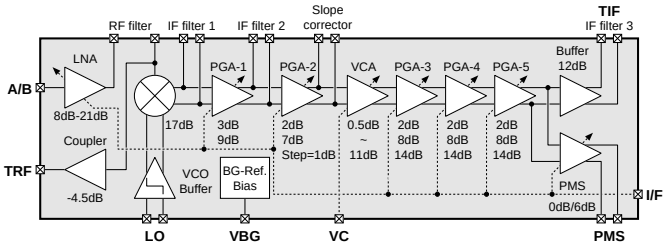

Figure 2: Block diagram of the DiReRa RF front-end.

The DiReRa RF front-end ASIC is a single conversion superheterodine RF front-end that includes all blocks needed to build the RF section of the L-band radiometer.

Figure 2: shows the block diagram of the ASIC. It contains a programmable gain LNA (2 different gains), a double-balanced active RF mixer with active input signal coupler (transmission-line couplers do not exist in IC form), an IF-strip comprising digitally programmable gain stages (PGAs) and a VCA stage, and finally an IF output buffer with linear power measurement amplifier and the output for the 1-bit AD-converter.

1) Frequency Plans

The DiReRa RF front-end is a wideband design with no on-chip filtering, it thus supports a wide range of frequency plans. Some possible frequency plans – based on ESA and TRYO Aerospace requirements – are shown in Table 1:

Table 1: Some possible frequency plans for the DiReRa chip.

RF Freq.	LO Freq.	IF Freq.	fs.	Unit
1200-1600	1180-1580	25-35	130	MHz
1413.5	1396	17.5	55.84	MHz
1200-1600	1167.5-1567.5	32.5	130	MHz
1200-1600	1037.5-1437.5	162.5	130	MHz
1413.6	1288	125.6	55.84	MHz

Basically good frequency plans for an RF receiver with IF sampler are obtained by placing the IF roughly in the middle of a useful band of the AD-converter, i.e. IF=fs*(1+2N)/4,

with N an integer. Since due to the requirement to support widely different frequency plans the DiReRa ASIC does not contain any image reject mixer and has to rely uniquely on external RF filtering, frequency plans with a low IF that place the image frequency very close to the desired RF frequency will lead to rather challenging RF filter design.

2) Circuit Design

The main circuit blocks of the DiReRa chip, as well as the required external filters are described here. Support blocks such as the interface (parallel, combinational) or bias and band-gap reference circuits are omitted.

- **LNA:** It is a single stage inductively degenerated cascode amplifier, which provides 2 programmable gains. Such architecture was chosen to achieve good noise figure and linearity at the same time. It provides G = 18.0dB and NF = 1.7dB for the high gain setting, G = 6.5dB and NF = 2.3dB for the low gain setting. The ports are 50Ω unbalanced and require external matching networks.
- **Mixer:** An active double-balanced mixer has been used. Double-balanced active mixers provide good linearity, good local oscillator and common-mode rejections (substrate coupling, isolation from LNA) without requiring high LO drive levels at the expense of noise figure. All ports are balanced, the input port is 50Ω, the output port is 600Ω, while the local oscillator port is high impedance to simplify bridging of two channels on a single LO signal. The mixer has an SSB voltage gain = 14.5dB and NF = 12dB.
- **IF-strip:** it is a 7-stage amplifier chain consisting of 5 PGAs, a VCA, an output buffer and a PMS amplifier. A differential amplifier structure has been used throughout, in order to achieve rejection to common-mode signals and noise. The gain of the IF-strip can be programmed digitally in 1dB steps, while a VCA analogue input provides a further regulation over a 10.5dB span. The overall gain can be set from 19.5dB to 71dB nominally. All I/O ports are 600Ω balanced, and given the rather high gain that the IF-strip can achieve it is important that all ports are kept well balanced, otherwise instability or oscillation due to substrate coupling may occur.
- **Filters:** The DiReRa front-end is a wideband design and requires external filters to select the channel and remove the image frequency. At RF a SAW filter can be used quite effectively and has a small size, while at IF a coupled resonators LC-filter has been selected. This filter topology is particularly suitable for use with an IC receiver since the resonators will present a low impedance outside their bandwidth (i.e. the ports become shorted), thus improving rejection to substrate coupled signals.

Currently the 1st prototype of the DiReRa chip has been completely designed, integrated using the MPW program of the foundry (AMS) and successfully tested and characterized.

E. DADC AD-Converter Architecture

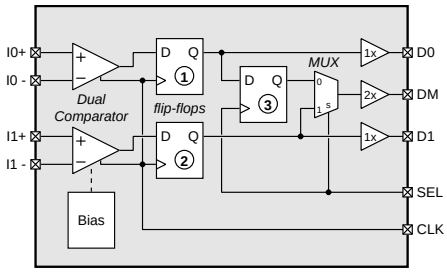

Figure 3: Block diagram of the DADC AD-converter.

The DADC 1-bit AD-converter is a dual latched comparator operating at up to 130MHz. It is meant to digitize the IF signal coming from the DiReRa front-end (TIF output). The most critical requirement is a 0-1 imbalance of 0.5% that should be obtained with no on-line calibration.

Figure 3: shows the block diagram of the DADC chip. The device includes two 1-bit AD-converters (comparators). The output of these comparators is stored in flip-flops 1 and 2 before being delivered to the output directly and through a multiplexer. The select input for the multiplexer is also the clock of flip-flop 3 and is available externally. An external delay shall be added between signals CLK (main clock) and SEL (delayed clock).

1) Circuit Design

Again only the main circuits – i.e. the comparators and the latching and deglitching circuits are described here.

- **Comparators:** they are latched regenerative comparators. Such comparator structure has been chosen since it provides high sensitivity (it can resolve signals <1mV rather easily), high speed and a clean low jitter sampling together with low power consumption. A rather careful design of the comparator is necessary to fulfil the specified 0.5% 0-1 imbalance specification. The intrinsic matching between transistors (a characteristic of the process) will become the limiting factor. The comparators are clocked with the CLK signal.
- **Latches and deglitching:** in order to have stable values the output of the comparators is latched into flip-flops (1 and 2 in Figure 3:) before being output. The outputs D0 and D1 change on the rising edge of CLK. The two comparator's output also go to a multiplexer. A deglitching flip-flop (3) – clocked by pin SEL – was requested by TRYO Aerospace for compatibility with their existing radiometer designs. In order to operate properly, a delay of ≥2.8ns is necessary between CLK and SEL.

Also the DADC chip is currently completely designed and was integrated together with the DiReRa chip in the same MPW. It has been successfully tested and characterized.

F. Chip Layout

The layout of the DiReRa chip-set is completely made by hand. Since the AMS process used is not rad-hard and thus no rad-hard library was available, all cells and I/O pads were re-designed from scratch following design rules developed by Saphyrion and briefly described in the following Section III.

Figure 4: shows the layouts of the DiReRa RF front-end (left) and the DADC dual comparator (right). The DiReRa RF chip has 42 pads and a size of 1280µm x1200µm. It is meant to be packaged in a hermetic 40 pins CQFN package of ceramic-metal construction (2 pads will be bonded to the die attach pad only). The DADC dual comparator has 16 pads and a size of 610µm x 880µm. It is meant to be packaged in a 16 pins CQFN package, again of ceramic-metal construction.

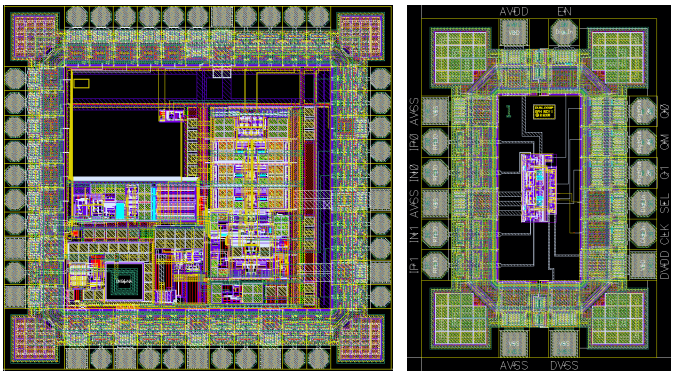

Figure 4: Layouts of DiReRa (left and DADC (right).

III. Radiation Hardening

The DiReRa chip-set is meant for use on board of satellites, thus a rad-hard design and Space qualification (to ESCC9000 [3]) is necessary. On the other hand a process with good RF performances at GHz frequencies is needed while whatever rad-hard technique used shall not degrade electrical performances or dimensions of the chip unduly. Since a commercial process had to be used (Section C), radiation hardening was done completely in-house by Saphyrion.

G. Total Dose

Robustness against total dose effects is mainly a characteristic of the semiconductor process used. Basically thin base BJTs and thin oxide MOS transistors give improved robustness. The process selected for DiReRa is the AMS S35 process, i.e. the same process used for the SY10x7 GNSS chip-set [4], [5] for which extensive TD tests with successful results up to >100kRad(Si) are available.

On the circuit design side, effective design techniques that give good robustness against TD degradations are e.g.:

- The use of balanced signal paths designed with carefully matched differential pairs, such that eventual parametric drifts are compensated,
- The use of active bias circuits that compensate β degradation of bipolar transistors.

These techniques have been used throughout where applicable in the design of the DiReRa and DADC chips.

H. Heavy Ions

SEE can be critical. Customers put indeed much weight on SEE, as previous experience has demonstrated. At the best SEE requirements must be based on existing standards and handbooks [6],[7],[8].

1) Single Event Latch-Up

SEL is a potentially destructive event for which no circuit design tricks exist to counteract it. Devices that show SEL <60MeV·cm²/mg shall be protected against SEL with external circuitry [7]. Our objective is pass at LET ≥85MeV·cm²/mg.

Achieving such an objective is possible also if a bulk (not SOI) process is used, as demonstrated by the SY1017C [5] device, if the following rules are followed:

- Continuous, uninterrupted guard rings are used to separate all opposing N and P areas.
- Good (distributed) substrate/well contacts are placed near to all transistors sources.

Figure 5: shows an example of such rules applied to digital standard cells. In order to save space the cells only contain the horizontal section of the guard ring, which is completed once the cells are assembled into lines. These rules were followed thoroughly in the design of the DiReRa chip-set.

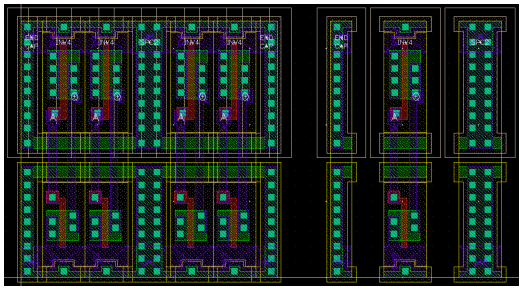

Figure 5: Rad-hard cells with continuous guard rings (example).

2) Single Event Transient, Upset

The DiReRa ASIC is an analogue RF chip that contains no sequential circuit. All control lines are combinational and level sensitive, thus SEU cannot happen. SET have the following effect on DiReRa:

- SET on RF/IF amplifiers and the mixer stage cause mostly noise.
- SET on enable lines may cause a circuit block to turn off and back on.

For the 1st case no particular countermeasure needs to be taken. The 2nd case is somewhat more delicate, as off/on transients on low speed blocks (bias, band-gap reference) may cause long recovery transients. Enable and control lines are protected with *drive strength hardening*, bias circuits are designed to recover quickly from transients, while the band-gap reference is protected with a large (external) capacitor.

The DADC chip contains latches (the comparator itself and the flip-flops) and is thus subject to both SET and SEU. Such effects will cause errors that however result only in

noise. The same protection strategies used on the DiReRa, i.e. drive strength hardening and fast recovery circuits were used also for the DADC. The use of TMR, especially on the sensitive comparator stage, was considered but not implemented due to the little advantage it would have provided.

IV. Test Results

The DiReRa chip-set was electrically tested and characterized in Saphyrion's laboratory. Since the DUTs operate at GHz frequencies, in order to characterize them specific RF test fixtures (PCBs) were prepared. The DiReRa and DADC bare dies were assembled in plastic scoop&goop QFN packages and soldered to the test PCBs. Finally filters and matching networks were aligned.

All measurements gave good results and showed a good agreement between simulated and measured performances. Also the rather critical 0-1 imbalance requirement (<0.5%) for the DADC seems achieved at least under typical conditions. Due to these results no major modifications or adjustments are therefore needed. The chips can therefore be completed and finalized using the unmodified circuit blocks. A summary of the measured results is shown in Table 2:.

V. Conclusions

The DiReRa RF front-end and DADC dual comparator 1st prototypes were designed, manufactured as MPW and electrically tested. Good results were achieved, which would suggest to proceed with the finalization of the design and if no problems are found to proceed with the industrialization. The remaining necessary steps will be the following:

- Do a *preliminary* irradiation test on the current prototype to mitigate any radiation-related risk and to characterize possible radiation-induced drifts.
- Finalize the chips using the current MPW-1 design data, then do an *engineering run*. Production ASICs will be taken from this engineering run.
- Develop and procure the *ceramic-metal hermetic packages* for both ASICs, then assemble a 1st lot.
- Develop *production screening* and run it on the 1st production lot.
- Do a *qualification* of the two devices, possibly in parallel to make better use of resources and save time and money. This involves endurance, environmental and radiation (total dose and heavy ions) tests.
- Prepare the necessary *documentation*, which comprises data sheets, procurement specifications, qualification and irradiation test reports.

At the end of this still quite long process, the DiReRa and DADC chip-set will be ready to be used in an actual radiometer system and will be introduced in Saphyrion's catalogue of Space-qualified ASICs.

VI. References

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Table 2: Summary of measured results.

Parameter	Conditions	Value	Unit	Notes
DiReRa RF front-end				
LNA gain	High gain setting	18.3	dB	Noise matched, 50Ω.
	Low gain setting	6.5	dB	
LNA noise figure	High gain setting	1.7	dB	Noise matched, 50Ω.
	Low gain setting	2.3	dB	
RF mixer SSB voltage gain	Balanced input, 50Ω	14.7	dB	Balanced output, unloaded.
RF mixer SSB noise figure	Balanced input, 50Ω	12.3	dB	
IF-strip overall gain range	TIF output	23.5 to 81.6	dB	PGAs+VCA, balanced I/Os, unloaded.
IF-strip PGA gain step		1	dB	Balanced I/Os, unloaded.
IF-strip VCA gain range	VC = 0V to 2V	12	dB	Maximum gain is limited.
Output 1dB compression point	PMS output, unloaded	−4.5	dBu	Referred to 600Ω.
DADC 1-bit AD-converter				
Sampling frequency	Maximum	130	MHz	Operates from ≈0Hz to 130MHz.
DC-offset	Input referred	±3.7	mV	Measured at DC, 2 samples.
0-1 imbalance	−4dBu, −40 to 125°C	0.5	%	Band-limited AWGN.